Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 02
Fixed and Variable Frequency Digital Control Architectures
Lecture - 18
Sampling Methods under Digital Hysteresis Control Methods

Welcome. In this lecture, we are going to talk about Sampling Method Under Digital Hysteresis Current Control.

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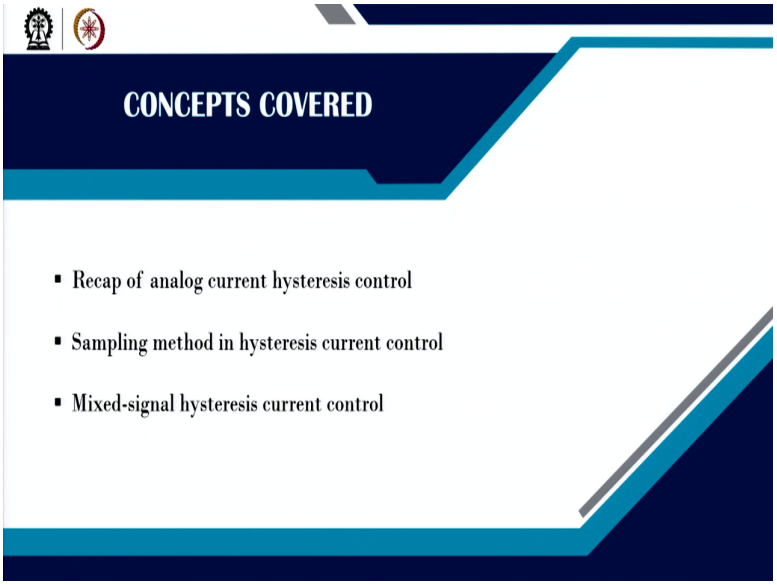

So, we will first talk about you know analog current hysteresis control, then what are the sampling method, and then how to implement it in the mixed signal domain.

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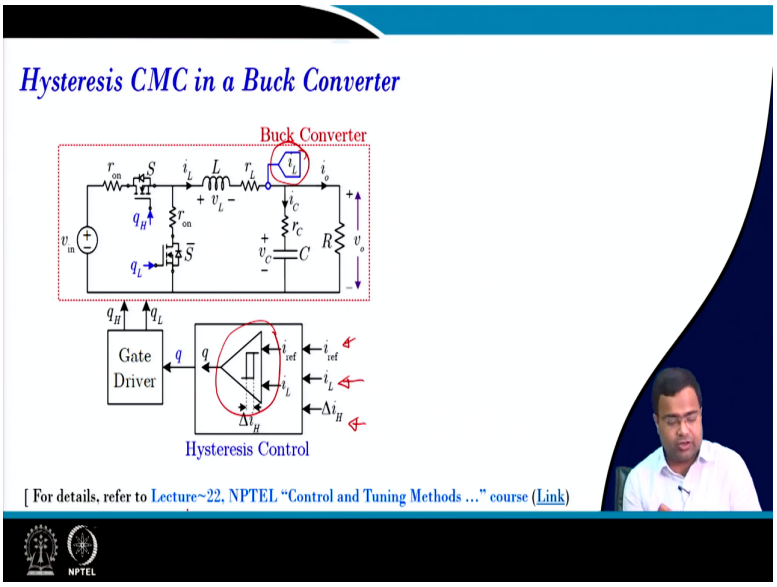

So, let us start with a current hysteresis control in a buck converter, where you know this is the sense inductor current. So, you can put a current sense resistor or any other way. So, the sense current is here, then we have a reference current that has to be trapped and this is the hysteresis band.

And, it is this is you know it can be realized using a pure you know hysteresis comparator and this is the control logic and then it will generate the gate signal. Now, for more detail about this hysteresis control, you can refer to our earlier NPTEL course, lecture number 22.

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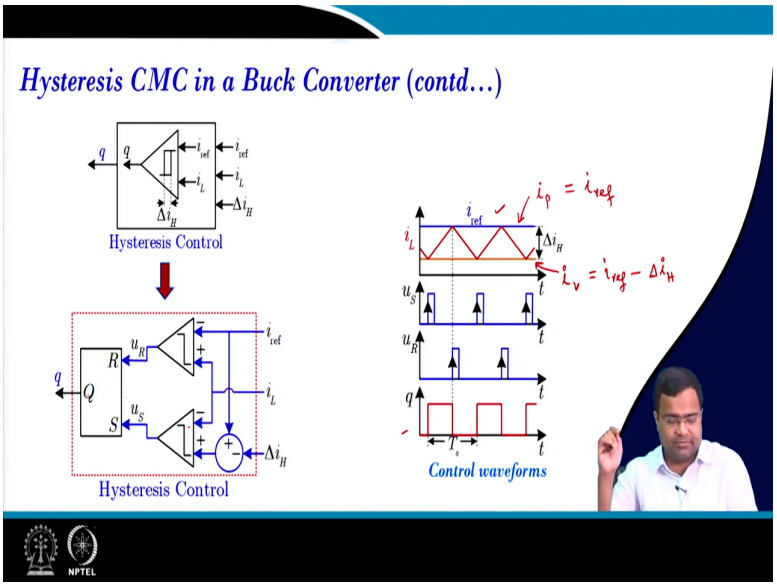

Now, the first step in this hysteresis control is the one way to realize although it is not a harder optimization you know just for sake of understanding you can use two comparators and one R S latch. So that means, whenever inductor current; that means, this is the waveform so, here the first one is I ref and then you have a delta I; that means, the valley current is this is my valley current and this is like my peak current.

So, here I have taken the peak current to be I ref and the valley current is my I ref minus delta I H. An inductor current is forced to follow the trajectory within that; that means, the ripple within that peak and valley. And, that way this R S latch will generate the gate signal and you will get the corresponding gate signal ok. Now, if we increase or decrease the hysteresis band then a ripple will increase and decrease, and as a result, the period will also vary.

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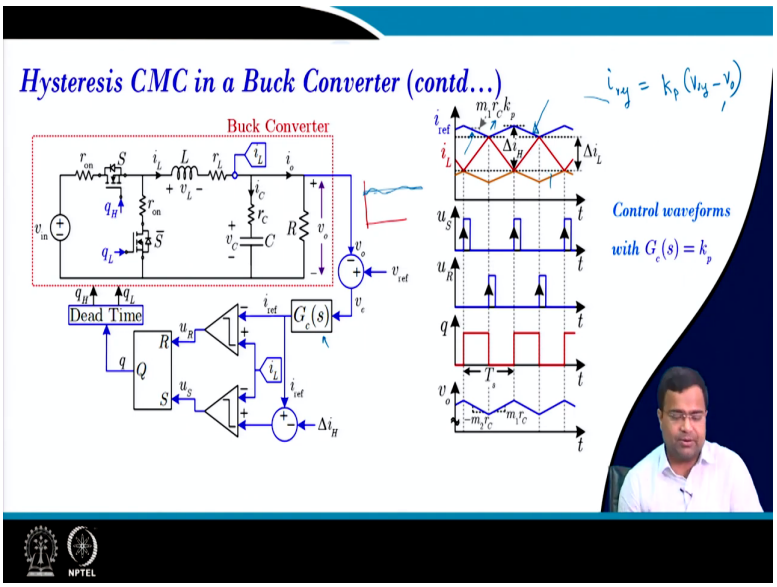

Now, the first question is this; so, here I was showing that if you take a pure you know the constant current different then you can keep the inductor current within that band. But, what will happen if you close the loop? Because, this reference current may be coming from the outer loop and when you implement this current reference, the outer loop means there will be some voltage ripple.

Because, if you draw the waveform of the output voltage, there will be some ripple information will be there, that will be there on top of the average value. And, that ripple will be propagated through this controller, let us say it is only a proportional control if it is then this ripple will be amplified by the proportional gain.

So, the current reference will also have some ripple information and you can see the current reference will carry the ripple information because let us say we are taking I ref to be for simplicity some proportional gain v ref minus v 0. So, you will get an inverted voltage ripple in the I ref profile and since the valley current is simply I ref minus delta H. So, the inductor current will be inside that band.

Now, in this case, the current ripple is not the same as the hysteresis band because due to this ripple in the I ref, that is differing. So, you will get a difference between the actual current ripple and the hysteresis band and that will make the design parameter sensitive and you can say r c is the.

So, if you take a buck converter where the output voltage is dominated by ESR, then the slope of this current ripple is a reference current because the slope of this output voltage is the ESR slope which is r c into m 1 for the rising slope of the current. And, since there is a negative sign so, it will be like a during on time it will fall and then it will be also multiplied by the proportional gain.

So, depending upon the value of proportional gain r c. So, this ripple of the I ripple will vary as a result there is a difference between delta I L and delta I H. So, any analog current mode control if you close the outer loop will suffer from this problem because our ultimate objective was that the inductor current should follow the hysteresis band.

And, at the same time, we wanted to achieve the current ripple to be equal to the hysteresis band. But, that is not possible in analog control particularly in this case when the outer loop is closed due to the effect due to the voltage ripple.

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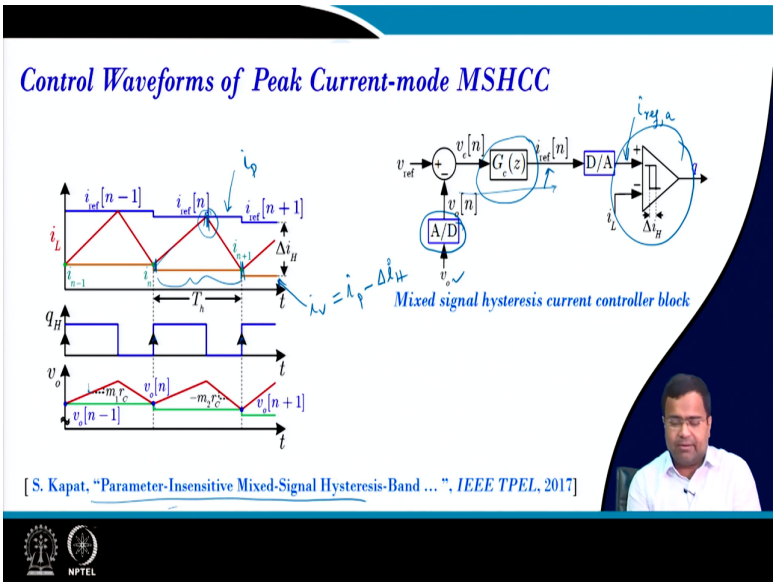

Now, how do you go about digital control? So, suppose I want the voltage loop to be digital, but the current loop is analog. So, if the current loop is analog; that means, you can continue to use the current comparator outside, but only reference current which will be used as one of the inputs of the hysteretic comparator that will be coming from the voltage loop, digital voltage loop now.

So, you need A to D converter; that means, the output voltage is passed through an A-to-D converter, then it is the same method as any other digital control architecture that we have discussed in current mode control or voltage mode control, the output voltage is you know digitized using ADC.

Then, the error voltage is passed through a discrete-time or digital compensator, then this number is digital and it is passed through a D to A converter. Now, the output of the D-to-converter is an analog current. So, it is now an analog current difference, it is in the analog domain and this will be used to compare with the hysteresis, I mean along with the hysteresis band. So, you will get a profile of the inductor current and it is something like this.

Now, since it is a hysteresis control, again this question will come because we have discussed in lecture number 11 that when because, of hysteresis control, the period is a variable quantity because it depends on the band and there is no clock. It is asynchronous, it is a pure comparator base. So, any change in the input voltage, if there is a slope change then the

switching frequency will change, if there is any change in the let us say I ref you know or if you change the delta I H; so, it will vary.

So; that means, the switching frequency can vary, and even cycle by cycle there can be jitter; because if you have any sensing noise in the current that will also cause some jitter in the time period, that is why this is one of the drawbacks of hysteresis control. Hysteresis control is sensitive to measurement noise because there is no latching mechanism or there is no modulation you know unlike in fixed frequency modulation, where it is locked concerning a fixed frequency clock.

If we go to constant on time then we have a monoshot timer particularly the duration is fixed, but the other duration is exposed to the comparator. But, here both the on and off durations are exposed to the comparator output because there will be sensing noise. So, you can always have a jitter in the time period and that will cause a slight deviation in the switching frequency around its nominal value. Even the steady state variation is different, but during the cycle, by cycle, there can be slight jitter in the switching clock, effective switching clock.

Now, the question is since the switching clock itself is jittery and there can be also a variation of the switching clock, because of this operation then how to make it? And, we also saw that you know analog control there is a band you know ref has was carrying some information of the voltage ripple multiplied by the controller gain and how to digitize the voltage ok. So, one of the methods we use a uniform sampling then there will be a there is a mismatch between sampling and switching instant and that will cause multi-limit cycle oscillation for detail one can refer to this paper.

So, if you do not; that means there is a mismatch between the sampling if you use a uniform sampling clock. So, there will be a mismatch between the sampling point and the switching point, and we will call multi-limit cycle oscillation, but if I use an event-based sampling, how to decide the event? So, let us consider the ideal condition, no delay.

So, whenever the gate signal goes high; that means if you take the gate signal which is going out. At the rising edge of the gate signal I take the sample of the output voltage, this output voltage sample and that sample will be constant for the entire duration until the next edge of the gate signal comes. So that means, I am now detecting an event, it is an event-based sampling. Here the event is the rising edge of the gate signal; that means, whenever the gates will turn on that edge will take to take the sample of the output voltage.

Now, one can ask if you cannot take this sample because that will be noisy, but we will see if there will be a delay effect. But, ideally to start with if you take this event as the point of sampling then we will capture the voltage sample. And, then this voltage sample will be processed through this digital comparator and DAC and it will generate the reference current. And, here I am not taking any delay then the waveform will look like the I ref will be constant for the whole cycle.

Even though there can be no ripple of the output voltage, since you are taking the sample at the beginning and you are not allowing any more information of the output voltage to pass through the ADC, there is no more sample you are taking till the next edge come. So, this sample voltage will be insensitive to the ripple parameter so; which means, there will be no variation, it will be constant.

Once you make that; so, this ref will be constant for the whole cycle then the valley current is your peak current. So, this is your peak current and the valley current will be peak minus what? It will be peak minus delta I H right? So, it will also follow the same trajectory, but with the difference in the hysteresis current, the inductor will simply follow. In this case, the current will be as if you see the ripple current and the hysteresis band if you can make sure it is stable, they will be identical ok. So, for further detail about this technique, you can refer to this paper.

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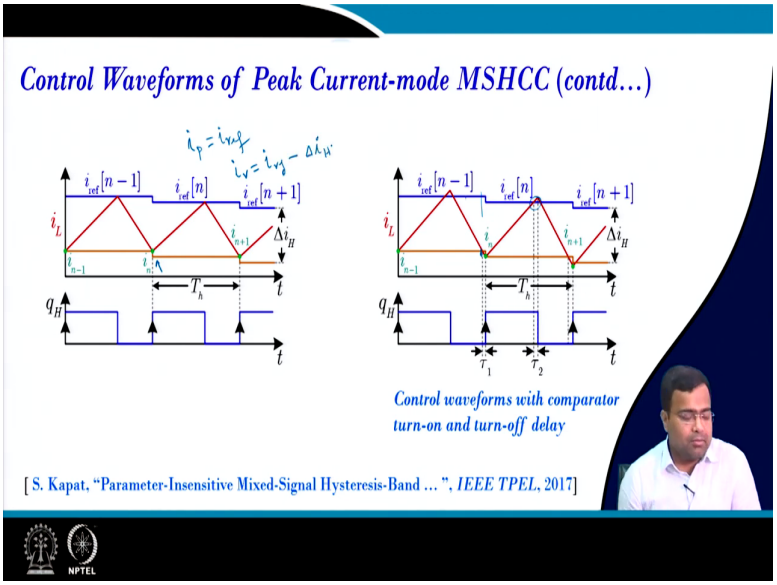

Now, once you do that, what if I told you that ideally, it is not possible, because we do not want and in fact, you cannot take the sample and process it immediately, you also need some time. So, here is the time; that means, you take whenever you get the gate signal; that means, you have to turn on the turn off the MOSFET or turn on the MOSFET high side MOSFET. But, that gate signal when it goes to the actual switch pass through the driver there will be a delay always.

Because the delay is due to the there will be some dead time, there will be driver delay and propagation delay. So, all this delay will be accumulated. So, you are taking a sample when it was before turning off turning on the switch. So, you are taking the clean output voltage sample and in that way, you can update the reference current accordingly. So, you are not taking the actual sample so; that means, your I ref can vary.

Similarly, whenever you have generated I ref; that means, you can take the sample even a little bit earlier you can delay the actual gate signal. So, this delay will also have a stability impact, but we are not discussing this delayed stability analysis, because it will be quite complex and quite advanced. But, just for conceptual understanding, imagine if you can generate the reference current which is a fixed value for the whole cycle, even for the analog comparator there will be some delay of the comparator.

So, your actual inductor current will be slightly greater than the hysteresis band because of the delay in the comparator. So, here the variation in the current ripple and the hysteresis band is due to the propagation delay of the comparator ok.

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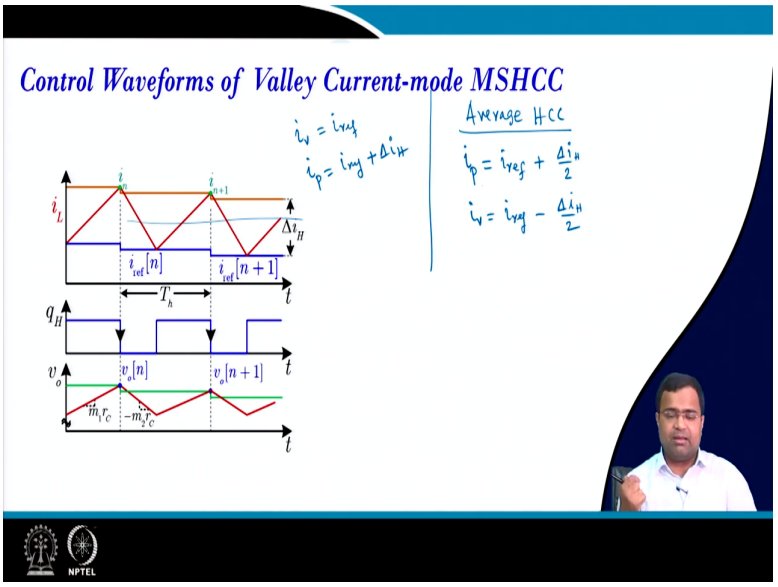

So, you can also implement this technique valley; that means, here I am using the peak value same as the reference, and the valley I am using reference minus delta I H. But, suppose I use reference to be vala ley, in this case, I am using valley to be a reference and the peak is a reference plus delta I H. So, then you can implement valley current mode control. You can also implement average current mode control. How?.

In the case of average current mode control, average hysteresis current mode control you take a peak to be I ref plus delta I H by 2 and I valley to be I ref minus delta I H by 2. Then, you are essentially forcing the inductor to follow this you know the inductor's current profile will be, you know it will be constant within that I peak and I valley. So, naturally, that average will be I ref so; that means, the average inductor current can follow I ref and you can implement the average inductor current.

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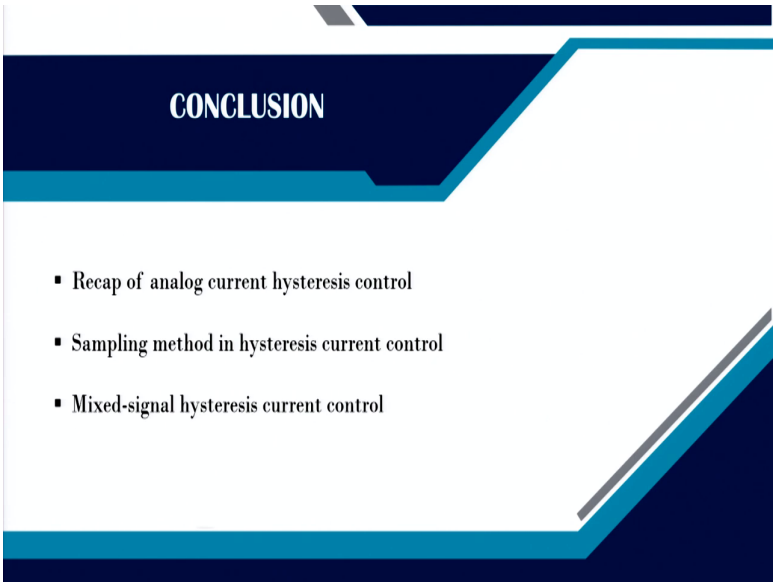

So, in summary, we have recapitulated the analog hysteresis control method, we have discussed event-based sampling in hysteresis current control and we have also discussed mixed signal hysteresis current mode control implementation. But, there are other structures like a fully digital hysteresis control, but these are more like advanced research topics. But, if one can understand how to implement a hysteresis digital control; so, the mixed signal will be the starting point and we will implement it in MATLAB.

So, I want to finish it here.

Thank you very much.