Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 02
Fixed and Variable Frequency Digital Control Architectures
Lecture - 16
Sampling Methods under Constant On/Off-Time Digital Modulation

Welcome. So, in this lecture, we are going to talk about Sampling Methods under Constant On/Off Time Digital Modulation.

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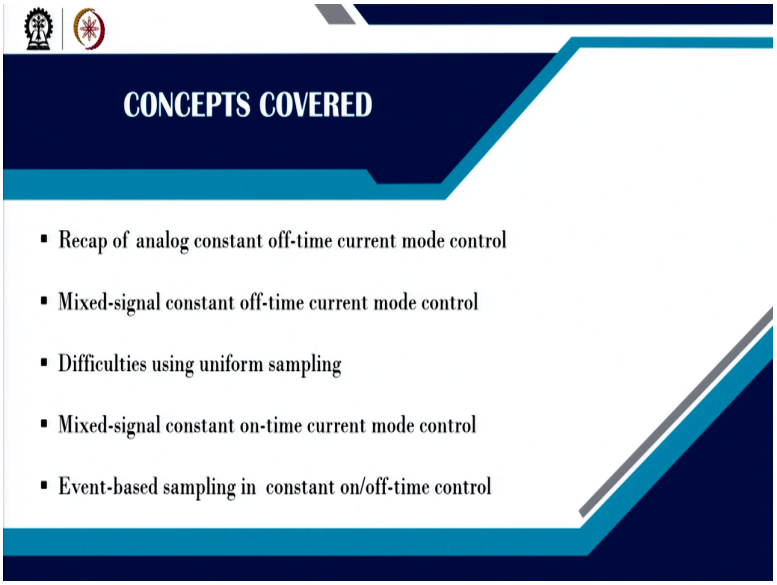

So, here we will first recapitulate our analog constant off-time current mode control, then we want to present mixed signal current mode control; that means, the digital architecture of constant off-time current mode control. Then what are the difficulties using uniform sampling, then what is like what is the logic behind mixed signal constant on-time current mode control and then event-based sampling in constant on-off time control?

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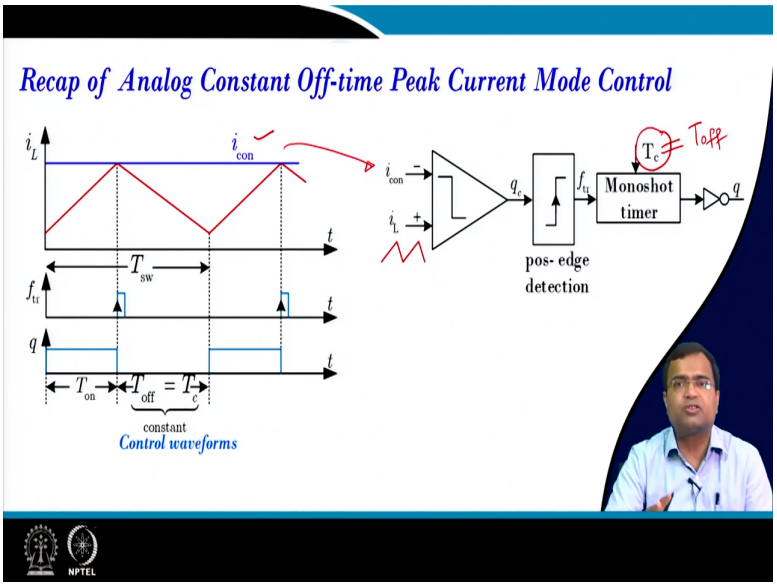

So, if we recap you know our peak current mode like constant off-time control and we have learned in our previous course, in the NPTEL course where you know it is analogous to trailing edge peak current mode control, but the only difference here is the off time is constant. In regular current mode control, our time period is constant; here the off time is constant.

But, otherwise, it is equivalent to the peak current, I may control the peak current, and this; means if you take this peak current reference this is my peak current reference. So, it is here and it is compared with the sensed inductor current and the output of the comparator goes to an edge detection circuit, and then it enables the monoshot timer and this timing parameter is nothing, but our off time.

So, our off time is loaded here and as long as this is off then the output of the monoshot timer will be high and it will simply turn off the switch.

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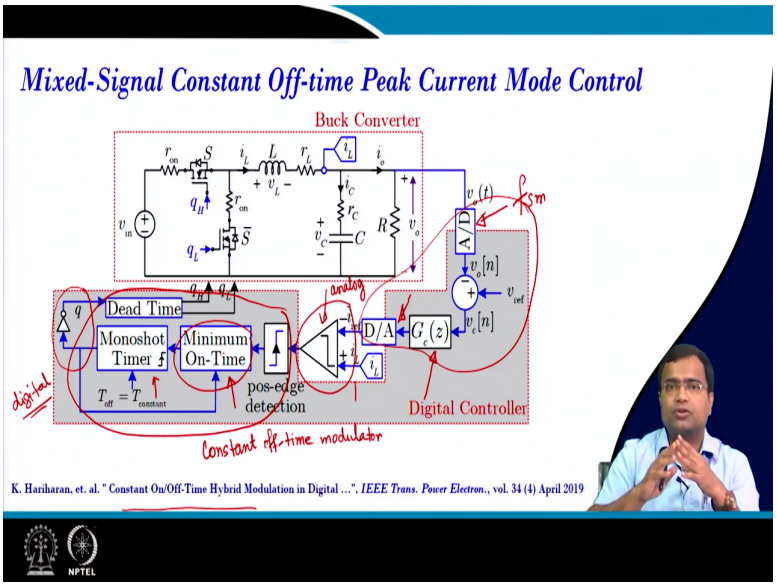

And, what does the mixed signal off-time peak current mode control look like? So, in this architecture we are considering the same method; which means, the analog current loop; that means, it is the peak current reference analog loop and it is compared directly with the sensed inductor current you can see this logic remains the same.

And also that this logic is the monoshot timer logic; that means, this is our constant off-time logic, constant off-time modulation, this is a constant off-time modulator; this remains the same, as what we have done in the analog current mode control. And here reference current is also in analog and inductor current is in the analog domain. So, it is an analog comparator. So, these are all in the analog domain.

But, the only difference in this part, if you look at this part in the analog version there is no digital loop; that means, here since we want to digitize. So, here we need to use an A to D converter and then this is a digital compensator and then there is a D to A converter. And, that is why it is called mixed signal because your current is in the analog domain and the voltage loop is in the digital domain and you know this has been discussed in detail in this paper.

What is the benefit? Because if we talk about the benefit of keeping the voltage loop in the digital loop. You know this paper also it is discussed the same structure one comparator, one DAC, and one ADC you can, reconfigure to constant on-time control suitably, actually you know for constant off-time you need to consider the minimum on-time that we have also discussed earlier. And, the monoshot timer is configured as a constant off-time modulator. If

you change to constant on time then this will be minimum off time and this will be constant on time modulator that is it.

And, then based on this edge detection circuit you need to change this algorithm. So, in this form right now it is default by default set as constant off time, but you can configure it to constant you know on time by switch because this whole logic is in the digital domain. So, this is in the digital domain. So, you can make this logic, you can just little bit modify this logic and it will work. And, everything else remains the same like a voltage loop in digital, and then the current loop, analog number of ADC, DC everything remains the same.

But, we will also discuss whether there will be a change in the sampling clock that one if we take to talk about the sampling clock the what should be the edges of the sampling clock, will be different for under constant on-time and off-time. So, this architecture is quite similar to the analog part, similar to analog current mode control, but the digital part is added.

And, this digital part we can program; as I told it is not necessary that you have to use always the compensator output as the reference current, we can program; that means, we can keep a programmable current limit we can adjust, we can do a trajectory tracking kind of control. So, we can do a very fast recovery control using this modulator.

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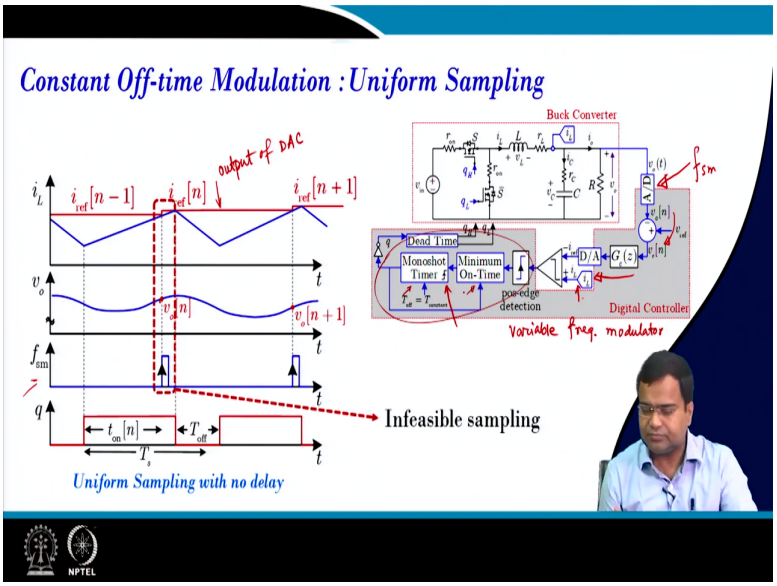

Now, with this constant off-time modulation you know we are using uniform sampling if we use because, as I said we need to discuss this sampling clock; so, what should be the

sampling clock? Because, this is a variable frequency modulator, this is a variable frequency modulator where any small change in your know disturbance in the initial condition or even the sensing noise, can affect even cycle by cycle a little bit there can be jitter in the switching clock.

Because, it is only the off time that is constant here, but the on-time comes from the comparator output. So, if there is any sensing noise and if the noise you know varies cycle by cycle, then you may have some jitter in the on-time and as a result, there can be a slight jitter in the switching clock. So that means there is you cannot guarantee exactly in a real system that on time will be identical.

Now, the question is that if the period is not identical and we can think of a random number that can be a slight variation of the switching frequency for a range within a small range; then how to sample?

If you use a uniform sampling here I am showing, suppose you use a uniform sampling clock which is a fixed frequency. And, you set this sampling clock in such a way that you need to achieve some desired switching frequency; that means, you want to achieve a desired time period by suitably setting this off time and you set this sampling clock.

What will happen? Suppose, if you sample right here and you update because the sample current voltage will come through this error voltage and compensator then it will pass through the DAC. So that means the output of this DAC; so, this is my output of DAC, the output of DAC. So, we are assuming that the output of a DAC is updated immediately, but practically it is not possible. In that case, it may so, happen that the sampling point and the switching point can vary.

Because in fact, we discussed at the very beginning of this week's lecture when we discussed lecture number 11, the basic sampling mechanism in you know variable frequency and fixed frequency modulation. So, there will be a difference. So, here if we use this, it is an infeasible sampling because you cannot update the reference current immediately at the sampling point. After all, there will be a conversion time and computational time.

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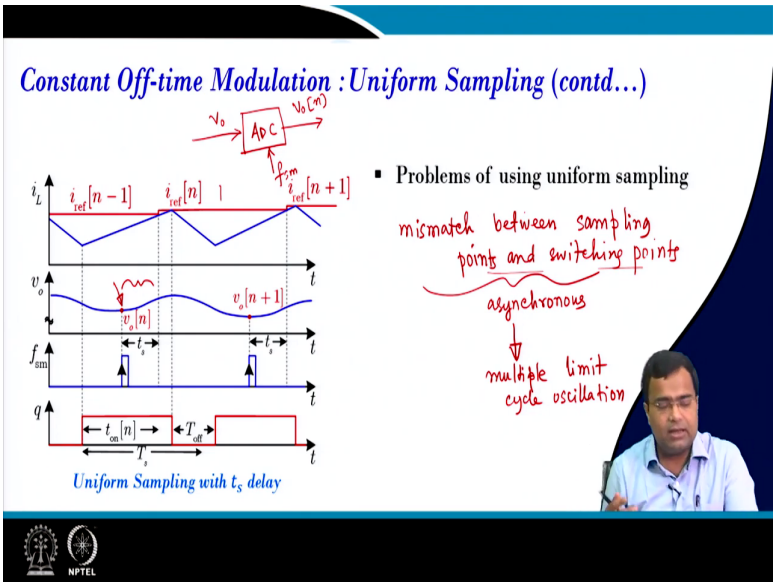

As a result, your practical waveform will look like this; that means, this is your sampling point where you are sending the sampling command. And, we have discussed that if this is your ADC and if you are sensing this output voltage and this is your sample output voltage, I can say v 0 n. So, you require a sampling clock ok. So, you require a sampling clock here.

So, this sampling clock is fixed and here we are providing a delay for accommodating the conversion and computational time, but even at this, it is practically feasible for you can implement. But, you will see because when you go to MATLAB simulation in next week's lecture, we will see this will lead to multi-limit cycle oscillation. Because there will be a mismatch between the sampling point and the switching point because we are using a fixed-frequency sampling clock.

So that means, the sampling point is fixed in every cycle, but the switching time period can slightly vary. And, as a result, you may end up with a mismatch and that will lead to multi-limit cycle oscillation. So that means, the problem is that you can have a mismatch between you know between the sampling point and the switching point. And, this is asynchronous, they are asynchronous, they are not sync asynchronous and that will lead to what is known as multiple limit cycle oscillation; multiple limit cycle oscillation.

And, we will see in the subsequent lecture when you go to MATLAB simulation ok. So, multiple limit cycle oscillation; that means, is one of the drawbacks. But, if you increase this sampling rate, you may reduce this effect mismatch, but still, you may not eliminate this

problem. But, the problem will be if you use a very high sampling rate then your you know ADC power consumption will increase and your computation, that because you need to update this reference current much more frequently.

So, you know the computational you know requirement or the power consumption will increase. So, as a result, it may incur more losses.

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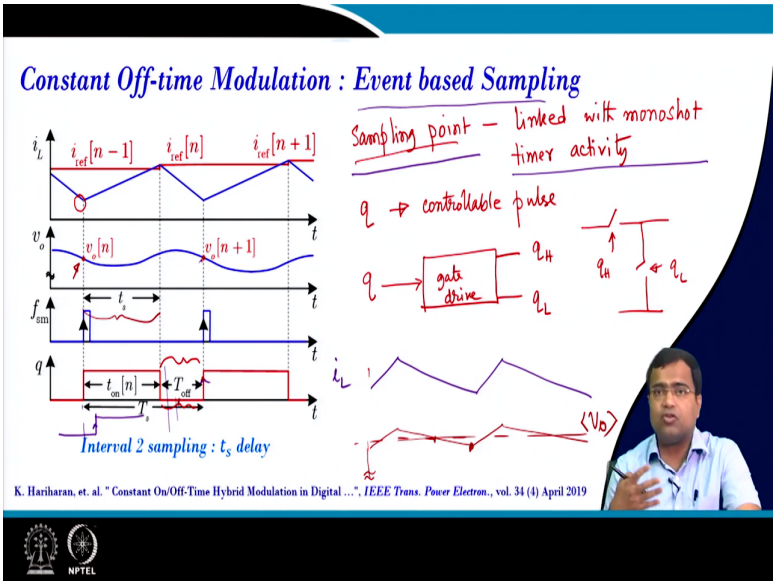

So, to overcome that we can use instead of uniform sampling, we can use an even base sampling. How do you do that? So, you take an event for example, here since it is a constant off-time control. So, constant off-time means it will enable a monoshot timer and for this particular duration, your monoshot timer will be will set at the active height, because that is the monoshot timer it is in an unstable state. So, it will remain high for that particular duration then it will come back to a 0 state.

So, when the monoshot timer is about to finish the counting; that means when it just finishes the counting; that means, this edge we can take a sample ok; that means, it is concerning an event. And what is the event? Whenever the monoshot timer finishes counting then we will sample the output voltage. So that means, the first thing conceptually; that means, that sampling point is a first logic, sampling point linked with monoshot timer activity.

Why I am saying activity? Here I am taking the sample when the monoshot timer finishes its time counting. I can also select the sampling point when the monoshot timer is just enabled or

I can select the sampling point in between anywhere in the monoshot timer. So that means, we are linking the sampling point with the activity of the monoshot timer so; which means, it is an event.

So, we are not talking about any fixed frequency clock and whenever the monoshot timer is activated, then we have the freedom to select the point anywhere between the timer.

Now, you can ask me what will happen if you sample right at this point. So, if you sample right at this point then the problem is you may end up with the noise because; this can be a noisy point ok. So, you have to be careful because whenever the switch will turn on, there can be a spike, switching spike; so, you need to avoid it. One way to avoid you know whenever you identify the monoshot timer finishes its counting.

This is your q pulse; that means, I am saying the q pulse is the gate; it is a controllable gate signal, a controllable pulse. And, when this q signal goes to the gate drive, you know there will be a gate drive right gate drive then the gate drive will generate the high pulse and the low pulse for the respective synchronous switches. Because we have two switches right, one switch is here and another switch is here if you take a buck converter.

So, let us say it is a high pulse and it is a low pulse and if you are talking about a practical switch there will be a finite turn on turn off time. And, to avoid any shoot through then we need to provide some delay or dead time, and also the driver will also have some propagation delay. So, as a result the actual; that means if q is here the actual q l; that means if you take the actual q l if you take the actual q l. So, actual q l can be, it can go high somewhere here; that means, it can go high.

So, there can be some delay due to the driver or there can be some delay due to avoid; that means, due to the dead time. So, as a result, even if you send the sampling command right at you know whenever the monoshot timer finishes its counting, this is good enough because practically the switch cannot be turned on at this point, because there will be some delay. So, as a result, we will be able to capture a clean sample.

But, the bottom line is this we are linking the sampling point concerning the activity of the timer, as a result, it is called event-based sampling. And, we have discussed in sufficient detail what will be the impact on stability if you keep on changing the sampling point; that

means, if we take a sample either here or here or here, based on that there will be various possibilities because you know one thing is a regulation.

Suppose, if you take the sample here which may be at the end of the off cycle then if you take you to know ESR-dominated ripple. Suppose, if you are talking about the output voltage ripple of a buck converter, if the output voltage ripple let us say is primarily dominated by the ESR of the capacitor, then the ESR ripple profile will be identical to the inductor ripple profile in a synchronous buck converter.

So, as a result, this is my inductor current, if this is my inductor current profile then if I take if I talk about the output voltage profile the output voltage will also have a similar kind of profile here and I am talking about this output voltage. So, this is my reference, this is my average output voltage, and this is my average value. So, this will also have.

Now, if we take the sample right here, we are talking about the sample close to the valley point of the voltage and if you regulate the voltage what will happen is your actual average output voltage will be slightly higher than v ref so, so that may lead to some kind of penalty in the regulation. So, to avoid that you may choose a sampling point at the midpoint; so, that you know you can sample somewhat close and you can achieve better regulation.

So, all these possibilities exist in this and we have discussed some of the detail in this paper. So, the bottom line is that here we are talking about event-based sampling.

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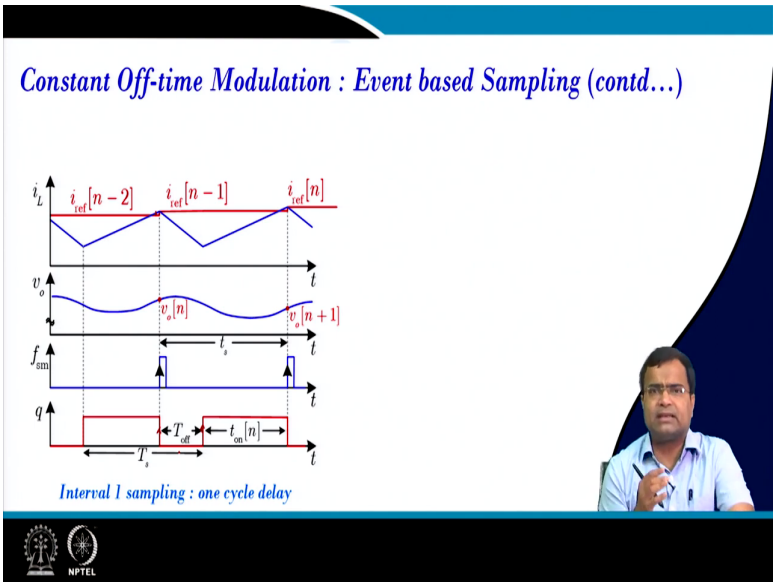

Now so, in earlier event-based sampling there is a delay because while we take the sample at this point, we are updating the reference current somewhat later and this is to accommodate our ADC conversion as well as controller computation time. So, as a result, this will provide some you know headroom for this conversion. So, it is a practical converter.

But, suppose you use a software control architecture, or if you are using a slower A to D converter with a slower conversion time you may take a full cycle delay; that means, you take the sample, and you know you can take the sample again at this point. There is no issue and you can update the next cycle or you can take the sample just where before the switch turns on, because you are trying to sync the activity with the timer monoshot timer.

When the monoshot timer enables then you can take the sample and then you can take the action in the next cycle. So, this is something of a one-cycle delay. So, this may potentially provide more headroom for you know I will say the conversion and computational time. But, we will discuss when we will go for analysis at least one case study will show what is the effect of sampling delay in the stability.

So, you will find because there will be cycle-by-cycle stability we have to ensure; that means, we do not want any subharmonic instability. So, to avoid any subharmonic instability, we need to find out some gain, controller gain, proportional and integral gain and this gain range of this gain will depend on the sampling delay. So, if you take a larger delay, you may end up with a lower smaller range of controller gain for stable behavior.

So, it will give rise to a conservative choice, a set of controller gains. So, that will be the penalty that we will discuss. So that means, we may if we incorporate delay first of all it will penalize because this delay will be introduced in your loop. So, it will naturally slow down the transient performance because of this whole cycle delay, but as I said digital control has other provisions and alternative paths to speed up the transient.

But, in effect at a steady state this delay if we increase the gain may also end up with sub-harmonic oscillation. So, some part we will discuss some in the stability analysis aspect, but not too much because you know this course, we do not want to make too much advance. We should know the basic concept first.

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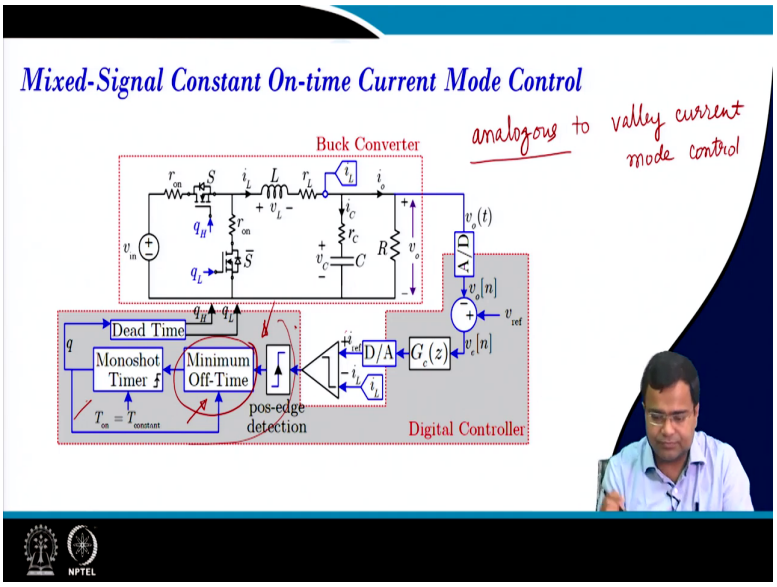

Now, if you are going for a mixed signal on-time control and we know this control is analogous, it is analogous to valley current mode control, valley current mode control; where we are directly controlling the valley current and the reference current will be the value of the inductor current. So, when the inductor current hit the lower limit; so, we are going to the waveform.

So, it is exactly analogous to valley current mode control in fixed frequency and the difference here in valley current mode control for fixed frequency operation, we keep the time period fixed, but here we are keeping the one-time fix. But, you see everything else is the same; that means, you know what is the change here? Only this timer value is updated with the minimum time.

If you go back to the previous diagram if you see what is the change? Maybe this terminal even you do not have to change this because you can accordingly take care in this block diagram. So, here you see there is a monoshot timer, there is a time and the edge whether it is a positive edge or negative edge that you can always change inside the digital block, it is not a big deal. And, the dead time also we will have because when we learn HDL coding, we will synthesize this whole thing in a Verilog code.

But, here the difference is you can see the comparator again analog comparator. So, you may not need to change the polarity of the terminal, or; that means, you do not need to physically change the terminal of the comparator. You can keep it as it is, but you have to take care of

that action in this digital block. So, here again, you need a constant off time minimum off-time block. There is a small timer and another monoshot timer.

So, all these blocks are common, only some functionality of these digital blocks will be different and that can be taken care of just inside the digital block without fundamentally changing anything.

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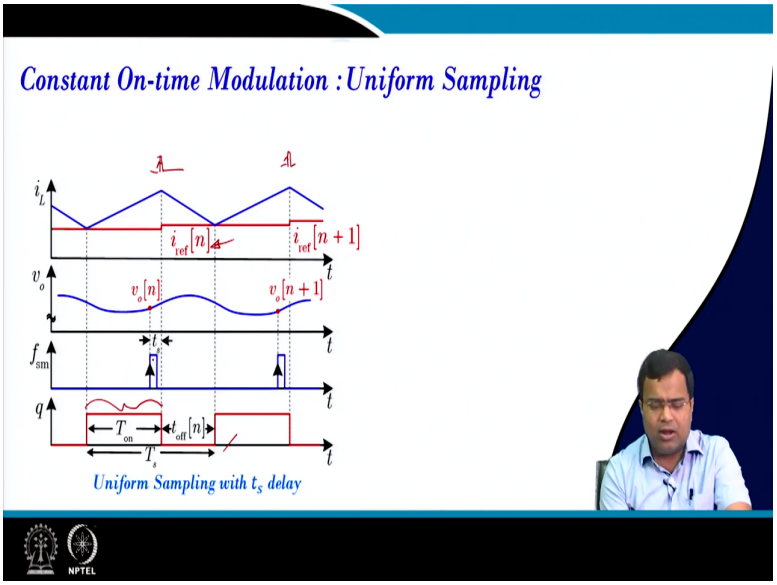

So, here it is analogous to valley current mode control. What does it look like? You know valley current mode control means generally we know whenever in fixed frequency the clock edge comes, we turn off the switch and when this the inductor hit the lower limit then the switch is again turned on. So, in fixed frequency, it is linked with the clock, but here there is no fixed frequency clock because it is a constant on time. So, how does it work?

So, first, if the monoshot timer is enabled. So, it is enabled for this T on duration, once it is disabled then the switch is turned off, and when the switch is turned off the inductor current starts falling. And, when the inductor current hit the lower limit that is my valley reference that again the switch turns on or basically, it will trigger the monoshot timer and the monoshot timer goes high. So, that is how this operation and we have discussed it in sufficient detail.

But, in the digital architecture only the voltage loop is digital, everything else is analog. Here is how to sample. Again, if we use the uniform sampling that we discuss; so, what will

happen is there will be a mismatch between the sampling point and the switching point. And, it will again lead to multi-limit cycle oscillation and we want to show a MATLAB case study for this particular example also.

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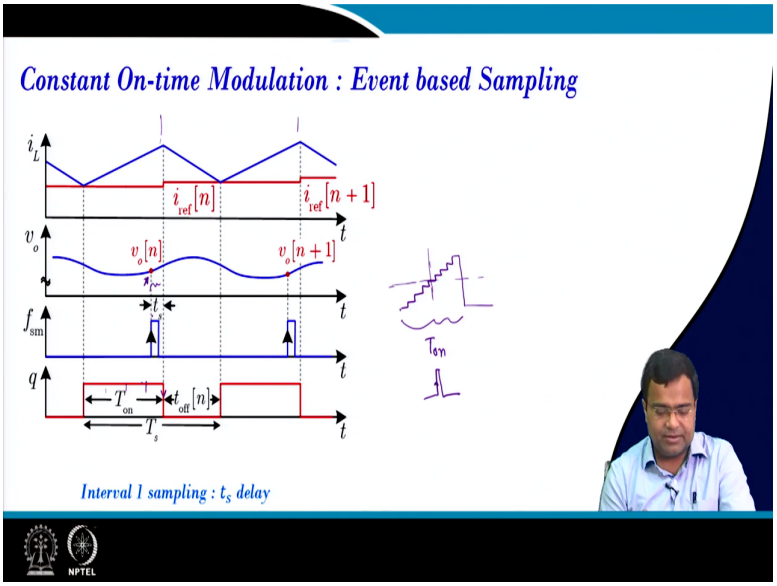

So, we have identified that a constant on-time dilation even by uniform sampling will maybe to you know multiple limit cycle oscillation. So, then again similar to constant off time, we can now do event-based sampling. So, how do you do that? So, here you know it is a constant on-time modulation which is a variable frequency like a valley current mode control, where we need to identify if you think there whenever the monoshot timer finishes are counting then the switch is turned off and the inductor current starts falling.

And, whenever the inductor current reaches the reference current which is the valley current, then again the monoshot timer is activated and the switch is turned on. And, it remains to continue to remain on for the on-time duration when the monoshot timer is activated. As, we have discussed in the previous lecture under constant off time; means, here in the event-based means we want to link the sampling point concerning the activity of the monoshot timer.

So, here we want to take the sample a little bit earlier than the monoshot timer finishes counting because we can choose any point in this duration; because we can because this counter is a counter right. And, it will start counting like you know if you take a just simple counter. So, the counter will just simply start counting and once it reaches then it goes low. So, this is let us say this is your T on duration right?

So, if we fix a comparator here so; that means, you can create a clock whenever it goes midway then you can activate this clock. So, this can be used as the sampling clock; so, either midpoint or anywhere in this point because it is ultimately a counter. Now, if you send the sampling command here then you can update the current difference after some time and this is to accommodate the delay due to the ADC conversion as well as controller computation.

Although in this diagram, the delay seems to be very small, we can always increase the delay amount right or even you can take a full cycle delay that we have discussed. So, all these possibilities are there and it is for the conceptual understanding that we need to introduce a delay to accommodate conversion as a computational type, but it is ultimately event-based sampling ok.

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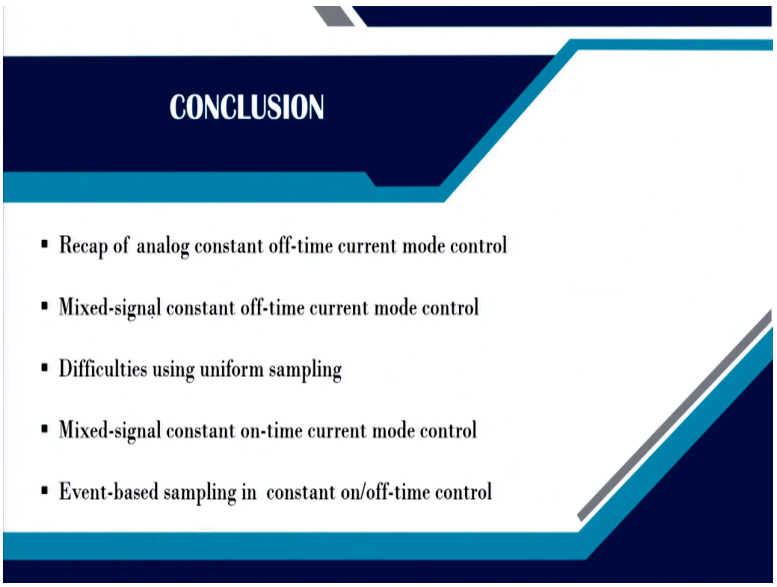

So, in summary, we have a recapitulate analog constant off-time current mode control, we started with this. Then we discussed mixed signal constant off-time current mode control, then we understood what are the difficulties of using uniform sampling. Then we have also seen the constant on-time current mode control mixed-signal architecture and finally, we have also discussed event-based sampling in constant on-off-time control.

So, we got some reasonable idea about how this kind of control logic operates. So, then we will discuss a little bit about the architectural aspect in the next lecture. So, we want to finish here today.

Thank you very much.