Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 02
Fixed and Variable Frequency Digital Control Architectures
Lecture - 15
Overview of Fixed Frequency Current Mode Control Architectures

Welcome. In this lecture, we want to summarize what we have learned in the previous class. So, we want to give an Overview of Various Fixed Frequency Current Mode Control Architectures.

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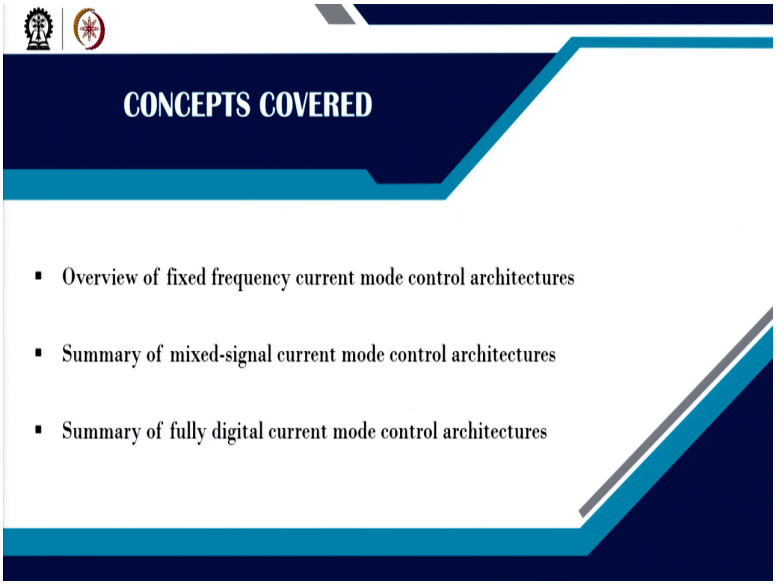

So, we will give an overview of fixed frequency current mode control architecture, we will summarize various mixed-signal control current mode control as well as fully digital current mode control.

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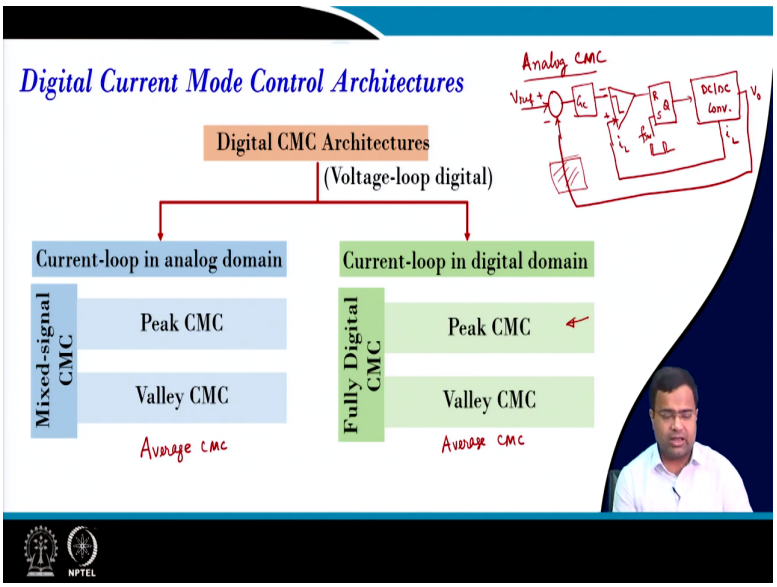

So, if we go for digital current mode control because, it is a two-loop control where, we are considering; that means, you know if you take analog I will say analog current mode control where we have this V ref. Then you know there will be v 0, there will be a controller, then the controller will go to a comparator and this is my inductor current. So, then it will go to an RS latch. So, I am talking about peak current mode control. So, this is my switching clock and then it goes to my DC-DC converter.

So, this comparator as long as the inductor current is if inductor current crosses this it will be plus it will be minus and we are taking the inductor current sense from here, and then we are taking the output voltage here. So, this is my output voltage, this is my inductor. So, it is a two-loop control. We have an inner current loop and the outer voltage loop.

Now, in this control when you go for digital control, we are taking all the time the digital loop voltage loop is digital. So, that is the voltage loop in digital. Now the architecture will differ based on whether the current loop is in analog or digital. So, first is the current loop in analog, where you can have a peak current mode control, and valley current mode control and we have also discussed that we can also have average current mode control; average current mode control architecture.

In the digital, so this is a mixed signal implementation where the current loop in analog, and we can retain the first dynamics of the current loop. Now if you go to fully digital then your current loop is in the digital domain. Where you can also have peak current mode control as we have discussed, valley current mode control and we can also have average current mode

control here, but we have not demonstrated this in this course because these are somewhat advanced topics.

So, one can if some understanding of digital control is developed, then one can try to search the literature, research papers, or maybe some commercial product. So, this is called fully digital current mode control where both the current and voltage loop are digital domain and the mixed signal voltage loop is already in the digital. So, the current loop in analog.

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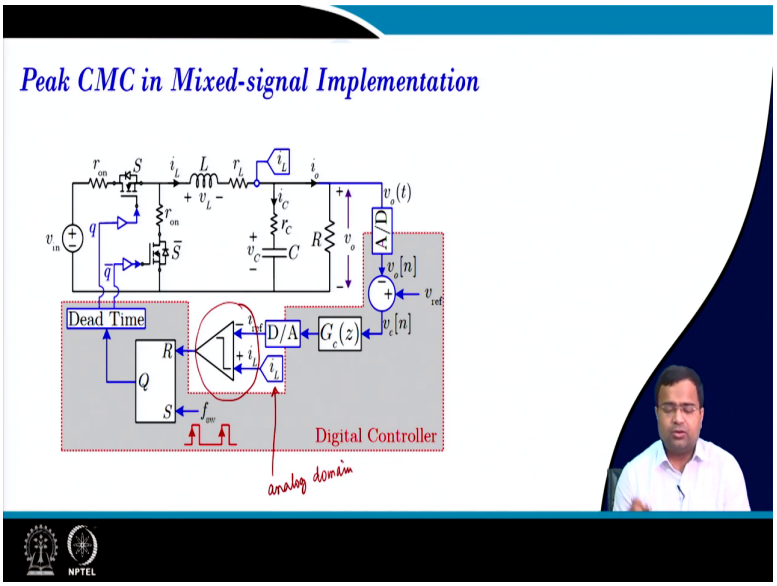

And we already know about the architecture, this is like your analog comparator and this is a sense current in the analog domain in the analog domain and your voltage in the digital domain. So, we know about all this architecture.

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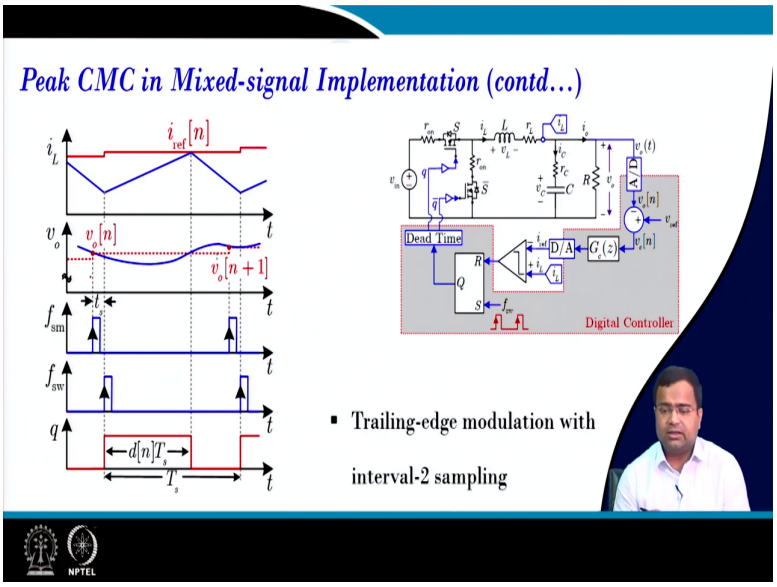

And we know about the control waveform; that means, we will here we are talking about the peak current mode control and interval-2 sampling that we have discussed in the previous lecture.

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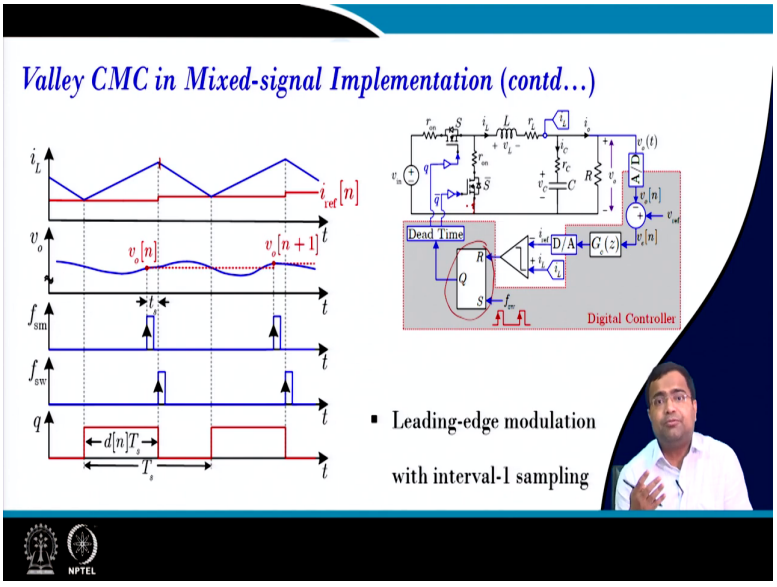

And valley current mode control also in mixed signal implementation we have discussed that, if you just turn on the switch turn off the switch at the rising edge of the switching clock, and then the switch will turn off when the inductor current will touch the valley current and by

that process, it will continue and it is under leading edge modulation with interval one sample.

And we know we have also discussed that if you remove this R S latch and represent using you know the configurable algorithm digital algorithm, the same hardware can be used for peak as well as valley current mode control. Because if you want to go for wide duty ratio operation may be one can you know go from peak to valley, but for that purpose, we need to sense the full current.

But, in many implementations actually, the current is sensed like only the high-side current is sensed. So, in such cases, we can go for only peak current mode control in mixed signal realization. For valley current mode control we need to sense the low side current ok and when you go for variable frequency architecture because valley current mode control if you go for low duty ratio operation then it is inherently unstable for then you need to add you need to consider RAM compensation.

Now, when you go for constant on-time control which is a very popular solution then you will get an inherently stable current loop, but it is also easy to sense in a low side current because you can sense you know through the RDS on of the switch. After all, it is a ground referred or you can put a small resistance in series with you know you can put a small resistance here as a sense resistance and it is a ground referred so you can directly sense.

But, for peak, current mode control implementation you need to you know sense the high side current in the mixed signal. But if it goes to fully digital current mode control even with sensing the low side current because you are taking the sample of the valley current and you emulate the rising slope in the digital domain. So, you can sense the valley current and still can implement peak current mode control if you go for a fully digital current mode control architecture.

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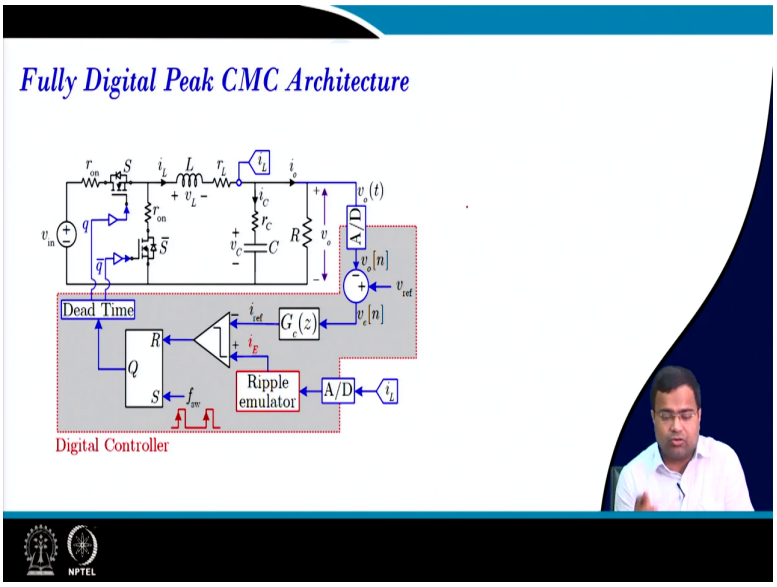

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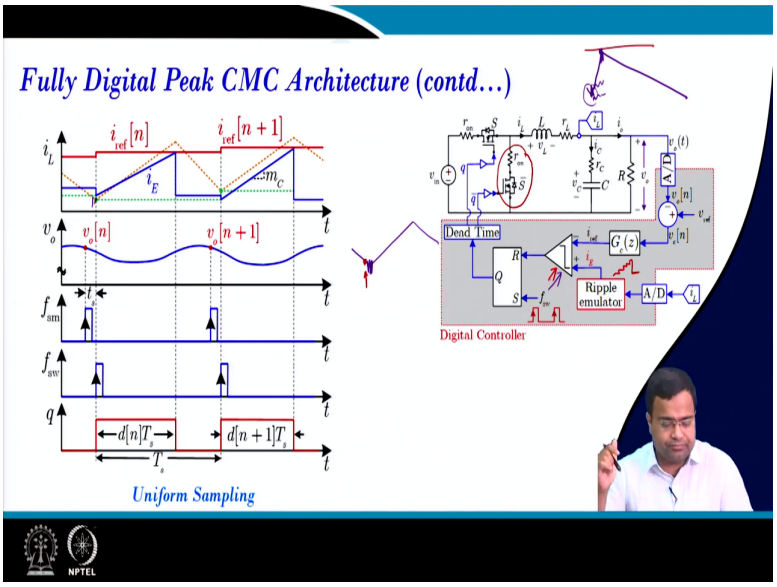

So, in fully digital current mode control architecture if you go for peak current mode you see we are sensing the valley current mode before the switch turns up; that means, you can just take you can sense the low side current mode which is very easy to sense and you can emulate in the digital domain. Another problem can be addressed because there is a one-cycle delay because in peak current mode control you know if you see if you want to implement the peak current mode control for a very low deterioration operation some major difficulties are there.

So, suppose I want to do analog control for example. So, in analog control, the deterioration is very low ok, and suppose you have some spike in the sensor. So, first of all, the current sensor can have some spikes and you have a very low time because of the high frequency. So, you need to blank some time here in analog implementation and this time is so low from the comparator's point of view, it will be very take tough to take a decision.

That is why for low-duty operation in analog controls people go for constant on-time control. Because if you go for valley current mode control you have a longer duration of off time, but it is inherently unstable for low deterioration, and we have discussed in our previous NPTEL course that is our control and tuning method in switch mode power converter.

But, in digital control, since we are taking the valley current here and that is the process for the whole cycle you get a full time and you are comparing in the next cycle using internally to the digital. So, these are digital comparators. A digital comparator means it can be a simple subtractor and you can check the difference by looking at the MSB. So, you do not need a physical comparator it is just a 2 s complement subtractor.

And that can be; that can be very very fast and there is no switching noise because you are taking the sample at the, the. Because I am just talking about this valley current mode control even though there is a noise. So, I am capturing the sample here, I can sample it here before the switch turns on. So, I am getting a clean sample and then I can add RAM right?

So, we can avoid such switching noise since the inside of the controller is noise insensitive, and our digital sawtooth already is very fast because it is a sawtooth and you know you are making the because we have discussed various architecture of RAM you know this emulation RAM right.

So, we have discussed RAM and the component means just a subtractor. So, you can make this operation extremely fast and you can realize peak current mode control even for low deterioration operation. So, that means, when you go to digital control many possibilities which are difficult in analog can be easily realized in digital.

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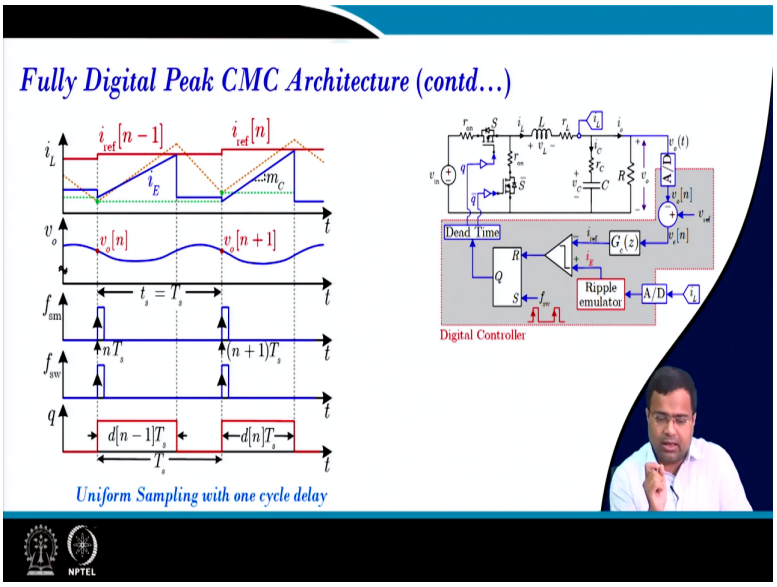

In fully digital if you take one sample delay for the voltage loop also you are taking one sample delay. So, the current is already one sample delay otherwise you cannot make it feasible and voltage also you can delay by one sample and you can also take voltage a little bit earlier. So, there are many things, but we need to be very careful about the stability analysis, because, in this course, it will be very tough to consider all the case studies in the stability.

But, we will show a few ideas or maybe one or two realistic case studies and it will enable you to know the participant in the future to go for you know use the methodology that we will discuss to analyze stability for various possible delay options and how to analyze stability, but one bottom line is this you can implement various digital control architecture peak valley etcetera in this fully digital current mode control.

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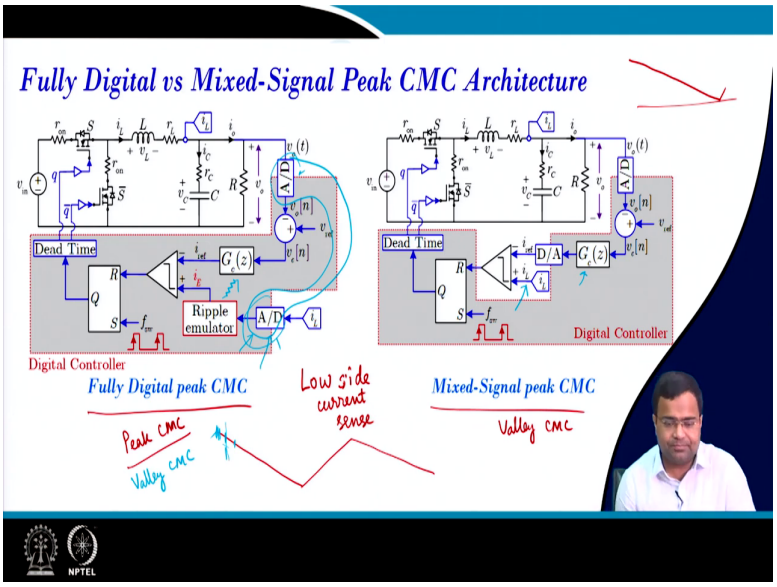

Similarly, if you want to compare the first thing in fully digital; that means, mixed signal. So, if you sense let us say you are only sensing the low side currently, the low side you know I will say low side current sense. So, this is easy for a buck converter because the low side switch is very easy to sense, then in fully digital you can do peak current mode control. But, here it will be valley current mode control because the current loop in analog ok.

And low side current means because it has to compare with the physical current right. So, it will be valley current mode control and you can implement peak current mode control if you go for variable frequency architecture and even you can implement peak valley in the same architecture itself, but we are not going to discuss here in fully digital you can implement peak current mode control.

Now, I may ask can you also do valley current mode control in fully digital why not? You can also sense; that means if you take the low side current that means, I am talking about; I am talking about the low side current this is the inductor current low side current. Now if you can sense may after reasonable this time maybe if you have to provide some delay because you have to avoid this switching point.

Now, you take the sample somewhat closer after that is settled down may give some delay, then you process for the next cycle and implement a valley current mode control. So, it is still possible that using low-side sensing you can go for both peaks as well as valley, valley current mode control, but there will be some delay. So, that you have to take into account. So,

that means, fully digital mode control is flexible and you can also max using a single ADC. These two ADC can be maxed here because we are taking only one sample per cycle.

But, the fully digital control is a quantized current. So, that means, you will have a limit in terms of quantization which has a similar problem in voltage mode control. So, you have a quantizer here, you may have a quantizer because of this you know the ripple emulator and you also have a quantizer of ADC. So, it is very important to match this quantization otherwise it will end up with a lot of instability in this architecture whereas, here you have only analog current.

So, quantization is primarily defined by ADC and your Q factor of this compensator and we will discuss it in a fixed-point implementation.

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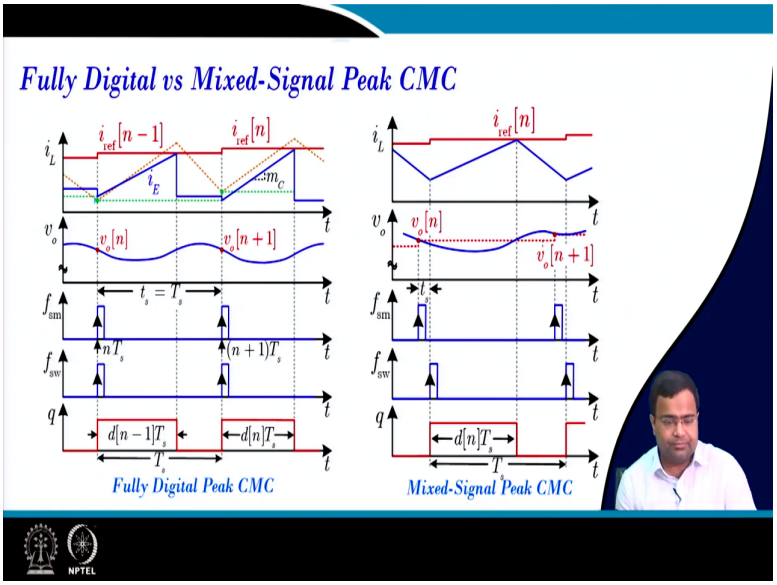

So, we can here we have shown the peak current mode control architecture of fully digital and current mixed signal. Here we need a valley current sensing for peak current mode control implementation. Here we need peak current sensing or high-side current sensing for peak current mode implementation. So, these are the difference. So, you can think of many possible architectures. So, I am just giving you some basic ideas. So, I hope you can take it forward.

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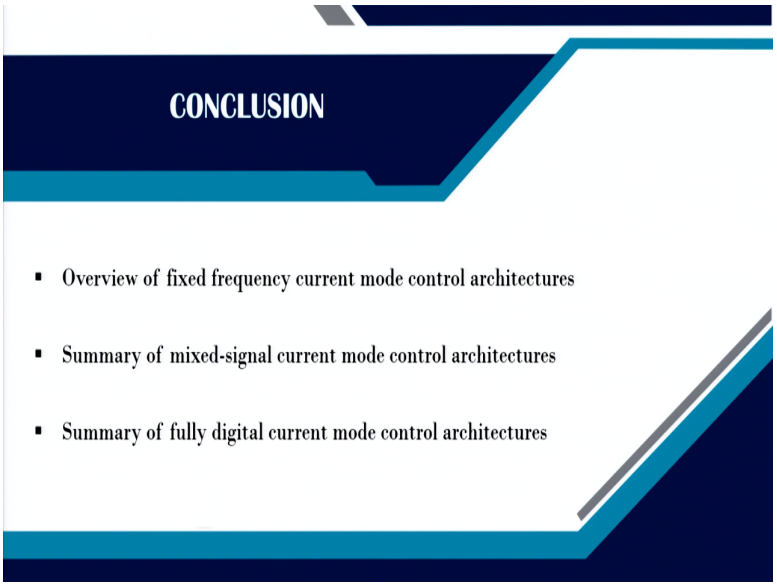

So, in summary, we have discussed various fixed-frequency current mode control architectures. We have summarized mixed signal current mode control and the possibility of various valley and peak architectures. We have also discussed some fully digital current mode control architecture and we have shown that even using sensing either side current you can implement both peaks as well as valley current mode control and we need to also simulate and model this.

So, we will implement you know at least fully digital and peak current mixed signal current mode control using MATLAB simulation. So, we will realize how to implement this control logic, and then you can think of a more advanced control algorithm for your further study. So, with this, I want to summarize here.

Thank you very much.