Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 02
Fixed and Variable Frequency Digital Control Architectures
Lecture - 14
Sampling Methods under Fixed Frequency Current Mode Control

Welcome. So, in this lecture, we are going to talk about Sampling Methods under Fixed Frequency Current Mode Control.

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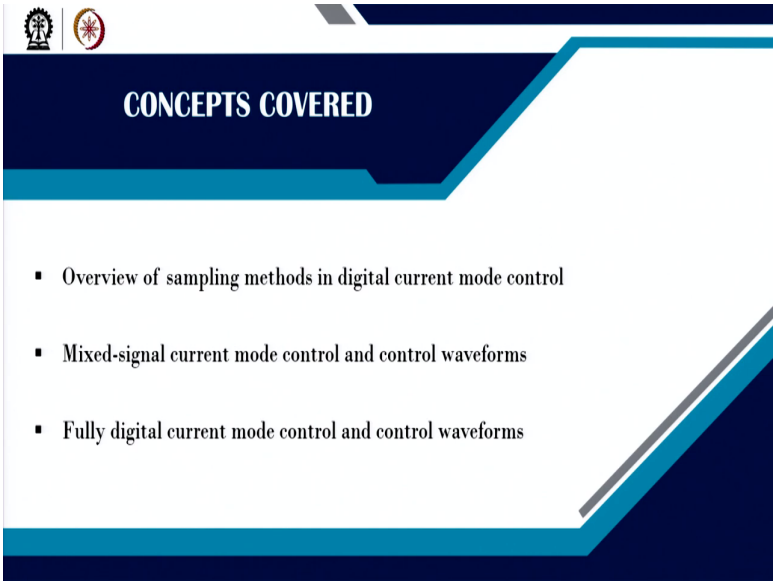

So, here you know we have already discussed in the previous lecture the digitization method for multi-loop control. So, we have some basic ideas. So, we will talk about the overview of the sampling method in digital current mode control. Then we will talk about mixed signal current mode control and the waveform, then fully digital current mode control and the control waveform.

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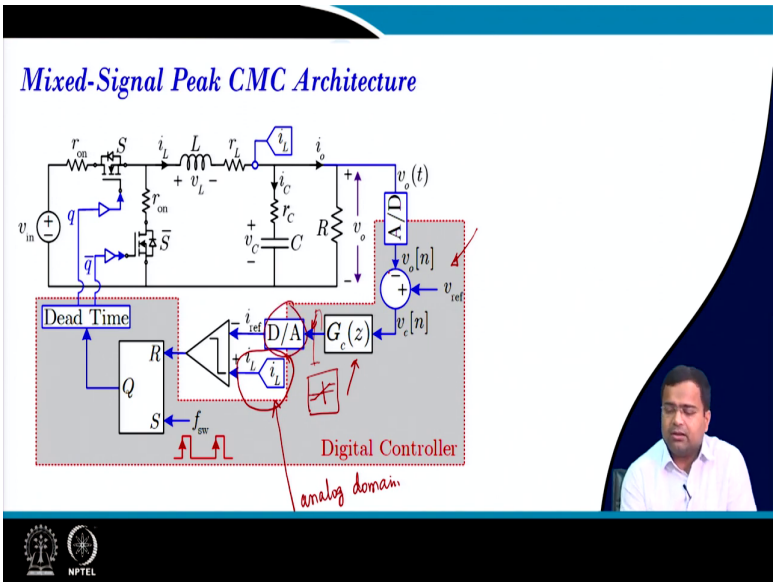

So, first, we will talk about mixed signal peak current mode control. When you say mixed signal we have discussed that current inductor current sense will be sense inductor current in the analog domain. So, this is in the analog domain whereas; the voltage loop is in the digital domain. So, this is in the digital domain.

And we have discussed this and in fact, we will see as we move forward because of the digital domain we can tune the controller. We can program this reference current because we can put a maxing operation. So, either we can pass the controller output or we can set some non-linear value thresholding of the current in terms of the protection circuit. We can easily put you know saturation block here like this kind of saturation block you can easily incorporate by this digital function ok algorithm.

And we can also do some trajectory-based control because the current will simply follow it. So, that means, there are many advantages to keeping the digital loop that voltage loop in the digital domain, but the keeping current loop in the analog domain. So, in this architecture, since the current is an analog we need a D to-A converter and here voltage already has an A to-D converter.

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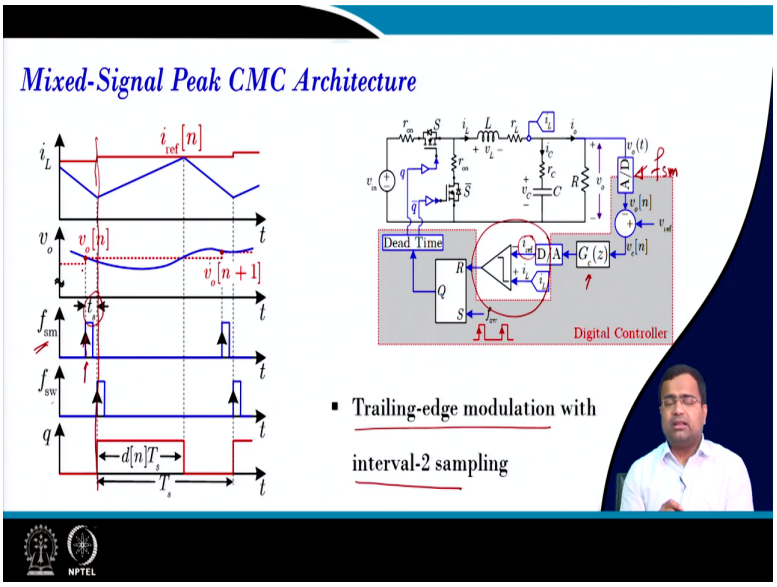

Now, how does it work? So, if you take the control waveform as usual we need some time for conversion from A to D as well as the computational time. So, naturally, our sampling clock is used here. So, here we are using a sampling clock s f sm. This is in synchronism with the switching clock part with a time delay. So, the sampling edge will come fast.

So, that will send a comment to the ADC that we need a sample at this point, but the data will be available an after sometime because there will be A to D conversion time followed by the controller computation time. So, your peak reference current is the output of the DAC and it is the output of the digital controller followed by a DAC that will also be ready at this time because this is a peak reference current you see it is ready.

When it is ready then we start the switching operation. So, we have to select this edge in such a way we get sufficient time. In this case, we talking about t s which include conversion time and computation time in such a way that data should be ready the controller output should be ready at the point of switching clock when it is in appear because we are talking about trailing edge modulation which is nothing but the peak current mode control.

The rest of the process once you generate the peak reference current is the same as analog peak current mode control because you see this R S, and Q are already digital and the output of the component is also digital. So, the only analog part is the current sensor, and you know the analog comparator and you need a D to A converter for converting the controller output to generate the reference current.

So, this is called trailing edge modulation because it is peak current mode control is well known, but it is also called interval to sampling because we are taking sampling at the falling edge of the voltage; that means when the switch is off.

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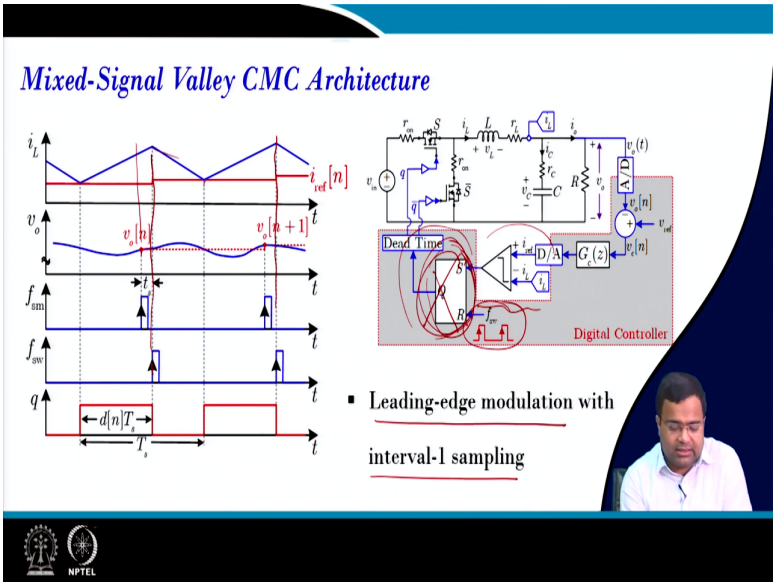

Now, in mixed-signal current mode control, you can also have a valley current mode architecture because this is a leading-edge architecture. Where know basic you know fundamental block algorithm is known because in the leading edge when the switching frequency clock comes the switch turns off and switch turns on when the inductor current hit the valley current and then again it will continue to turn on until the next clock comes. So, the next clock comes here.

Again in this method, we have to generate the valley current reference current and interestingly in digital control you can easily reconfigure this block and this block in such a way that you can the same architecture can be used for both peak current mode as well as valley current mode control because you need to only change this block to represent you do not need to change the terminal of the comparator. After all, that can be easy. So, you have to sink the reference current can be used as a valley or a peak only you have to change the algorithm as well as the modulation mechanism.

So, what will be the clock and this R S flip-flop will replace it? So, here whenever the switching clock will come that is the bottom line, the switch will be turned off and when it will hit the lower limit the switch will again turn on. So, this algorithm of this latch circuit as

well as this clocking you can easily reconfigure in digital control. So, you can use the same mixed signal architecture for peak as well as valley.

Here again, you have to take the sample a little bit earlier than your actual switching clock comes because you need to provide time for sampling as a conversion time of the ADC as well as a computational time, and since the sample is captured during the on time. So, this is known as it is of course, we are told it is a leading-edge modulation and it is known as interval one sampling because we are taking during the on the state of the switch ok.

So, we can use the same hardware, but not this block a replacement of this block then will represent the valley current mode. Here we are using that you know this architecture is dedicatedly used for the valley, but if am saying if you want to use a generic peak or valley. So, you simply change this algorithm and the clock then you can use the same architecture for peak as well as valley.

So, if you can implement peak and valley then what is wrong with the average current mode control?

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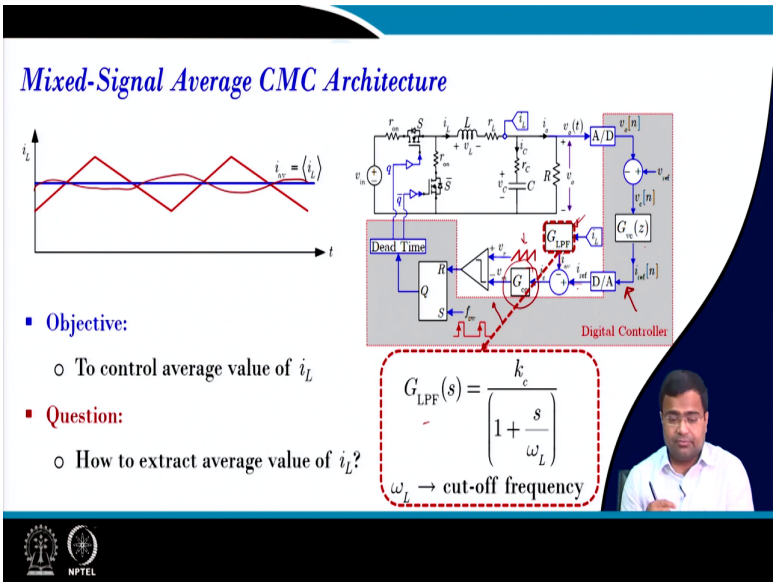

Yes, you can do that. So, in average current mode control, we are only showing the averaging technique in the analog domain, but there are many advanced architectures in digital, which easily can do average current mode control in fully digital. But in analog you know traditionally since we are sensing inductor current, we can pass through a low pass filter to

extract the average value then it is compared to the reference, and the reference is giving the average current.

So, this is like for example, if you take a LED driver or PFC. So your average inductor current has to follow your reference trajectory. So, this reference trajectory can be generated from here either there can be a controller or you can have just a current difference for you know for constant battery charging application and so on. Then the average current output error; that means, the reference current minus the average inductor current that error will pass through a pi controller. So, you want to minimize the steady-state error.

So, the average value should track the reference, and the rest of the logic you know there has to be a sawtooth waveform. Also, you can generate your knowledge through a digital controller if you go for full digital implementation, but in analog, you can keep it. So, here you can change the reference command from the digital very effectively you know, or if required you can also close the loop. So, that means this is the same method we adopted for average current mode control in analog control, the only difference is the voltage loop in digital.

If you go for analog the low-pass frequency filter how do select the cutoff frequency because we need to extract the average? So, you may not get the ideal average. So, you need to get something like this kind of averaging. Because if you extract if you do the Fourier series analysis of the inductor current you will get the DC component, then you will get the fundamental harmonic.

So, if you cannot eliminate the entire fundamental harmonics there will be some amount of things because you cannot have a low pass filter bandwidth of almost 0, then your current loop bandwidth will be extremely low. So, you need to provide some amount of ripple permissible ripple. So, you can extend a little bit about the current loop bandwidth by extending the low-pass filter bandwidth. Once you extend the objective is to control the average current to track the reference current.

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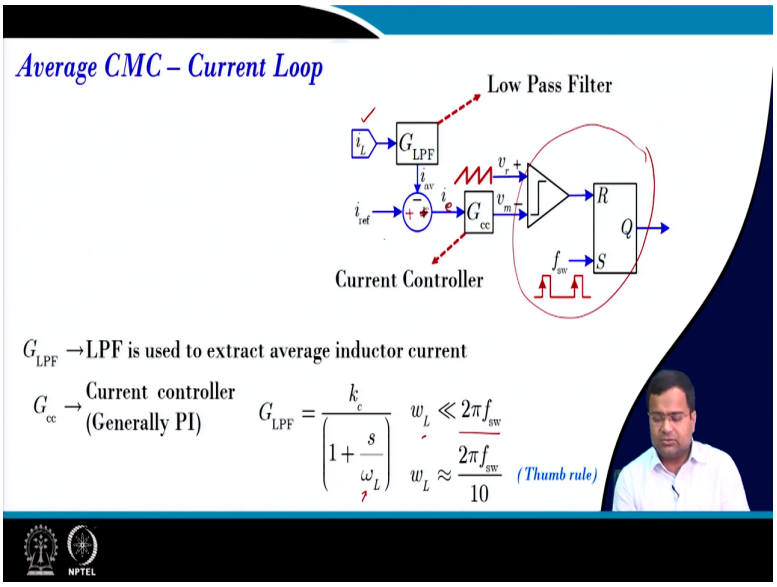

And how to do that, we know that the inductor current sense can pass through a low pass filter then it is subtracted from the reference. So, this should be reference subtraction and this is the error current here it passes through a current controller and is compared to a sawtooth waveform, and then it will generate the, and this is a modulator block PWM modulator trailing modulated.

And then the current controller low passes filter typical thumb rule is that the low pass filter bandwidth; that means, generally you know this low pass filter is one-tenth of the switching frequency it should be much lower than the switching frequency. So, one-tenth is a good thumb rule you know is a good choice.

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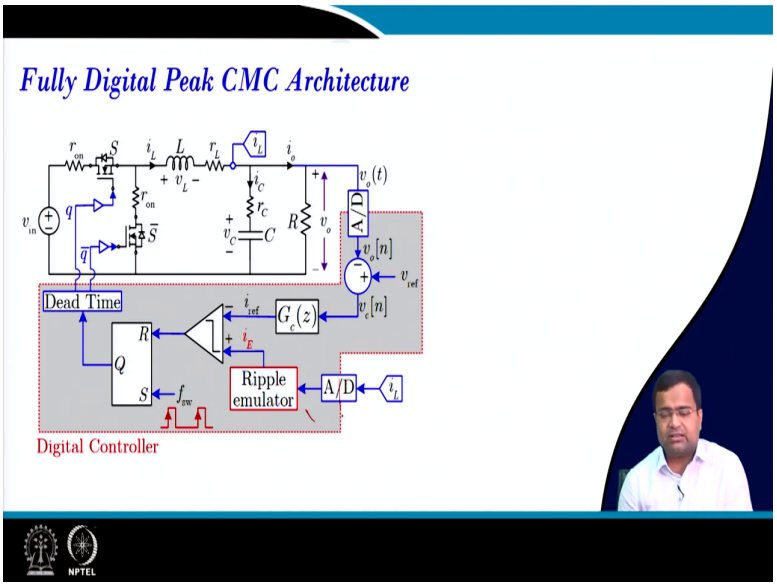

So, now if you go to a fully digital current mode control architecture, then we are keeping the digital currency in the digital loop. And we have discussed the method of digitization either we can use high sampling of the current or we can you can use our emulated ripple so that you can get more or less the current waveform at least we can retain some information about the ripple.

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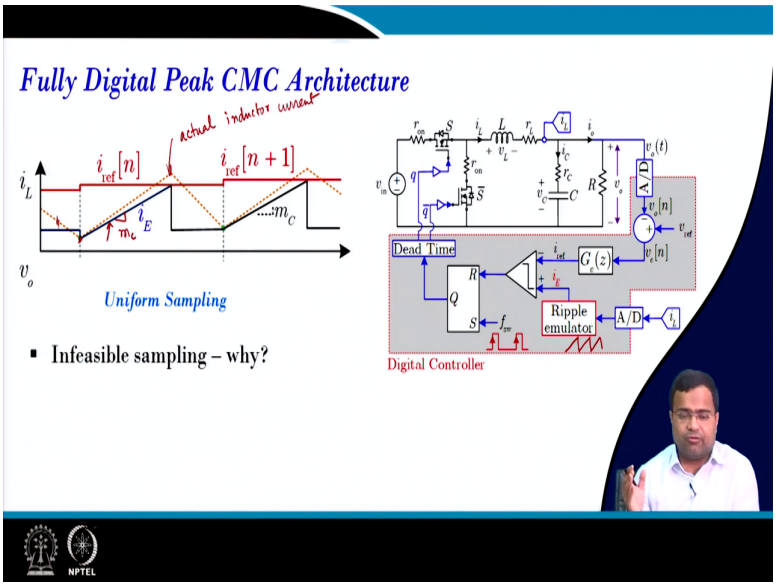

So, how does it work? So, if you take one sample let us have this waveform suppose this dotted line is the actual inductor current actual or maybe the sense inductor current you can

say analog inductor current. Suppose you have sensed more or less the same inductor current now you see at the very beginning of the turn-on time when the switch is about to turn on, you sample the current than with the sample current you add this slope.

So, this is m c which is nothing but the slope of this emulator; that means, in this emulator, we add this kind of ramp kind of characteristics.

So, which is like a staircase ramp, and this ramp will be added with the sample current, but you do not know if this slope can be exactly the rising source of the current or if it may be different. And there are many papers on this because it is very difficult to get the exact inductor slope and even if you do that you know first a scale stability point of view there can be an issue. So, we will discuss some aspects of current loop stability with only an open current loop when you go to the stability analysis and the modeling technique.

But, here I want to show that fully digital current mode control you are taking the sample current and adding that emulated ramp which is a ripple emulator, but this is practically not possible to implement why? Because when you take the sample of the current you cannot immediately use it because ADC will have some conversion time and computational time, but we still need the valley current because we need to add the slope. So, we cannot take the earlier case take the sample here and add it then it will not be a valley current right?

So, we need a valley current information, but we cannot process it immediately. So, what is the solution? So, the natural choice is you give one sign case cycle delay; that means, you capture the current sample here, but you use it in the next cycle so, that you can get sufficient time for the conversion.

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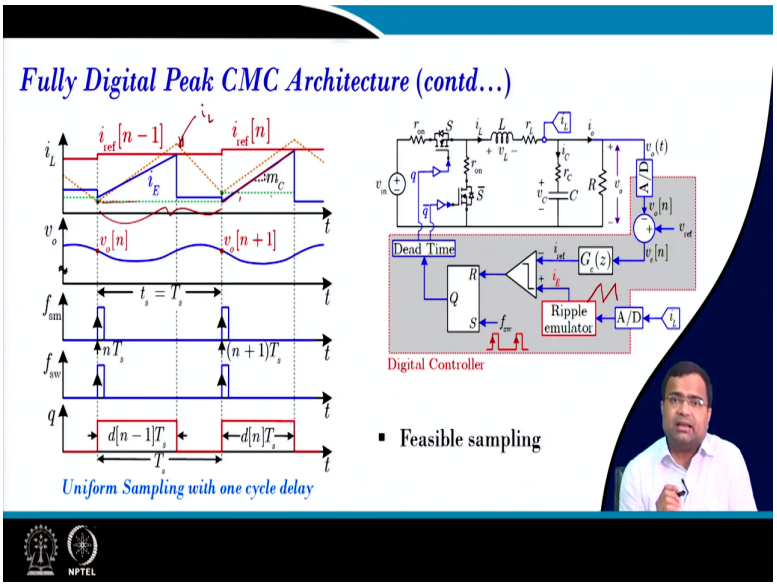

And that is the practically feasible implementation where you see the dotted line again is your inductor current this is your inductor current and you are capturing the inductor current waveform here. So, the green one is the sample value of the inductor current, but you are adding this sample current.

So, this is extended this waveform is taken here and you have added a ramp here sawtooth. And this is like an as I told so, this will add like a sawtooth waveform. So, you are adding this ramp in the next cycle with the sample value so, that you will get sufficient time for the conversion of this ADC because you want to retain the valley current information.

Similarly, if you capture the inductor current where it will be used in the next cycle. So, in that way, you will implement and I will show you when you analyze the current loop stability because of this one sample delay even if we use you know the same slope of the current mode control it will not be stable. So, that means, your emulated slope has to be larger than the slope of the actual inductor rising slope otherwise your current loop will be unstable because of this one sample one cycle delay and will analyze this in the modeling and the stability analysis I think it will be in week 4 or week 5.

But, we will discuss this stability in the current loop stability analysis for fully digital current mode control using one sample delay. So, our objective is that we cannot even choose m c, which is the same as m one then it will be inherently unstable the current loop ok so, but it is a feasible sampling because of one cycle delay and we have to suitably select the m c.

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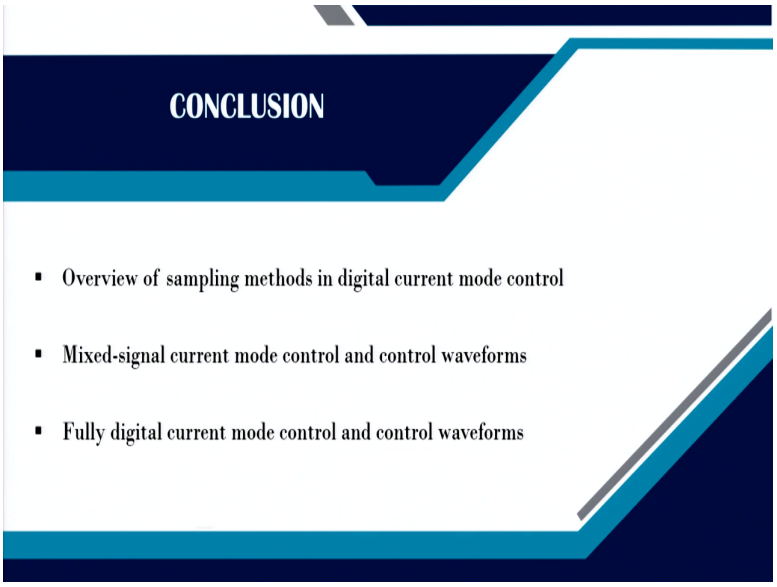

So, in summary, we have discussed an overview of the sampling method in digital current mode control.

We have discussed mixed signal current mode control and different control waveforms, we have discussed fully digital current mode control initially we started with like the same point sampling and use, but it was practically not possible then we used one cycle delay and we implemented fully digital current mode control waveform. So, I hope we got a reasonably good idea about fixed frequency digital current mode control architecture and we want to summarize this architecture in the next presentation.

Thank you very much.