Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 02
Fixed and Variable Frequency Digital Control Architectures
Lecture - 13
Overview of Digital Pulse Width Modulator Architectures

Welcome. So, in this lecture, we are going to talk about the Overview of Digital Pulse Width Modulator Architecture.

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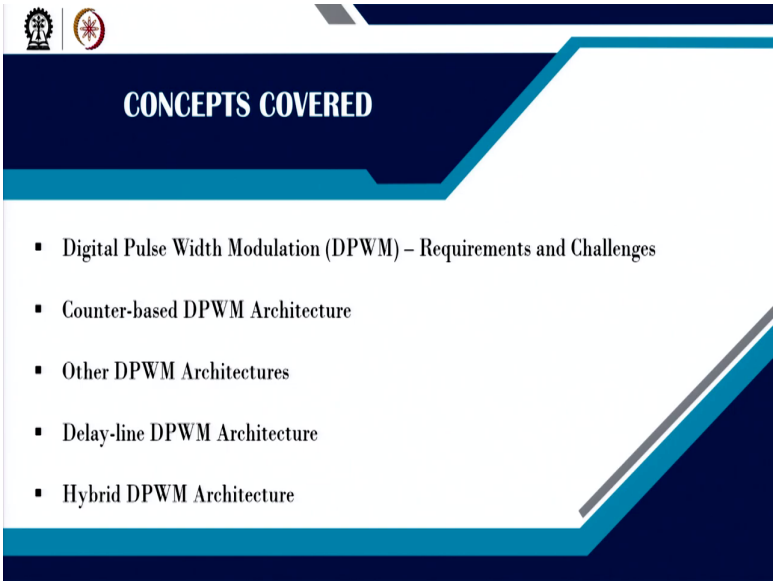

So, first, we will talk about Digital Pulse Width Modulation, their requirement, and the challenges of the counter-based DPWM architecture, and other DPWM architecture which will include delay-line DPWM as well as hybrid DPWM architecture.

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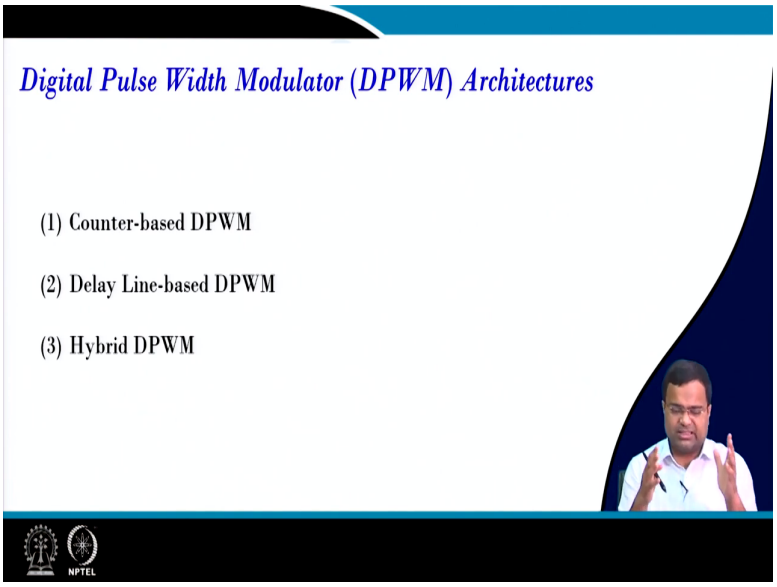

So, first, we want to talk about the digital pulse width modulator. So, here we will summarize the three different architectures, but first, we will go over the basic counter-based DPWM and how it works.

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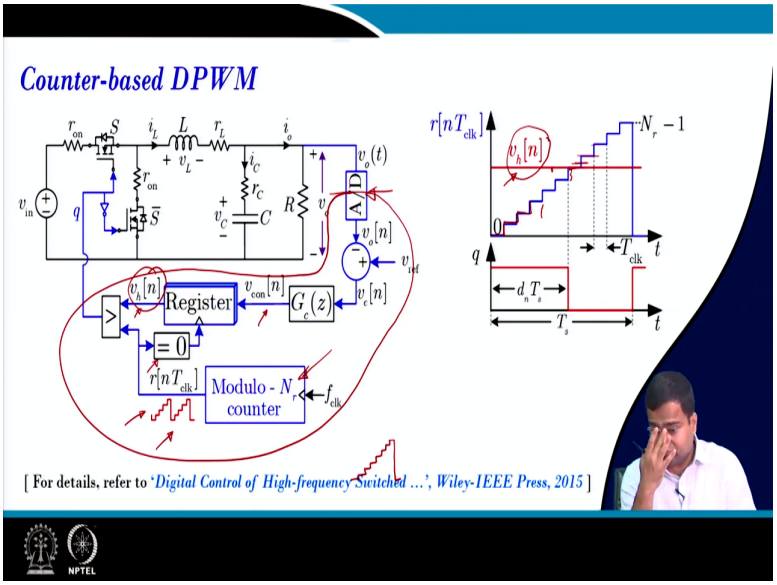

So, if you take a DC-DC buck converter for example, and we are talking about voltage mode control and we already know that ADC and then from this block onward we have everything in digital ok, these are all in digital.

Now, here this is the compensator and this is the controller output. So, this controller output is actually stored in a register, and then the output of the register, that is the same thing, but you know we need to synchronize with some clock and this actually; this value is compared with the sawtooth. Now, this question is how do you generate this sawtooth; that means, we have to generate this kind of sawtooth waveform like this. How to generate?

So, the easiest way is to take a counter and increment; that means, you counter 0, 1, 2, 3 and if it is a modulo counter; that means, the 2-bit modulo. That means, it will count you know 2 minus 1; that means, you know counting that means, N r means if it is a if you want to count from 0 to 13, then it is a 14 modulo counter; that means, 14 minus 1.

So, will upper limit will be from 0 to 14 minus 1 so; which means, for N r it will be 0 to N r minus 1 and it will again reset and it will repeat. So, this is the periodic signal which will hit the upper limit and N r minus 1, then will reset to 0 and that is called modulo counter and you can get detail in this book. So, in this architecture if you take this register output which is here and if you compared it with the sawtooth now, we want to make sure; that means when you talk in our HDL coding about q format.

So, each of these has a finite resolution; that means, DPWM will have a finite resolution as well as this number which is stored in the register it will also have a resolution. So, whether both are an 8-bit number, what is the bit size, then how do you decide the resolution so that we will discuss when we go for fixed-point implementation? But you remember that this value v h can change in the increment of this.

It cannot take any in-between value, but if the resolution of v h is higher than this DPWM then you can also get an in-between value; that means, how are you setting? So, it is recommended that the resolution of v h should be the same as the resolution of the staircase so that you can map to any of these numbers. So, they will be equal, that is why when they are equal, then you are shifting the register. That means you are storing the new value so it will update.

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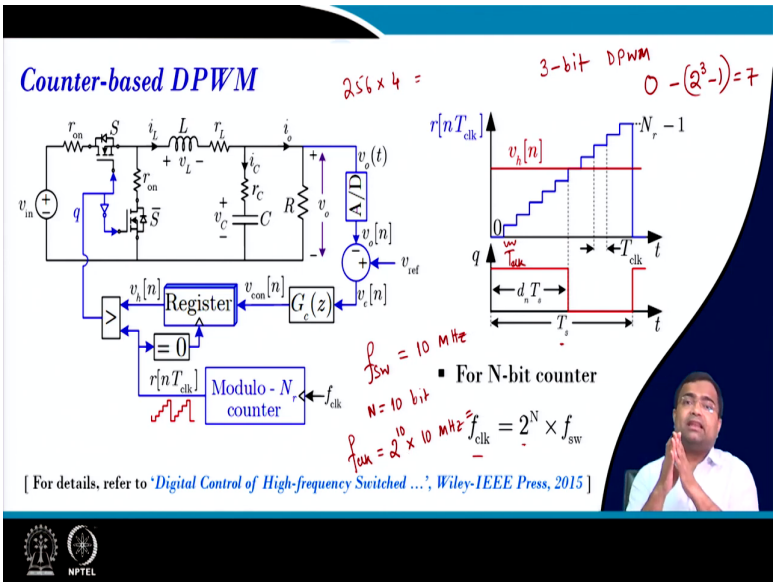

Now, the question is, if you go for this counter, I mean we want to generate a switching period of T s. And to get Ts so how many times this you have to count? That means, if you are talking about n-bit you know this DPWM, then we need to count from 2 to the power n; that means, 0, 1, 2, 3. So, if it is n-bit let us say 3-bit DPWM 3-bit DPWM, then it will come from 0 to 2 to the power 3 minus 1. That means nothing but 7. So, it will be from 0, 1, 2, 3, 4, 5, 6, 7 again it will repeat from 0.

So; that means, it will take a total of 8 clock cycles and that clock cycle is measured concerning this time period, T clock ok. So, for 3-bit you know resolution with the time period of T your clock frequency will be 2 to the power 3 into switching frequency. Now, if you imagine you need a switching frequency of let us say 10 megahertz for example, and you need N DPWM resolution to be 10-bit; then what is the clock frequency requirement? It will be 2 to power 10 into 10 megahertz.

So, it will be almost 10 gigahertz, because 2 to the power 10 is 1000, I think 1052 right it is 5 yeah 1260 256 into 4, it will be 1024. So, it is almost 10 gigahertz clock and which is practically impossible.

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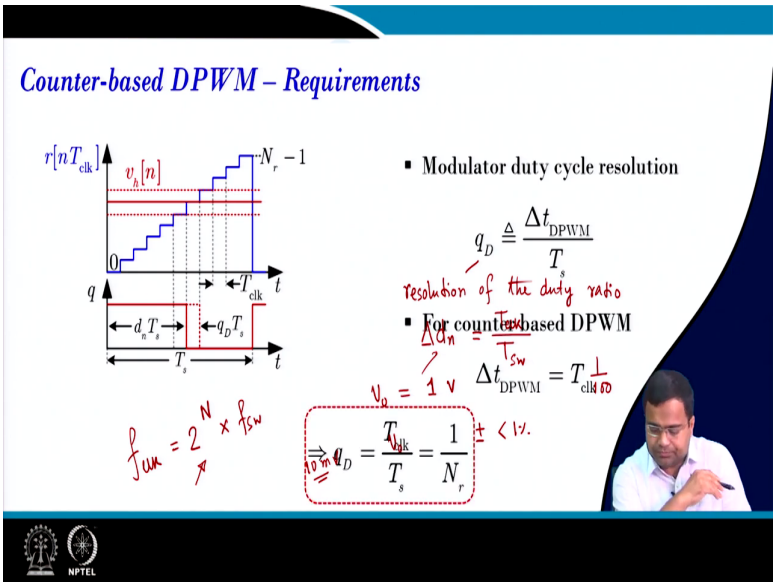

That means the requirement is that you need to meet a minimum resolution because the resolution of this DPWM will define the resolution of the duty ratio, resolution of the duty ratio.

Because, if your duty ratio resolution is poor then, you there are two problems; first of all you will not be able to meet the voltage regulation requirement; that means, the duty ratio resolution d n will be; what is the resolution? That means, what resolution can we achieve? It will be the time period of the digital clock divided by the time period of the switching clock ok. So, if you take a 100-time faster clock, then it will be 1 by 100 as the resolution if you take 1000 times so accordingly it will be selected.

Now, imagine if your output voltage v 0, the nominal value is 1 volt and you want the voltage regulation point that means, v 0 can be 1 volt and minus you know may be less than 1 percent of this, less than 1 percent. That means, that voltage regulation should be less than equal to 1 percent. That means, what is the resolution? 1 percent means it will be 10 milli volt the resolution.

So, to get 10 milli volt. So, you need a resolution minimum of 1 by 100 and if you get a better resolution you need more. So that means, to meet the required resolution the duty ratio resolution needs to be higher. And if the duty ratio resolution increases, then your f clock frequency requirement is 2 to the power N time f SW that inserts. So, that will become impractically high and you may not be able to implement it.

So, that is the bottom line of this counter base architecture; that means, you need 2 to the power N time higher clock digital clock for a high-frequency switching converter to generate this N-bit resolution two to the power; that means, N-bit DPWM. So, this is I mean this will put a limit on high-frequency applications; then what is the alternative y? So that means, this is the counter-based DPWM. Now; that means if we eliminate. So, we know about all these requirements.

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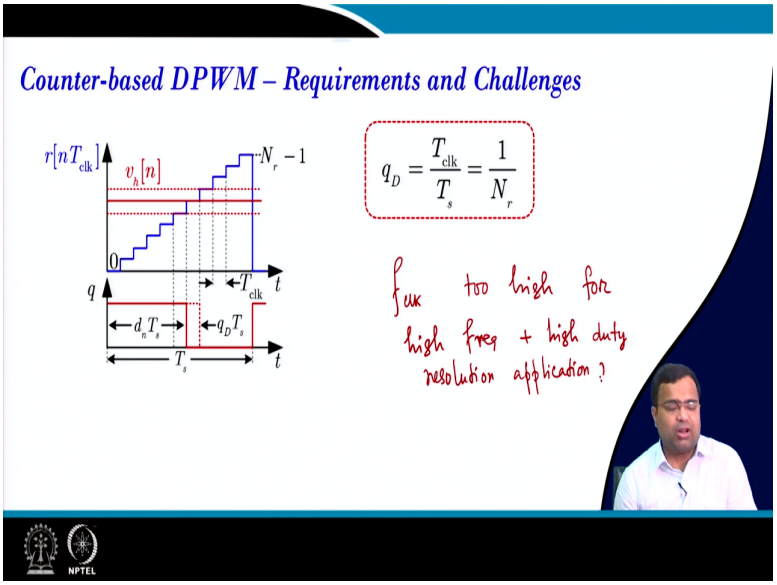

So, the challenges we have discussed, challenges mean the clock frequency requirement is too high for high frequency plus high duty ratio resolution application and that will put a limit.

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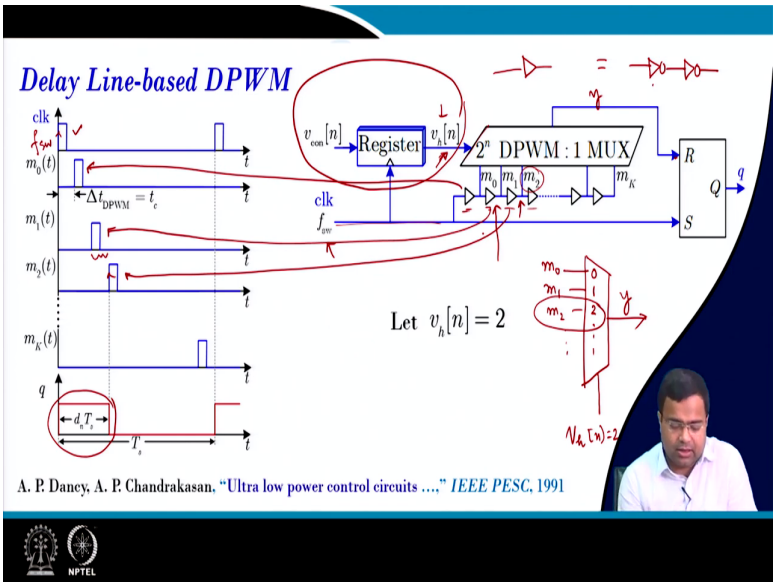

Then what is the alternative way? It is called the delay line approach, where again this part is common that register is there and this has to be compared. Now, we need to compare this value with the sawtooth waveform. So, here we are not using any high-frequency switching clock, we are simply using the switching frequency clock itself. But we are using many buffer circuits, these are the buffer circuit and each buffer circuit will have a propagation delay.

And what is the buffer circuit we know? The buffer circuit is nothing but 2 back-to-back inverters. That means each buffer circuit will require 2 plus 2, 4 transistors and each of these inverters will have a propagation delay. So, the buffer circuit will have a propagation delay. How does it work?

So, if this is 2 and you see this is the 2 to the power n MUX input; that means, an input number of inputs are 2 to the power n and single output. If this number is n, then 2 its will take this m 2 because you know if you take we talk about MUX right, this MUX. So, let us say it is 0, 1, 2 dot dot dot dot. So, these are the channel, I 0, I 1; so in this case it is m. So, let it be consistent; that means, here we are talking about m 0, m 1, m 2 dot dot dot and the output is you know, the output is here let us say y; so it is y.

So, now if we want to map; that means if the select line says that the select line is that; here what is the select line here? It is a v h n, if this is equal to 2 this channel will be selected. So, we are talking about this particular channel and this channel means, if you take the original

switching clock it will be delayed by 3 buffers; that means if you draw this is the original switching clock, which is the switching clock.

The first delay because this delay due to this delay, will be delayed, then the second stage delay will have another delay compared to the first stage and the third stage delay will be another delay. And since, the third stage output is going. So, this will reset, this will this high edge will reset this pulse and the clock of this f sw will set the pulse because it is a trailing edge modulation and this will reset.

So, this will be your duty ratio; that means, the resolution of the duty ratio will be in the order of the resolution, the difference between the buffer delay ok. That means if you can get more MUX input lines and you know by decreasing the delay you can get a finer resolution. But the problem is this delay is decided by the process technology and the supply voltage VDD.

So, you cannot assume all buffer circuits will have an identical delay because there can be some delta variation and that variation can cause a linearity issue in this case. So, here the resolution will not be linear, because all delays may not be identical, there can be some variation. So, that is one of the problems in this architecture and this architecture was proposed in 1991 you know by MIT.

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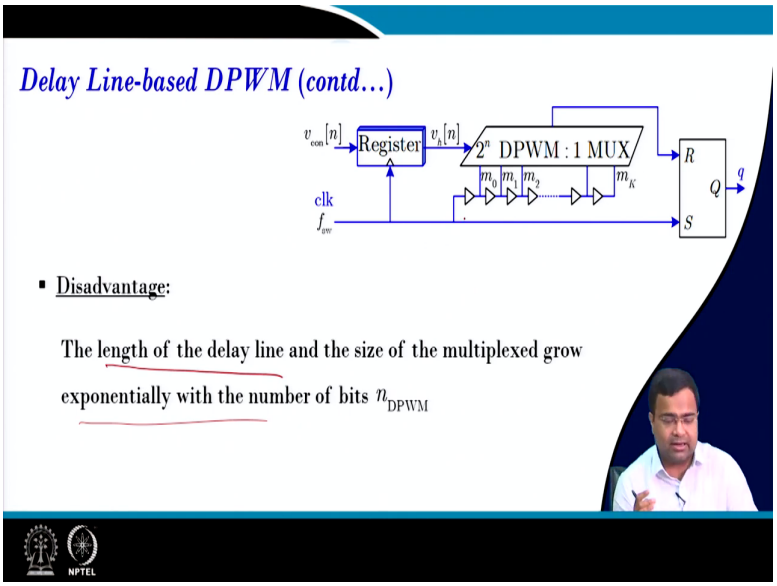

Then the next architecture; means, so that is the disadvantage that we discussed the length of delay the line is too large if you go for high-resolution DPWM. And then the linearity is and

that can exponentially increase as the number of DPWM resolutions increases. And secondly, the linearity is a problem, because all delays are not identical.

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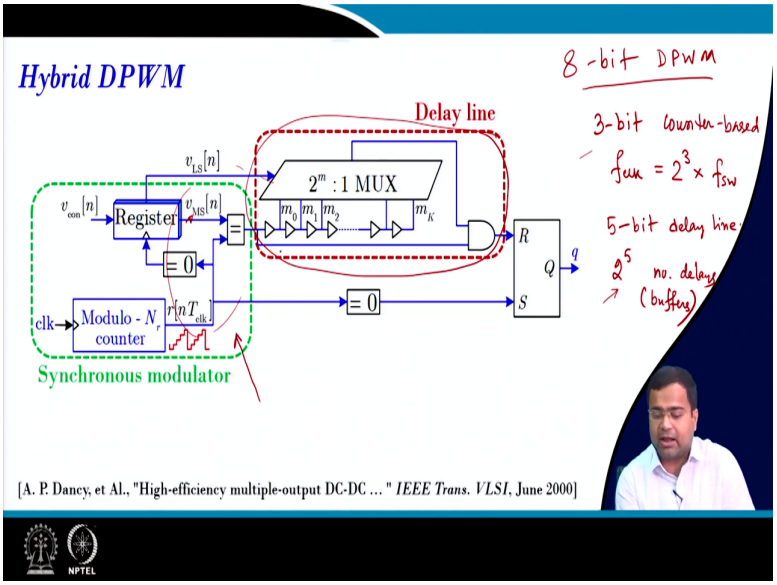

Then what is the solution? Again you know from the same group, it turns out to be another hybrid architecture; that means, you can use two structures. One is the delay line, which will reduce the clock frequency requirement, but it will give a fine tune resolution, but the coarse resolution can be achieved by the counter.

Because suppose if you use let us say need 8-bit DPWM. So, what we can do, we can use let us say you know let us say 3-bit counter base; that means, if your; that means, the clock frequency requirement will be 2 to the power 3 times f SW and we are using remaining 5-bit will be my delay line.

Then how much MUX input will be needed? It will be 2 to the power 5 minus 1 or here it will be 2 to the power 5, yeah it is almost a buffer how many buffers or delay lines? So, delay line for a 5-bit delay line you need 1 minute, the same number of the almost same number of channels, and the number of delays, or these are the buffers ok.

So, in that way you can reduce or you can improve the linearity issue because we are not using too many number delay lines, at the same time you can get a counter basis very good in terms of linearity, but it has a drawback of the clock frequency requirement. So, you can optimize.

So, you can see here, in this architecture if you take the MS b of this to use in the counter base and the LS b; LS b gives you a higher resolution MS b is a coarse selection. So, then LS b will go to the select line input, and accordingly, the signal will be delayed.

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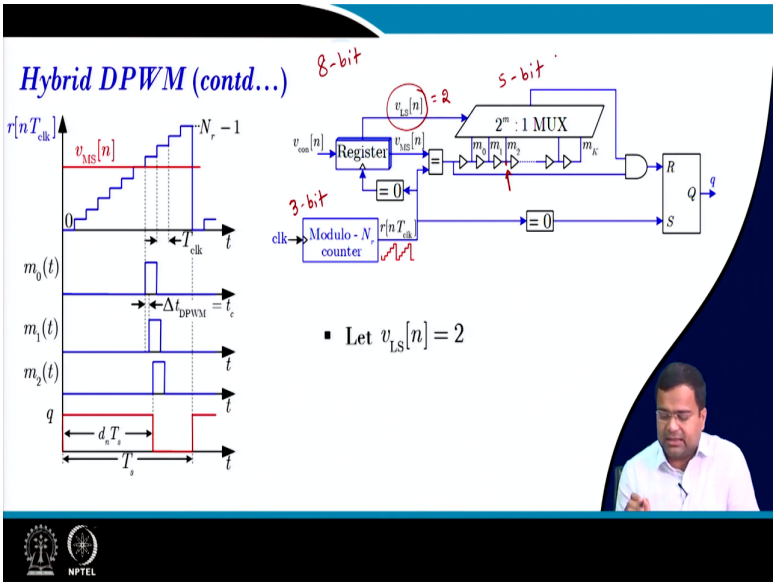

So, how does it work? That means, let us say if you take this LS b this LS b is 2. So, it will take this line; that means, m 0, m 1, m 2 this will be the line and this modulo counter is a, suppose we are talking about 8-bit DPWM and this is let us say 3-bit and this is a 5-bit ok.

So, then if LS is equal to 2, it will select this m 0 line and it is already a DPWM and this DPWM resolution may not be very high, because we are using a coarser selection.

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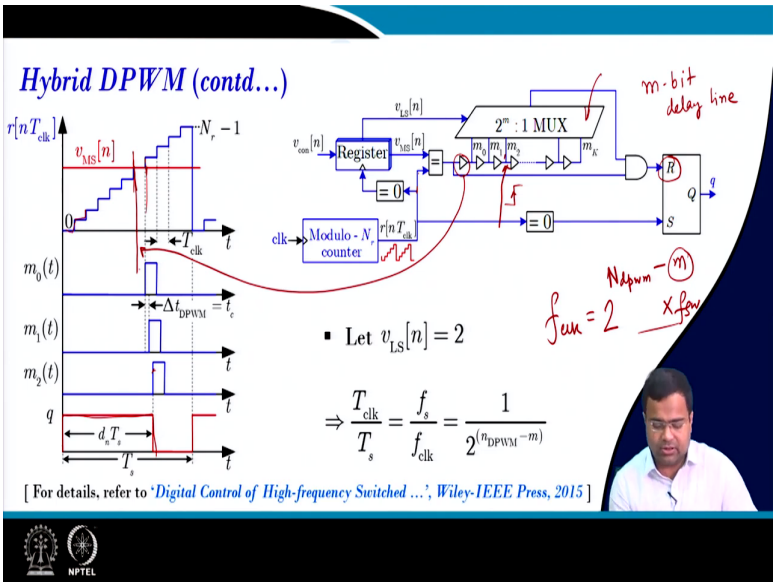

But once this is enabled, you see this pulse is enabled; that means when it will cross this part and this is the 1 and you know. So, this is the line when it will intersect then the first m 0 there will be a delay. So, this delay will introduce this delay, then it will go to the next stage by that way here will be my 2.

So, this will be my input that we are considering and your duty ratio will be like this because, at the beginning of the clock, the switch will turn on because it is trailing edge. And once this select line is decided, when this select line is going high, that edge will reset this pulse and it will switch off.

So, by that we can realize this DPWM architecture is called hybrid DPWM architecture and here the clock frequency requirement will be 1 by; that means, the ratio of the clock T clock or I will say f clock frequency will be 2 to the power N DPWM minus m. What is m? The m is decided by m-bit. I would say, this is the m-bit delay line. So that means, we are effectively reducing the number of the clock frequency into f sw.

So, you can reduce the clock frequency requirement, and that way you can improve both linearities as well as you can also reduce the clock requirement this is a very popular approach for high-frequency DC-DC converter, DPWM architecture. So, you can get detail about this architecture in this book.

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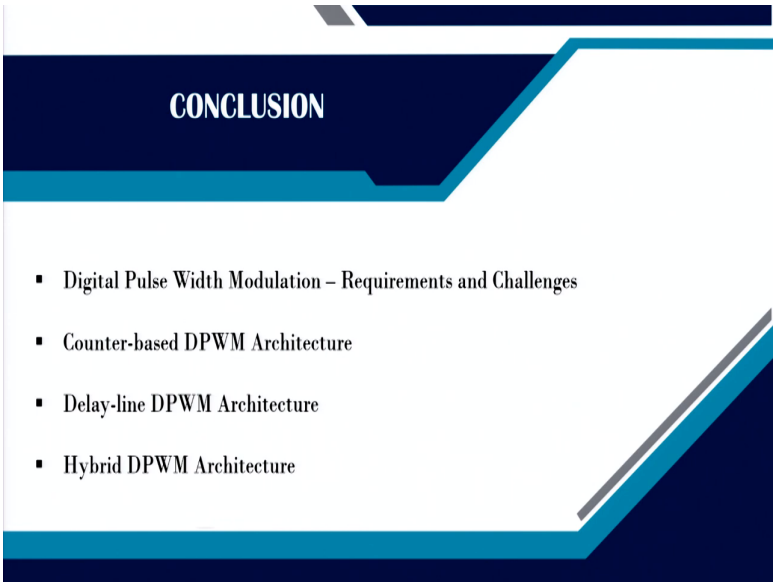

So, in summary, we have discussed various Digital Pulse Width Modulation - their Requirement and Challenges. We have discussed Counter-Based DPWM Architecture, and we have discussed Delay-Line DPWM Architecture. We have also discussed the Hybrid DPWM Architecture and how it works. So, with this, I think we will get a reasonable idea about how to implement it because we will implement some of this architecture using HDL. So, with this, I want to finish it here.

Thank you very much.