Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 02
Fixed and Variable Frequency Digital Control Architectures
Lecture - 12
Voltage Mode Digital Pulse Width Modulators and Sampling Methods

So, welcome, today we are going to talk about Voltage Mode Digital Pulse Width Modulator and Sampling Method.

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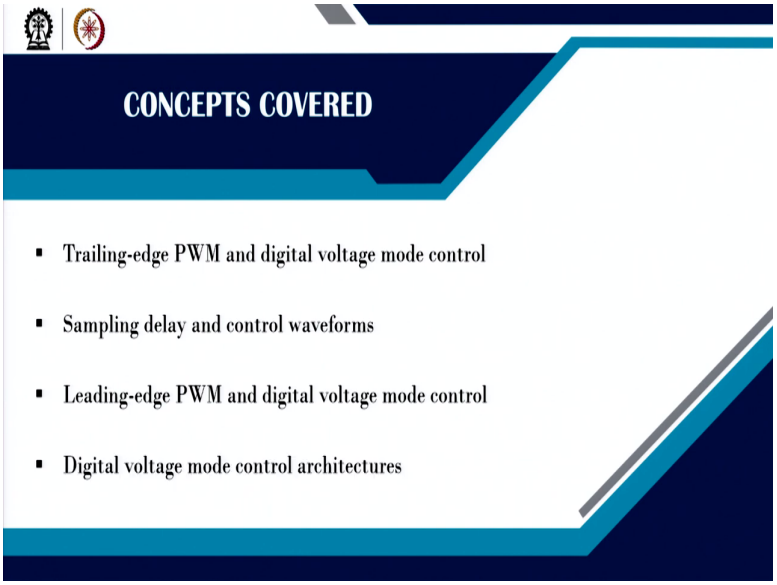

So, in this lecture, we will first talk about trailing-edge PWM and digital voltage mode control, sampling delay and control waveform, leading-edge PWM and digital voltage mode control and then digital voltage mode control architectures.

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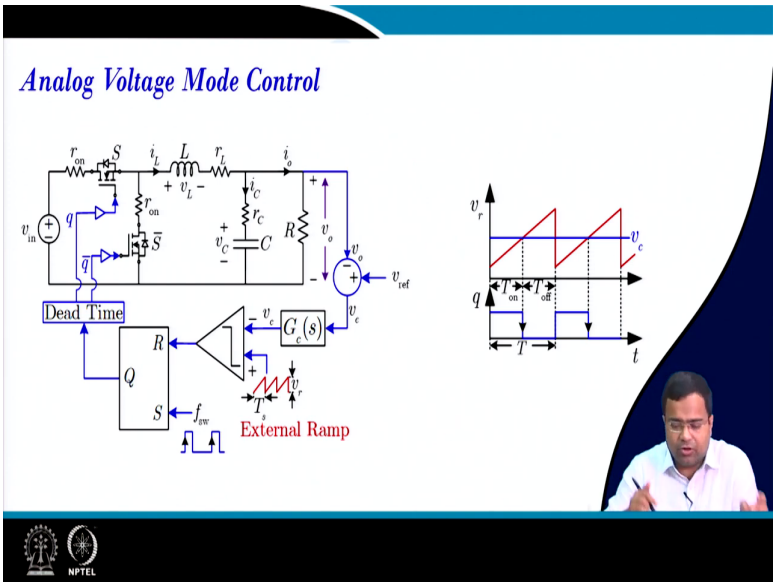

So, here we all know about Analog Voltage Mode Control. And this, you know you can get detail in our you know we have also discussed in week 1, I think it is probably in the 7th or 8th lecture where we talk about the single loop control.

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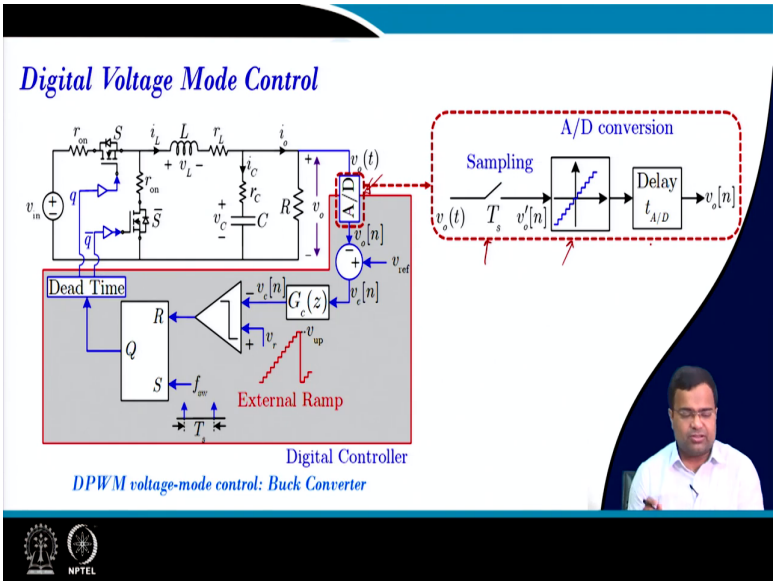

And then if we want to extend these two digital control, we have also discussed the digitization of the loop. So, here we want to we are assuming that we are already familiar with this architecture where we need an A to D converter and this is a discrete-time saw tooth

waveform where this is a sampling A to D converter means, we will have a sampler as well as a quantizer and a delay because of the conversion time.

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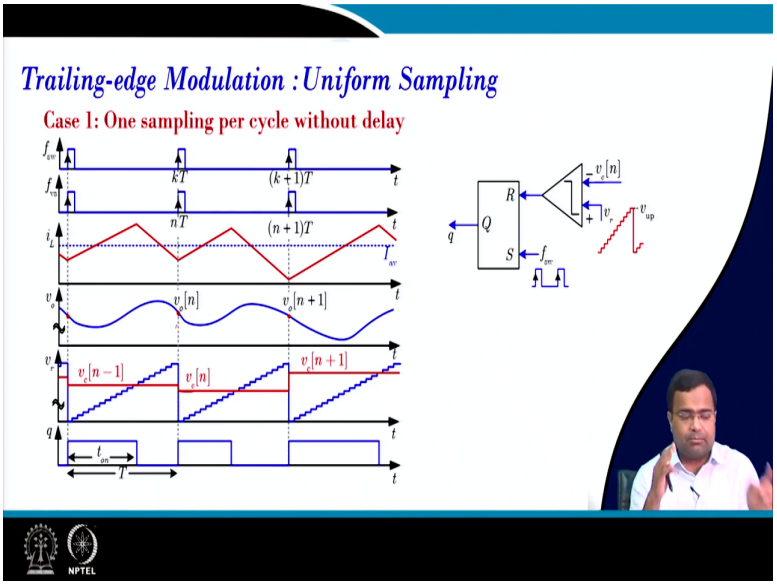

So that means if you want to realize and if you draw the control waveform, then ideally it looks like this if you take the output voltage sample here, then you need to pass through a compensator. Because, of the output voltage sample value, then it will pass through and first of all we will subtract from the reference voltage to generate the error voltage, then the error voltage is passed through the compensator and the compensator output is nothing but v c n. So, it will also get updated at the same instant.

So, we are talking about one sample per cycle, but this is practically not feasible because we cannot take the sample and immediately process it. After all, there has to be some delay.

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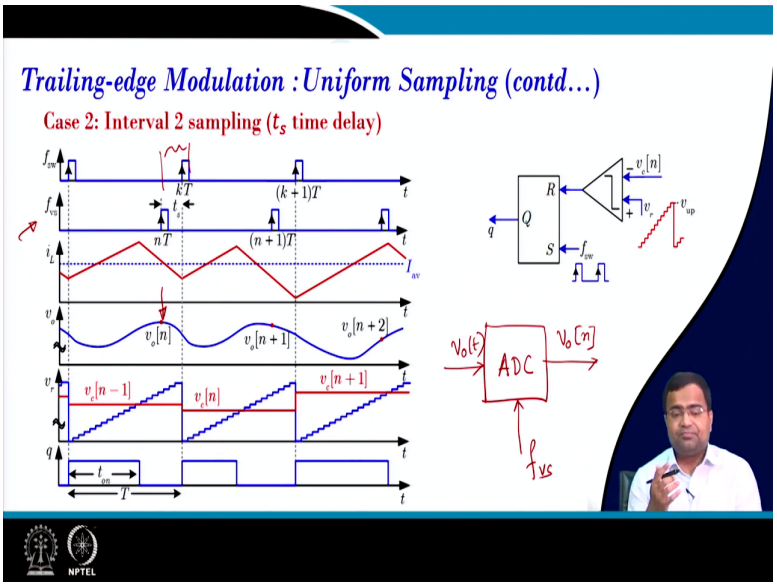

If you incorporate delay, then we need to send the sampling command here. So, you can see this is my sampling command because if you take this as our ADC, if this is our A to D converter and I am talking about this is the voltage waveform, this is a time domain and this is our discrete domain voltage waveform and here we are talking about f vs that is a sampling.

So, once you send this sampling clock, this is the time I will say this is the time that will take care of the conversion as well as computational time. But sometimes you know for hardware architecture this time is ok, you can take some fraction of the switching cycle, but if you go for a software-based solution or if you do not want to use too much of resources for high-frequency applications, then you need to reduce you know power consumption.

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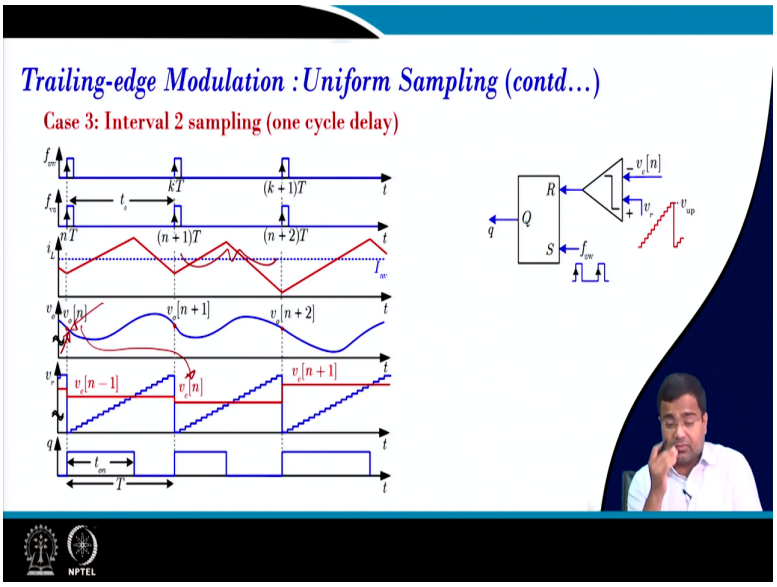

So, for that reason, we do not want very fast processing from the A to D converter. Then you can use one cycle delay; that means, you take the sample here, but after processing the error voltage followed by the compensator, you are updating in this cycle. So, that means, the controller output is updated in this cycle whereas, the voltage is captured here. So, that means, it is a one-cycle delay.

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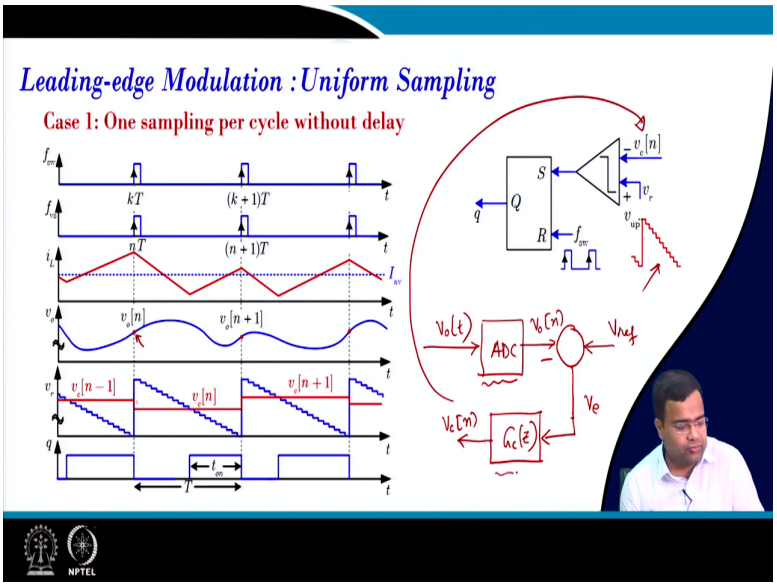

But it is on a uniform sampling, we are talking about one sample per cycle. Similarly, if we take leading edge modulation, where it is the same concept that we have discussed, though

voltage mode leading is not frequently used, just to understand the leading edge modulation technique. We can again use a decrement counter. If we go for a counter-base implementation, then again we can take the sample here, and ideally, we can process the control voltage in the same cycle because this will go through an error followed by a compensator, but practically that is not possible to realize.

So, to realize; that means, the practical conversion what we need to do; that means, if this is your ADC this is your V 0 in time, then this is your V 0 in the discrete domain, and suppose this is your subtraction and this is your V ref in digital V ref and this is our error voltage, then we pass through a compensator. So, this compensator is digital and we will discuss, how to realize that, and then it will generate our v c n that is shown here.

That is shown here and then it is compared with the sawtooth waveform. So, in that way, we can generate, but there will be a delay here.

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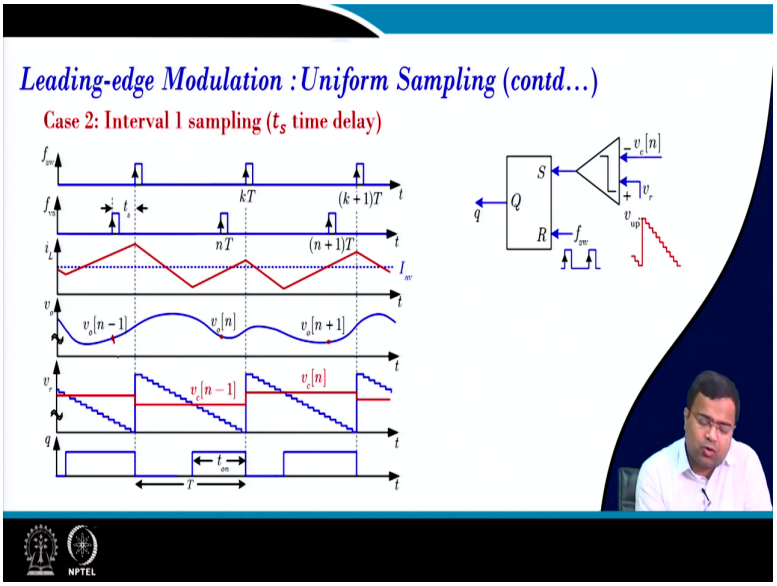

So, to accommodate that, we need to provide a delay and this is called interval 1 sampling because we are sampling during the on-state when the board one. In the earlier case, in trailing edge modulation, if you go back to the trailing edge modulation we are talking about interval 2 sampling because we are sampling during the off state of the switch that is why it is called interval 2 samplings.

So, in the interval 1 sampling, here there is no delay, but once you have a delay then you have an interval 1 sampling and this is the time for computation conversion as well as computation.

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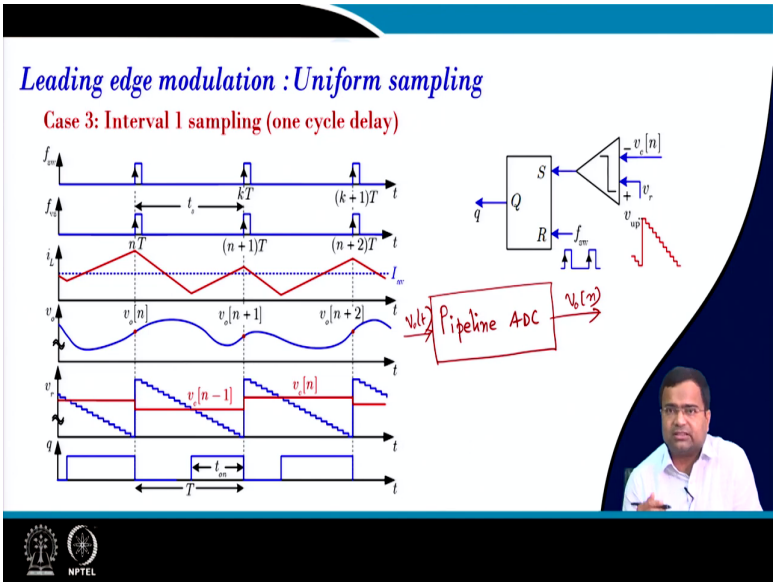

But, as I said, you can have a longer delay to accommodate that processing time because you may not want to. Now, you can ask me for the same ADC, how can we know to save power by increasing delay? So, if you talk about a pipeline ADC, a pipeline ADC. So, a pipeline ADC actually if you go for a pipeline ADC, suppose this is your time domain waveform and this is your voltage. So, pipeline ADC is the delay, and propagation delay depends on the clock cycle number. How many known pipeline stages are there?

So, now if we use a fast clock, then the delay can be reduced if you use a slower clock delay can be increased. So, even though the throughput is the same, that latency can be high, if you use a slower clock for the sampling. But if you want to speed up the conversion rate, you need to use a faster clock, which may consume more power. So, you have to be careful about the sampling of the ADC.

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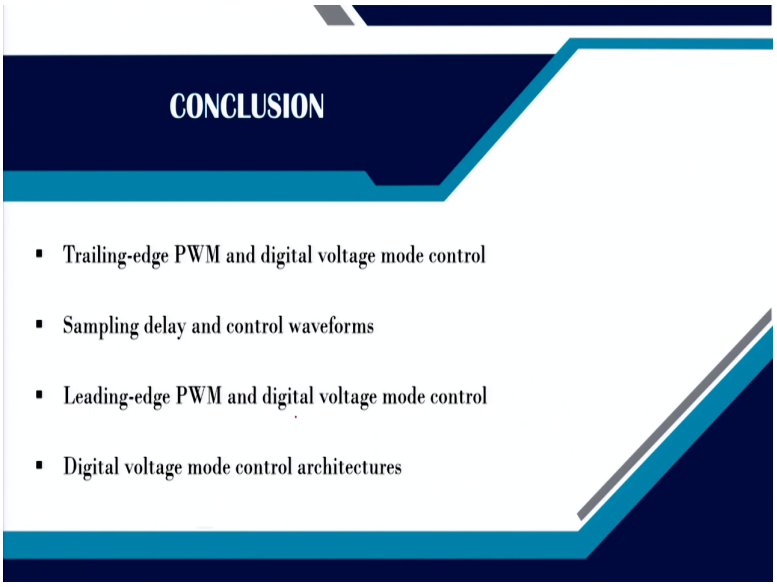

So, in summary, we have discussed trailing-edge Pulse Width Modulator and digital control architecture. Then we also discussed sampling delay and the control waveform. Then we have also discussed leading-edge PWM and digital voltage mode control and we have also discussed digital voltage mode control architecture; that means, leading edge and trailing edge.

Though in fixed frequency the leading trailing edge modulation is often used, we have not discussed how to generate this t r case; that means, saw tooth waveform. Because we will see there are various types of architecture exist and we will discuss them in the next lecture. So, with this, I want to summarize here that is it for today.

Thank you very much.