Digital Control in Switched Mode Power Converters and FPGA-based Prototyping
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Module - 12
Hardware Case Studies of Advanced Digital Control Techniques and Course Summary
Lecture - 119
Exploration of Architectures, Modeling, Design, and Control - Course Summary

Welcome we are coming to the end of this course and this is the pre-final lecture. And here we are going to summarize what we have learned in this course in terms of architecture modeling design and control technique. Then we will also see what are the implementation detail and what are the summary of different weeks.

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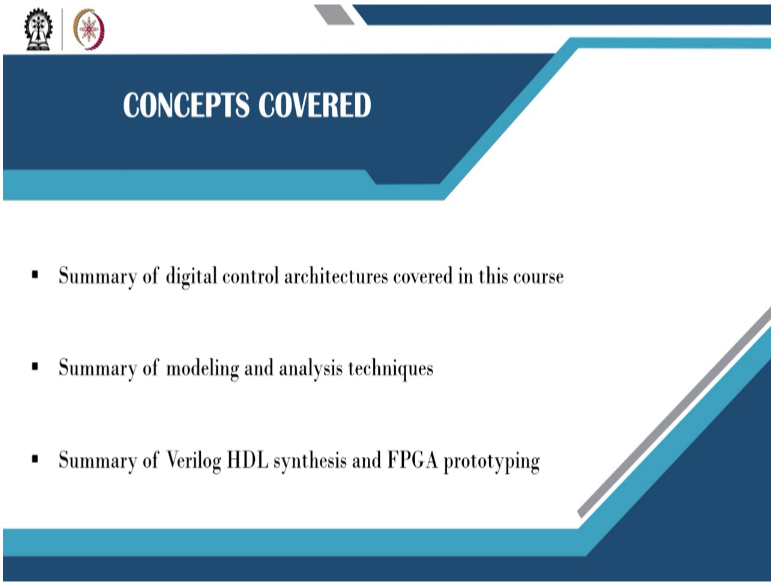

So, here will talk about we will summarize the digital control architecture covered in this course. We want to summarize the modeling analysis technique and we want to summarize the Verilog HDL, synthesis, and FPGA prototyping that we learned in this course.

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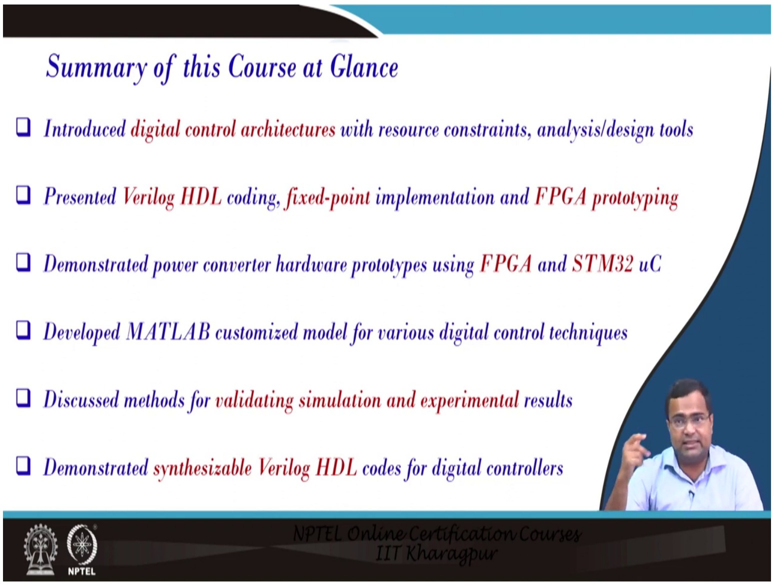

So, first the summary of this course at a glance. We have introduced digital control architecture with resource constraints and analysis and design tools in this course. We have presented Verilog HDL coding fixed point implementation and FPGA prototyping. Then we demonstrated a power converter hardware prototype using yes FPGA as well as STM 32 microcontroller in detail.

We have developed MATLAB customized model for various digital control techniques and we have discussed methods for validating simulation and experimental results. And we have demonstrated synthesizable Verilog code for digital control implementation and this can be used for ASIC power management IC design.

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In summary of this course, we have discussed the level of digitization in closed-loop switch mode power converters. We have discussed modulation and sampling techniques in fixed and variable fixed-frequency digital control. We have discussed modulation and sampling techniques in variable frequency digital control.

We have developed a custom MATLAB model simulation which is an interactive simulation model consisting of MATLAB code as well as Simulink environment combination for various architecture. We have discussed an overview of modeling techniques with their complexity and accuracy. We have compared the complexity and accuracy we have discussed the modeling of closed-loop digital control and what are the step for model validation both for I mean for large signal model validation.

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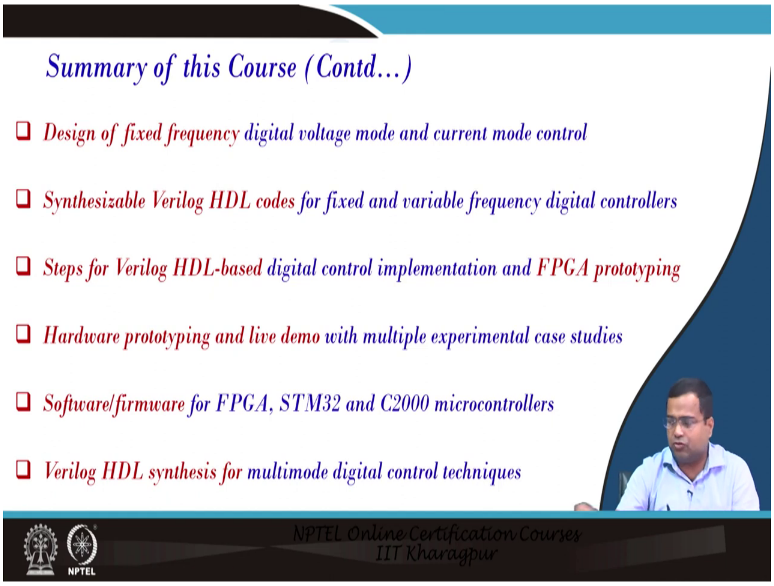

Then we designed fixed frequency digital voltage mode and current mode control. We have developed and demonstrated synthesizable Verilog codes for fixed-frequency and variable-frequency digital control in multiple case studies.

Then we developed steps for we have demonstrated step for Verilog HDL-based digital control implementation and FPGA prototyping. Then hardware prototyping and live demo with multiple experimental case studies, then software firmware introduction for FPGA STM 32 and C2000 UCS microcontroller. Then we have also presented Verilog HDL synthesis for multimode digital control technique.

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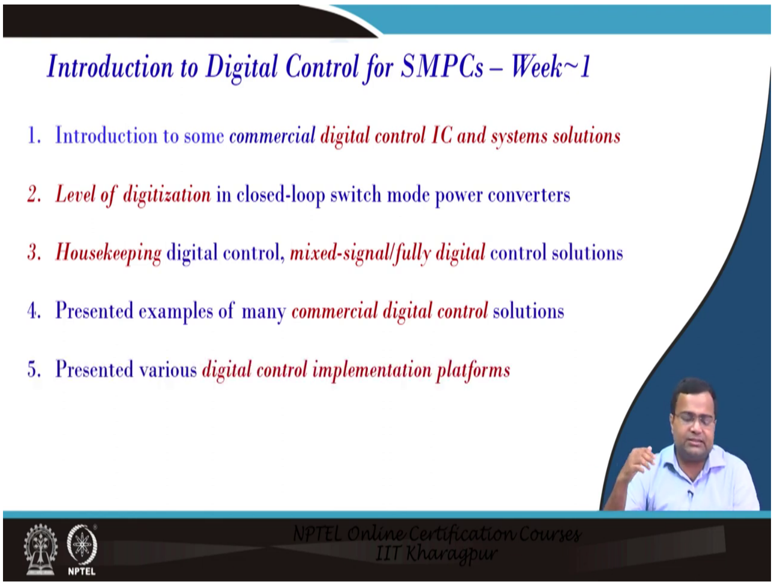

So, now we want to summarize weekly basis. In week 1 we introduced the digital control in the switch mode power converter. We have introduced some commercial digital control IC, IC, and system solutions, and we have discussed the level of digitization in closed-loop switch mode power converters.

We have discussed housekeeping digital control which is a very minimum digital digitally assisted analog control I would rather say. Then mixed signal as well as fully digital control solutions we have presented examples of many commercial digital control solutions including IC as well as system-level solutions. We have presented various digital control implementation platforms.

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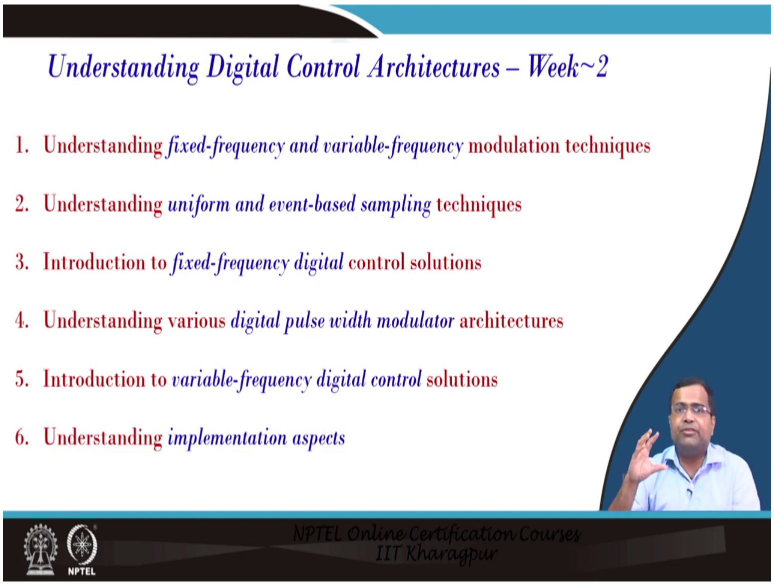

In week 2 we try to we have understood the different digital control architectures like an understanding fixed frequency and variable frequency modulation techniques. Understanding uniform and event-based sampling techniques then we understood, we have introduced a fixed-frequency digital control solution.

Then we have also introduced various digital control digital pulse width modulation modulator architectures, then we have also introduced various variable frequency digital control solutions. And we understood what is the implementation aspect of various architecture.

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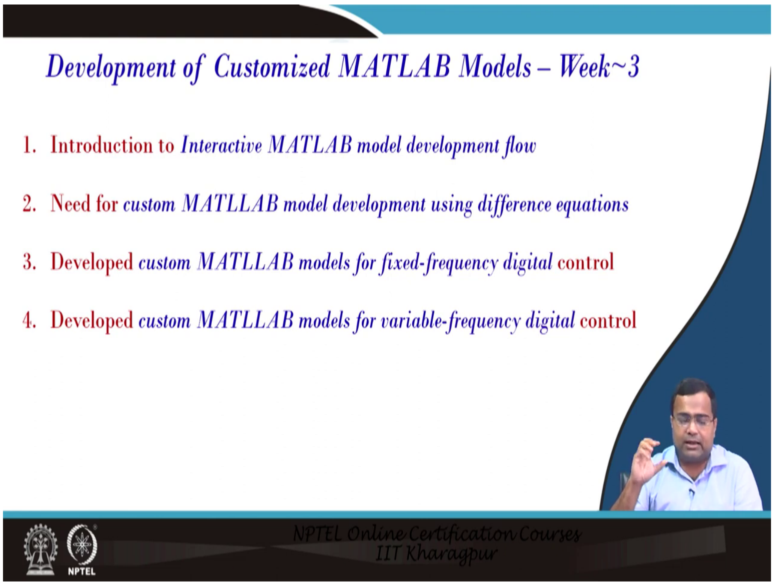

In week 3 we developed MATLAB customized model for various digital control solutions. First, we introduced interactive MATLAB model development flow, then we identified what is the need for custom MATLAB development using different equations.

Particularly if you want to sample at a particular time instant you know customized time instant like you want to vary the sampling time. Then if you want to do event-based sampling. Then how to develop MATLAB model? Then we developed a custom MATLAB model for fixed-frequency digital control. We have developed a custom MATLAB model for variable frequency digital control.

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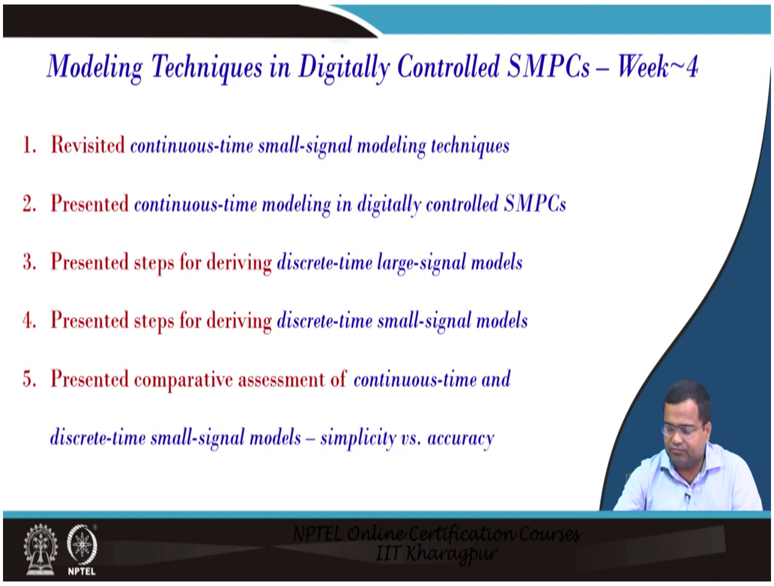

Then in week 4, we discussed different modeling techniques in the digitally controlled converters. We have revisited the continuous time small-signal modeling for analog control. Then we have presented the continuous time modeling small signal modeling in a digitally controlled converter. And we have shown that just introducing a delay can closely match your continuous-time small signal model from continuous time and the discrete-time small signal model.

But we also under-identified that from a subharmonic instability point of view, the continuous time MATLAB model may not be sufficient. Then we have presented steps for deriving the time domain discrete time large signal model, then we have designed steps for deriving the discrete-time small signal model. And we have presented a comparative assessment of continuous time and discrete time small signal models in terms of their simplicity and accuracy

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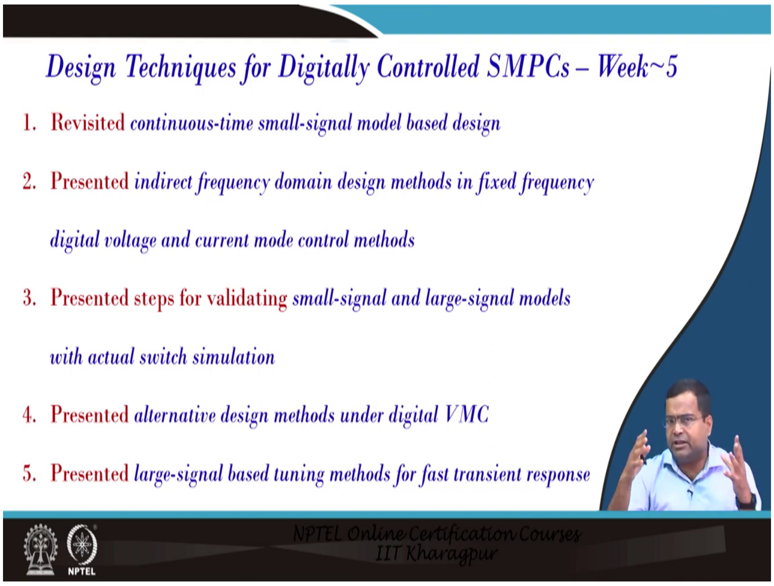

Then week 5 we discussed design techniques for a digitally controlled switch mode converter. Here we have revisited the continuous time small signal-based design method which we presented in our earlier course we have discussed in detail. Then we have presented the indirect frequency domain design method in fixed frequency voltage mode and current mode control method.

We have presented steps for validating small signal and large signal models with actual switch simulations. And we have presented some alternative design methods under digital voltage mode control which can achieve almost you know load insensitive output impedance and it can make the load transient performance much superior to the traditional stable pole-zero cancellation method.

Then we have also presented a large signal-based tuning method for getting near-time optimal recovery. And we have also discussed what is the practical aspect of large signal design and how to achieve that response using a limited gain and those aspects are also discussed.

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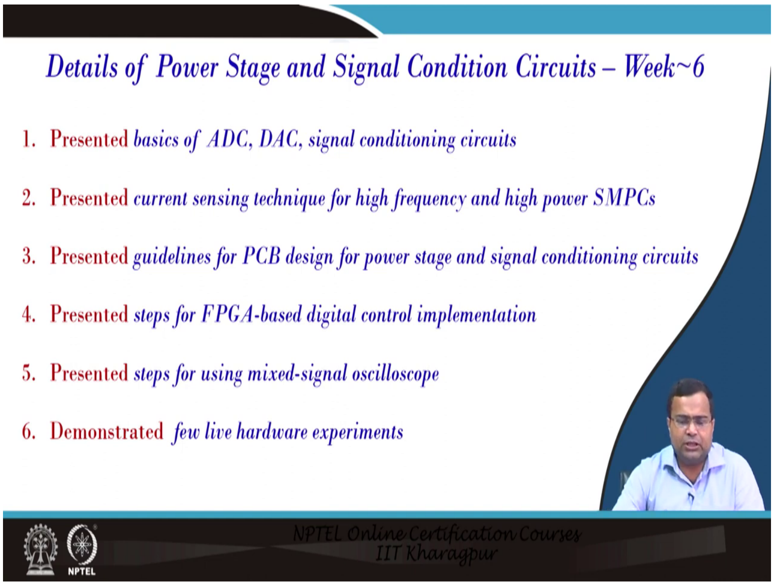

Then week 6 we presented some details about our power stage and signal conditioning circuit. We first presented the basics of ADC DAC and the signal conditioning circuit. We have presented various current sensing techniques for high frequency as well as high power switch mode power converters including both isolated and nonisolated.

We have presented guidelines for PCB design for the power stage and signal conditioning circuit. Particularly for our hardware case study hardware prototype then we have presented steps for FPGA-based digital control implementation and have presented a step for how to test and validate your digitally controlled converter using a mixed signal oscilloscope. And then we demonstrated a few live videos with hardware experiments.

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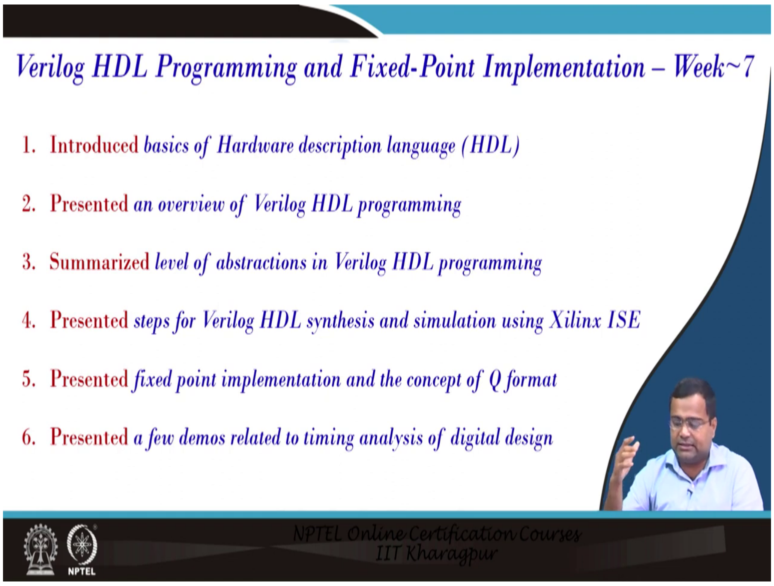

In week 7 we have started we introduced Verilog HDL programming as well as fixed-point implementation. We have introduced the basics of Verilog hardware descriptive language and why we need that hardware descriptive language. Then we have presented an overview of Verilog HDL programming, its basic rules, and what are guidelines.

Then we have summarized levels of abstraction in Verilog HDL programming like structural modeling data flow modeling and behavioral modeling and we have shown some example case studies. Then we presented steps for Verilog HDL synthesis and simulation using the Xilinx ISE simulator.

Then we presented fixed point implementation and the concept of the Q format and which was the basis for developing the digital control architecture. You know the Q format was very very crucial. Then we presented a few demos related to timing analysis and the digital for digital design.

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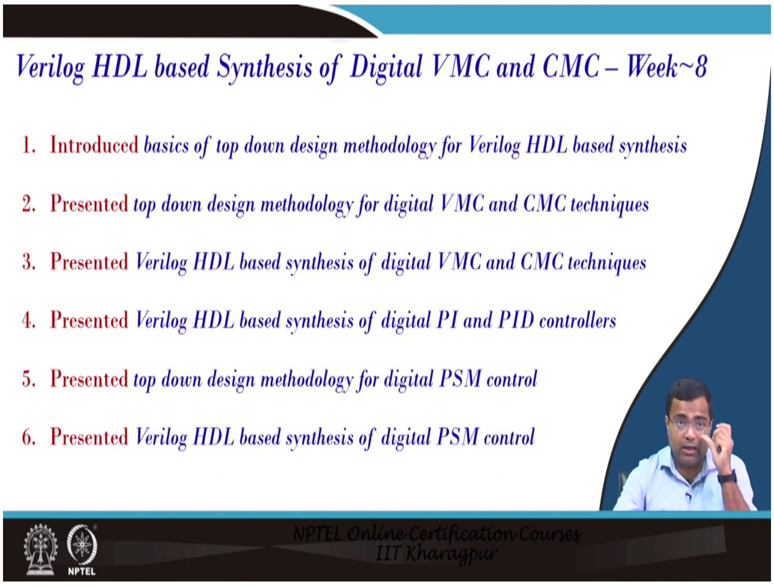

Then in week 8, we presented Verilog HDL-based synthesis of digital voltage mode control and current mode control. We have introduced a basic top-down design methodology for Verilog HDL-based synthesis. We have presented a top-down design methodology for digital voltage mode control and current mode control technique.

We have presented Verilog HDL-based synthesis of digital voltage mode and current mode control technique. We have presented Verilog HDL synthesis of digital, digital PI, and PID controller and we have presented top-down design methodology of digital pulse skipping control. And we have presented Verilog HDL-based synthesis of digital pulse skipping control and we have also shown some experimental results.

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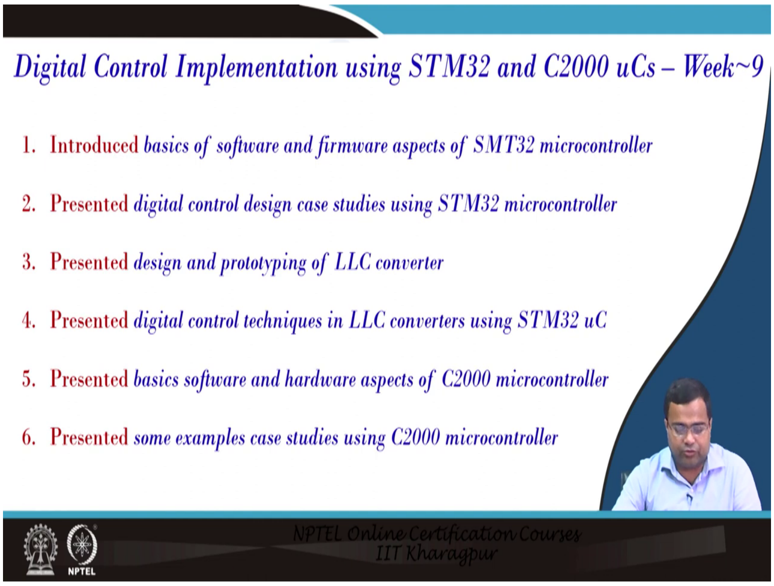

Week 9 is dedicated you know for digital control implementation using STM 32 and C200 UCS microcontrollers and the expert from STM microelectronics. They have introduced basic software and firmware aspect of the STM 32 microcontroller. They have presented digital control design case studies using STM 32 microcontroller.

They have presented the design and prototyping of LLC converters for different power levels. And they have also presented in detail about digital control implementation technique in LLC digital control techniques in LLC converter using STM 32 microcontroller. Then we have also you know experts from Texas Instruments who have presented basic software and hardware aspects of the C2000 microcontroller and then presented some example case studies using the C2000 microcontroller.

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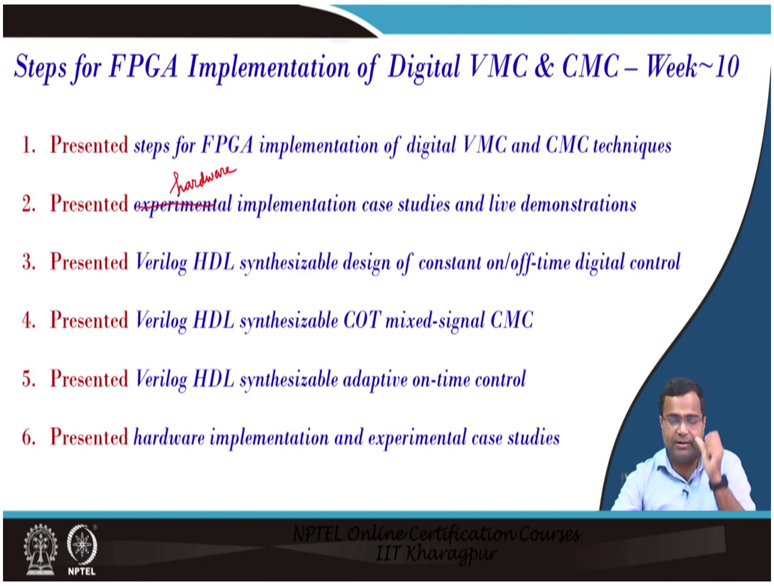

In week 10 we discussed in detail the steps for FPGA FPGA-sedimentation of digital voltage mode and current mode control including both fixed frequency and variable frequency control. We have presented step stepsFPGA implementation of digital voltage mode control and current mode control technique.

We have presented experimental you know experimental implementation I would say hardware implementation this should be hardware implementation. Implementation case studies and live demonstration we have presented Verilog HDL synthesizable design of constant on-off time digital control for both current mode and voltage mode.

We have presented Verilog HDL synthesizable constant on time mixed signal current mode control. Then also Verilog HDL synthesizable adaptive on-time control peak current based on what also we have discussed and we have presented hardware implementation as well as multiple experimental case studies. And we have also shown many live demonstrations.

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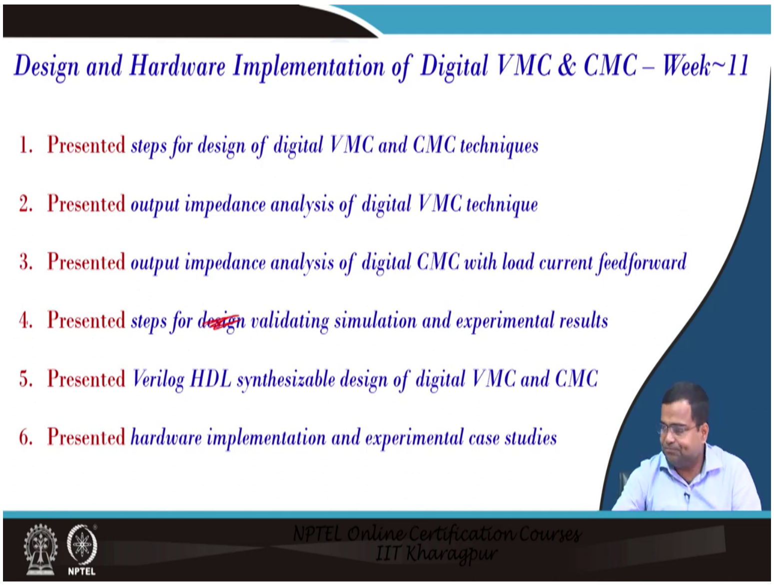

In week 11 we considered the design and hardware implementation of digital voltage mode and current mode control technique. We have presented steps for digital voltage mode and current mode control design, we have presented output impedance analysis of digital voltage mode control.

We have presented an output impedance analysis of digital current mode control with load current feed-forward and we have shown how the transient response can be significantly improved using load current feed-forward. We have presented steps for digital design validation, validation using we have a design step for validating it is not designed.

We have presented steps for validating simulation and experimental results. We have presented Verilog HDL synthesizable design of digital voltage mode and current mode control and we have presented multiple hardware you-know implementations and experimental case studies.

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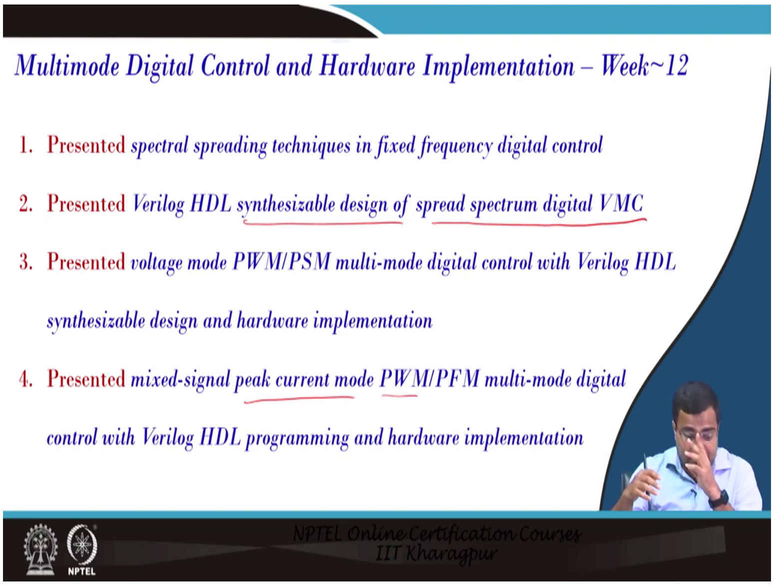

Week 12 which is the last week there we have presented the spectral spreading technique in fixed frequency digital control using bi-frequency modulation. We have presented voltage mode pulse width modulation and PSM multi-mode digital control with Verilog HDL synthesizable design and hardware implementation. We have presented Verilog HDL synthesizable design of space spectrum technique in voltage mode control.

Then we presented mixed signal peak current mode PWM, PFM multi-mode digital control and we developed the Verilog HDL synthesis and we have developed the architecture. And we have implemented using FPGA and we have shown multiple experimental case studies including transient response using multi-mode as well as using DPWM.

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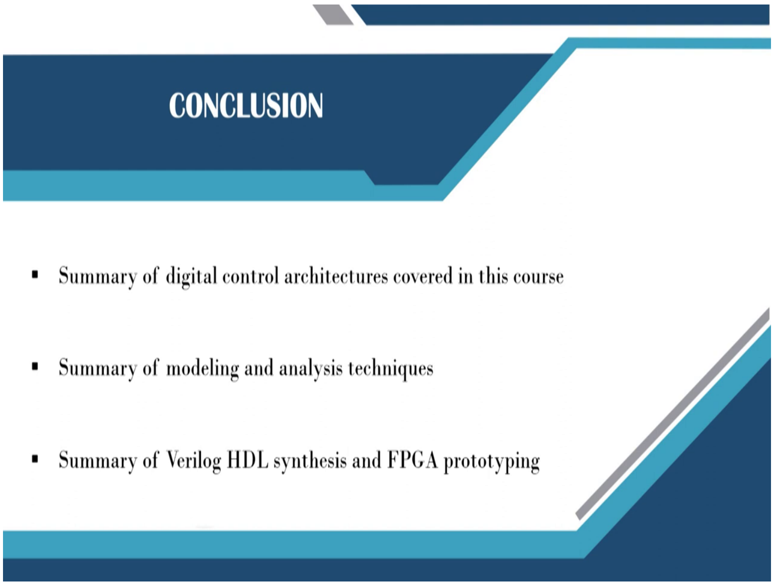

So, in summary in this course, we have discussed multiple digital control architectures covered in this class. We have discussed modeling analysis techniques we have discussed a summary of Verilog HDL synthesis and FPGA prototyping. And in this context, I think this course will be very useful you know different weeks are very important to come up with a new control algorithm, and Verilog HDL we have extensively covered which may be useful for coming up with IC implementation.

So, we will have one more week the last week where we want to you know summarize. And the course I mean particularly we will want to introduce our team and our activity and we will that will be the last lecture of this course that is it for today

Thank you very much.