Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 11
Hardware Case Studies of Advanced Digital Control Techniques and Course Summary
Lecture - 113
Top Down Design Methodology of PWM/PSM Multi-Mode Digital Control

Welcome. In this lecture, we are going to talk about the top-down design methodology of pulse width modulation and pulse skipping modulation based on multi-mode digital control.

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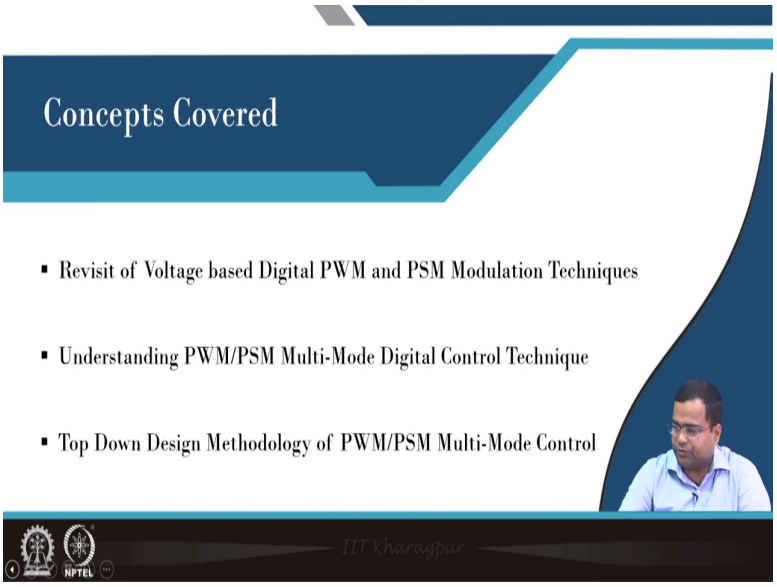

So, here we will first revisit the voltage-based digital PWM and PSM modulation techniques that we have already presented. Then understanding the PWM PSM multi-mode digital control and then the top-down design methodology of PWM PSM multi-mode control.

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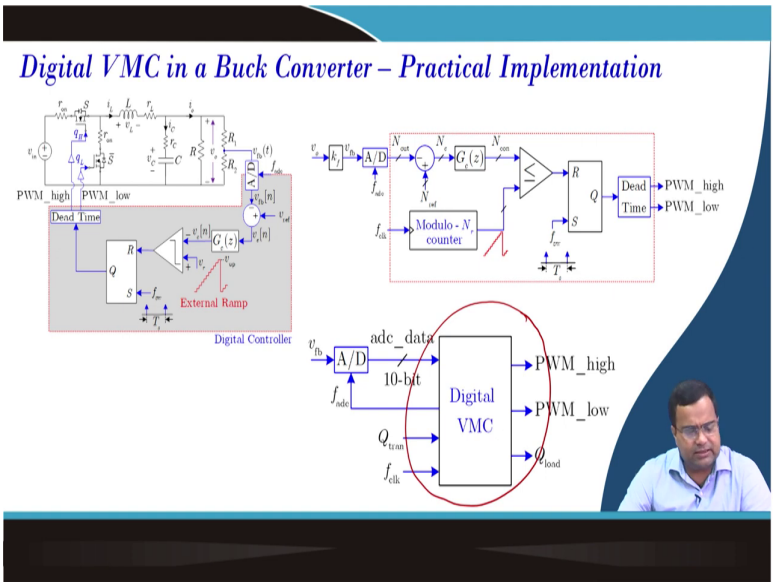

So, here if we talk about digital voltage mode control in a buck converter that we have presented you know multiple times I think in lecture number 71 to 74 we have discussed this in detail and this is the architecture that we have already developed and we have implemented. We have synthesized using Verilog HDL and we have also implemented using FPGA and all these architectures are discussed in detail.

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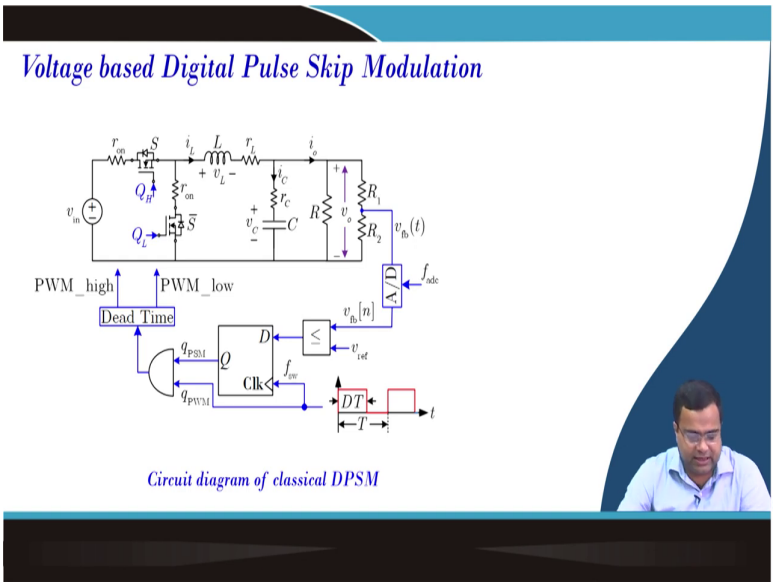

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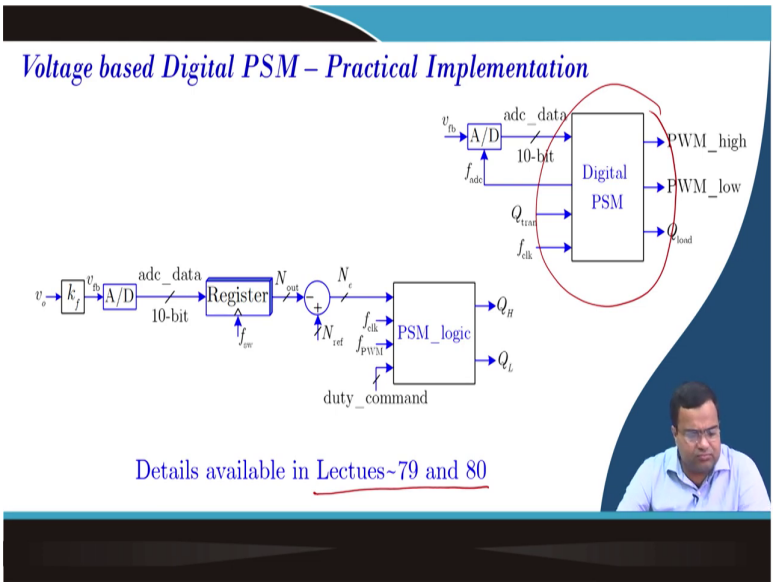

We have also discussed the digital voltage-based digital pulse skip modulation technique, where the practical implementation of this block we have developed in lecture numbers I think 79 and 78 we have discussed the top-down design methodology as well as HDL synthesis synthesizable HDL Verilog HDL code and also we did FPGA prototyping for hardware implementation.

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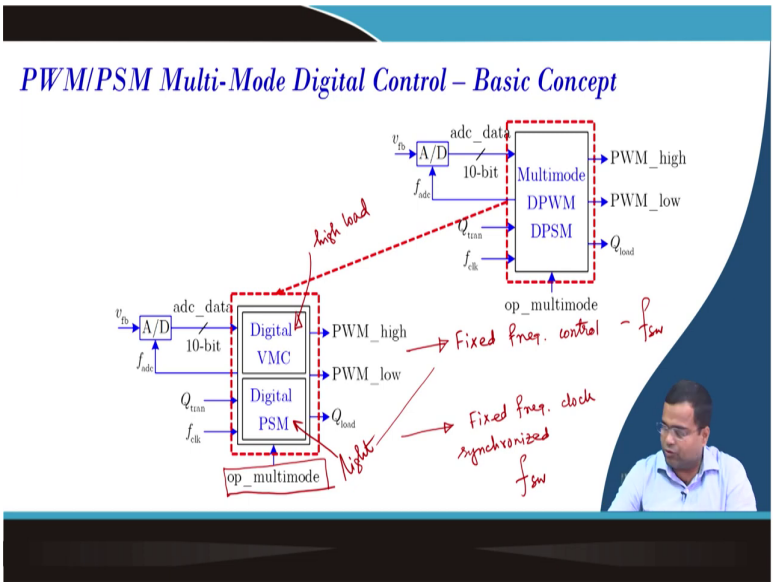

Then now we are going to multi-mode control where we want to interface between PWM and PSM and it is well known we have discussed in lecture number 110 what is the need for

multi-mode because we need to improve the light load efficiency. So, typically this will operate you know under I will say high load and this will operate under light load.

So; that means, we are trying to interface digital voltage mode control and digital pulse skipping modulation, the good thing about this is these two control like a voltage mode control is a fixed frequency control we know that you know it is a fixed frequency control. It is a fixed frequency control or basically, it is a trailing edge modulation and here it is you know that fixed frequency clock synchronized.

That means if this is it is a switching frequency clock it is synchronized with fsw because, at every rising edge of f sw clock, it will decide whether to skip the pulse or charge the pulse and depend upon the condition of the output voltage with respect to the reference voltage. So, here we have the option either to go for multi-mode or we can continue under pulse width modulation throughout and we will show in the subsequent lecture we will show the experimental case study also.

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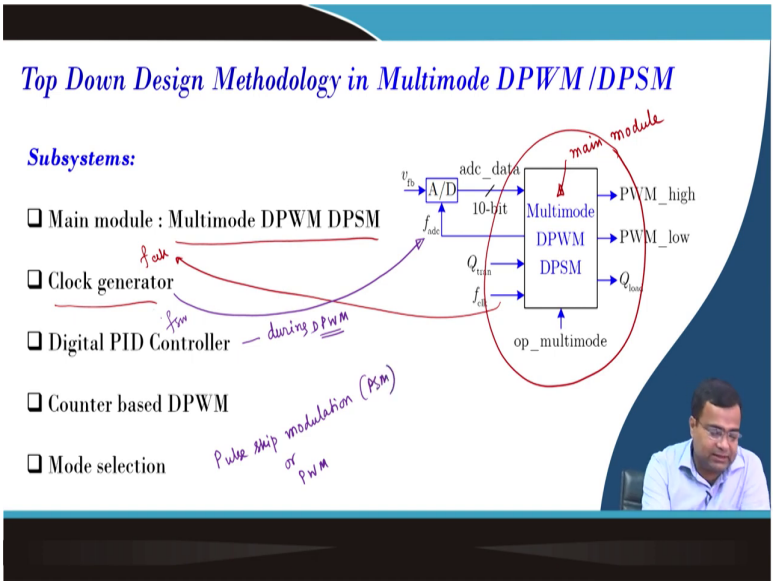

Now, the next question is how to interface. So this block now we have to synthesize using Verilog and we want to describe the Verilog top-down design methodology, but before that, we need to understand what is there inside this block. So, first of all, if we want to design the Verilog HDL code this is the main module. So, this is the main module that will interface with the io pin outside to pin. So, it should look like a digital controller ic.

So, as a main module then it requires a clock generator because this will generate, this will take what input we know that this highest frequency clock. This is the input to this block and it will generate an ADC clock; that means, the output of this will generate what output of this will generate this ADC clock. It will there is no DAC requirement and also it will generate a switching frequency call clock ok.

The digital PID controller because we want to consider the digital PI controller during PWM, if PWM is activated or digital PWM I will say DPWM then we will activate the digital PID controller because we need a feedback controller and we are using a counter bases DPWM because this will be used to generate both and there is a mode selection; that means, whether to go for pulse skip modulation; that means, PSM or PWM whether to go for PSM and PWM.

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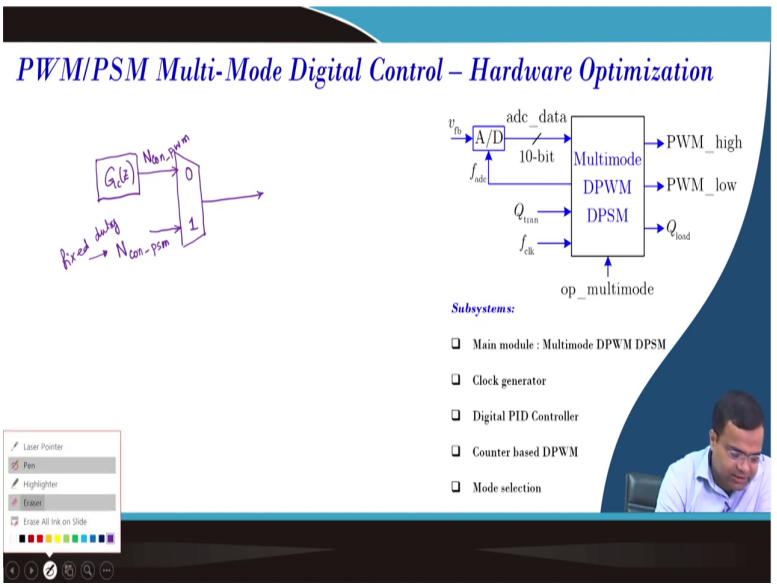

So, we need this module and we want to optimize the hardware. So, we want to optimize the hardware. So, the main module; means, let us consider how can we optimize the module. So, suppose we consider a block like this where this is our controller, this is our G c Z, and assuming that they are properly scaled. This is the controller output I will say this is the controller output and this is the N command, this is the duty ratio command. So, this is 0 this is 1; that means, this is the this is I will say it is PWM controller and this is the duty ratio related to I would say this is related to you can say PSM.

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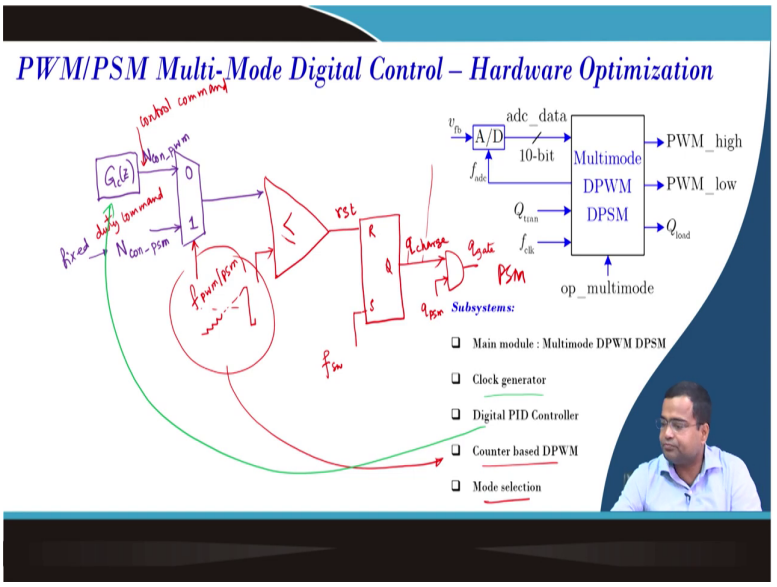

So, this is the fixed value because we are talking about a fixed duty ratio. This is related to fixed duty command and this is the control command which is a duty ratio command but under closed-loop control. Now, this has to be compared with a sawtooth waveform what is that? That means, we need to have counter-wise DPWM right?

So, this will you know whether it is higher or lower based on that it will decide; that means, if it is you know this is typically less than equal to then, then it will generate a pulse which is the reset pulse. That means, it will turn off the thing because we will have what we have reset and there is a set; that means, R S flip flop, and what is R S flip flop? R S flip flop will be I would say it is a switching frequency clock at every rising edge.

And whatever will be generated is like a p you can say Q charge pulse and it will be combined with Q PSM. What is Q PSM? That means, that is a mode selection and it is the final, P I will say gate signal that will go to the driver circuit. So, depending upon whether you are using a synchronous configuration or whether you are generating you know asynchronous; that means, the diode-based thing.

If the pulse skipping logic is 0 then it will go. So, under if we go purely by voltage mode control then we need to have an additional bypass. So, we will go into that, what is the mode selection logic? So, this looks like this block is like a PSM mode operation ok. So, under PSM there will be a select line on whether to select f PWM versus PSM. If it is 0 it will take

PWM, if it is 1 it is PSM and during PWM we can take this straight away as a gate pulse, and then it will go to the gate time circuit.

So; that means, it requires a mode selection of the counter base DPWM this will come from here we want to optimize the hardware. It requires a digital PID controller which is nothing, but this digital PID controller ok, the clock generator which will generate all this clock and the main module.

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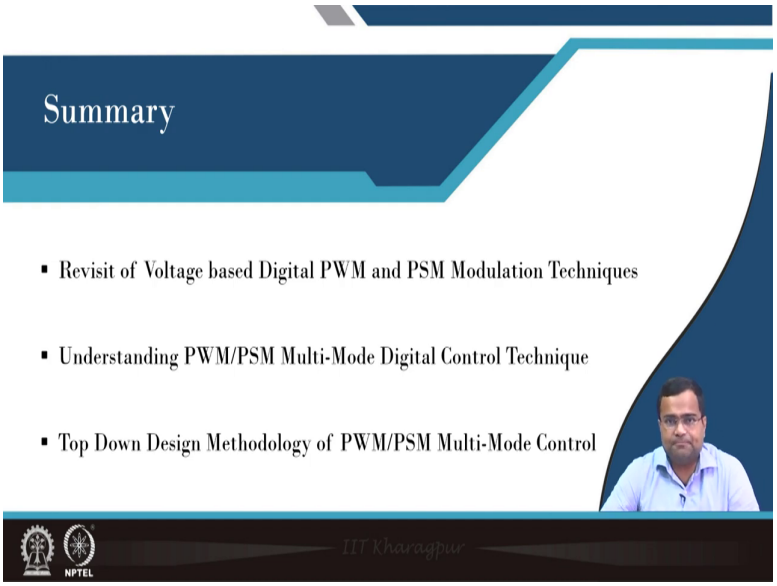

So, this will be continued I mean we are going to continue in the next lecture about the Verilog synthesizer block.

So, today we want to summarize that we have revisited the voltage mode digital PWM and PSM technique. We understood the PWM PSM multimode digital control technique and what is the top-down design methodology for this control. So, in the next lecture, we are going to synthesize this PSM PWM multi-mode digital control using Verilog HDL and we want to consider some experimental case studies that are it for today.

Thank you very much.