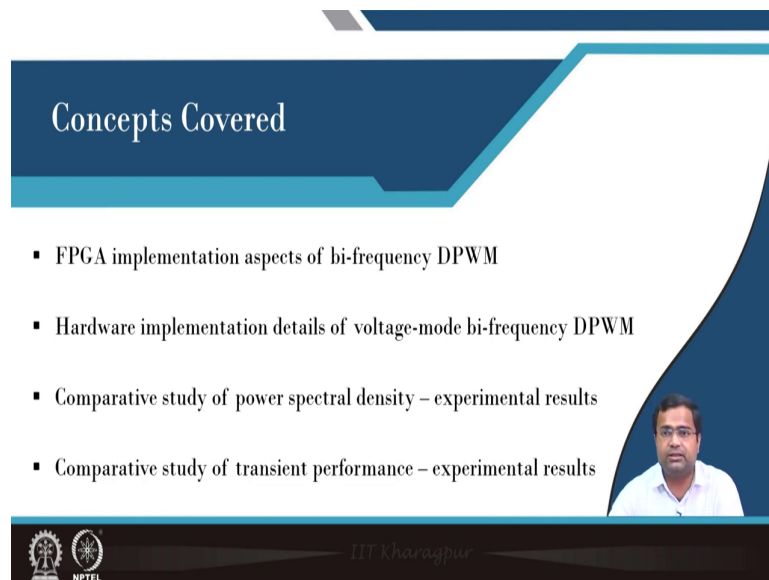


Digital Control in Switched Mode Power Converters and FPGA-based Prototyping
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Module - 12
Implementation of Multimode Digital Control and Course Summary
Lecture - 112
Performance of Bi-frequency Spread Spectrum DPWM and Experimental Results

Welcome it is a continuation of the previous lecture and we are going to consider here the Performing Assessment under Bi-frequency Spread Spectrum DPWM using Experimental Results.

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Concepts Covered

- FPGA implementation aspects of bi-frequency DPWM
- Hardware implementation details of voltage-mode bi-frequency DPWM
- Comparative study of power spectral density – experimental results
- Comparative study of transient performance – experimental results

The slide features a dark blue header with the title 'Concepts Covered' in white. Below the header is a white area containing a bulleted list of four topics. A small video inset of the speaker is visible in the bottom right corner of the slide. At the bottom of the slide, there are logos for IIT Kharagpur and NPTEL.

So, here we will first talk about briefly touch upon the FPGA implementation aspect for our hardware. And then we want to show the hardware implementation detail of voltage mode bi-frequency DPWM then a comparative study of power spectral density using experimental results and also the impact on the transient performance using experimental results.

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Spectral Spreading using Voltage Mode Bi-frequency DPWM

The slide illustrates the concept of spectral spreading using Voltage Mode Bi-frequency DPWM. On the left, a graph shows the inductor current i_L and the Bi-Frequency (BF) control signal over time t . The current waveform is a high-frequency ripple superimposed on a lower-frequency envelope. The control signal is a square wave with a period T_1 and a duty cycle q_{PWM} . On the right, a circuit diagram shows a buck converter with an input voltage v_m , a MOSFET S , an inductor L , a diode \bar{S} , and a capacitor C . The output voltage v_o is filtered by a network of resistors R_1, R_2 and capacitors C_1, C_2 . The digital control system consists of a Voltage Mode Bi-frequency DPWM block that takes a reference q_{PWM} and a switching frequency f_{dk} as input and outputs $v_{in}[n]$ and $v_{in}[n]$ to the converter. A feedback loop with a transfer function $G_c(z)$ and a dead time block is also shown.

[S. Kapat, "Reconfigurable Periodic Bi-frequency DPWM with Custom Harmonic Reduction in DC-DC Converters," *IEEE Trans. Power Electron.*, vol. 31, No. 4, pp. 3380 - 3388, Apr. 2016]

So, we have discussed this bi-frequency modulation technique in detail. And this conceptual waveform also we have discussed in the previous lecture. And the details of this technique are discussed in this research paper.

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Digital Bi-frequency VMC in a Buck Converter – Practical Details

The slide provides practical details for the Digital Bi-frequency VMC in a Buck Converter. On the left, a circuit diagram shows the buck converter with an input voltage v_m , a MOSFET S , an inductor L , a diode \bar{S} , and a capacitor C . The output voltage v_o is filtered by a network of resistors R_1, R_2 and capacitors C_1, C_2 . The digital control system consists of a Voltage Mode Bi-frequency DPWM block that takes a reference q_{PWM} and a switching frequency f_{dk} as input and outputs $v_{in}[n]$ and $v_{in}[n]$ to the converter. A feedback loop with a transfer function $G_c(z)$ and a dead time block is also shown. On the right, a table lists the power stage details:

Power Stage Details	
Inductance L	1.8 μ H
Capacitance C	200 μ F
Input Voltage V_{in}	5 V
Output Voltage V_{ref}	1.8 V
Switching Frequency f_{sw}	200 kHz
Load resistance (R_c, R_{sw})	(13.5 Ω , 0.33 Ω)

Below the table, a block diagram shows the digital control system. It includes a 10-bit A/D converter that takes the output voltage v_o and provides adc_data to the Voltage Mode Bi-frequency DPWM block. The block also takes f_{dk} and Q_{ref} as input and outputs Q_{load} to the converter. The output of the DPWM block is $v_{in}[n]$ and $v_{in}[n]$.

And in this technique what we are going to design first of all we have already designed this block using Verilog HDL in the previous course previous lecture and we are going to consider our hardware prototype which we have discussed multiple times that we have used inductor value this capacitor value this.

In this case, we are we have considered an input voltage of 5-volt reference output 1.8-volt switching frequency nominal. So, this is our nominal switching frequency of 200 kilohertz and we have changed the load resistance between; that means, 13.5, and then the switch load is connected or disconnected based on and this will create load step up and step down transient. And this is our schematic diagram.

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Digital Bi-frequency VMC in a Buck Converter – Practical Details

Controller Details	
Proportional gain K_p	1.926
Integral gain K_i	0.2
Derivative gain K_d	11.85
ADC resolution	9 bit
DPWM resolution	9 bit
Controller clock f_{clk}	100MHz
Voltage feedback gain k_f	0.27
Ramp voltage V_m	2V

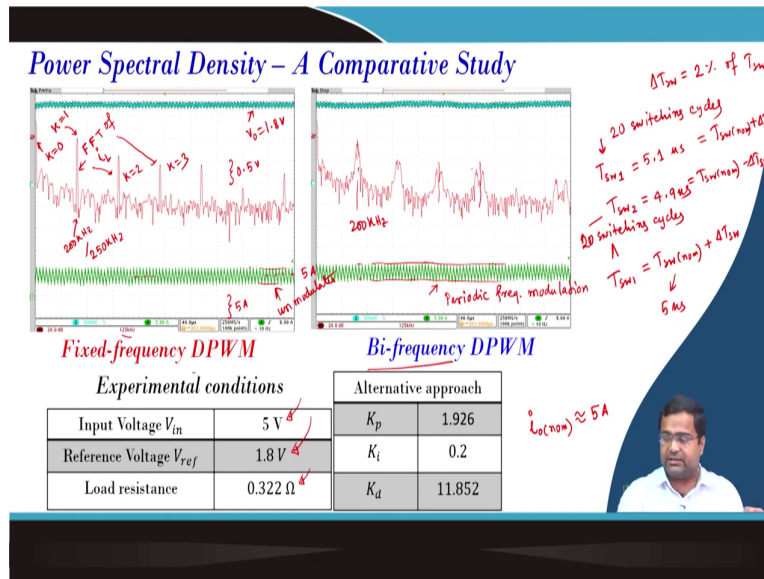
Digital PID controller
 $f_{sw} = 200kHz$
 $f_{clk} = 100MHz$

Now, the other hardware detail we have considered is a digital PID controller. We have considered a digital PID controller. And the implementation of the digital PID controller we have discussed multiple times. And these are the K_p discrete-time integral gain and discrete time derivative gain. Though we are using 10-bit ADC, we have discarded 1 bit, because otherwise, ADC bit should not be higher than DPWM. It should be smaller than DPWM, but since DPWM resolution we cannot increase it beyond 9 bit.

Because we are using 100 megahertz the digital controller clock, that is our f_{clk} and our switching frequency is 200 kilohertz nominal. So, we cannot have a better than 9 bit resolution, but we can drop one more bit to the ADC, but it will affect the regulation. That is why we kept nine bit and it is more or less we are getting we are not getting as such limit cycle oscillation. That is why we have continued with this design.

And we know that the voltage feedback gain is 0.27 and we are using an equivalent ramp voltage of 2 volts.

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Now, we want to show an experimental case study of power spectral density. And we have considered a 5 volt input of 1.8 volt is the desired output. The equivalent load resistance is 0.322 and we are getting a nominal load current which is around experimental we are getting a 5 ampere load current. And this is the power spectral density where which is the effect of the inductor current. These are the spectral peak these are the spectral peak.

And this is the fundamental component where K is equal to 1. This is the switching frequency, this is the dc component where it will be K equal to 0 then this will be K equal to 2, K equal to 3, and so on. And it is visible that this frequency is because it is 125 kilo, which is 250 kilohertz. So, this point is 200 kilohertz ok.

Now, this is the waveform of the inductor current and you can see the inductor current in this division is 5 ampere and the output voltage here in the division is 0.5 volt and it is v0 is 1.8 volt ok. And you can see the average load current is roughly 5 ampere. That is an inductor load current average inductor current is the load current. The same operating condition we have continued with the bi-frequency.

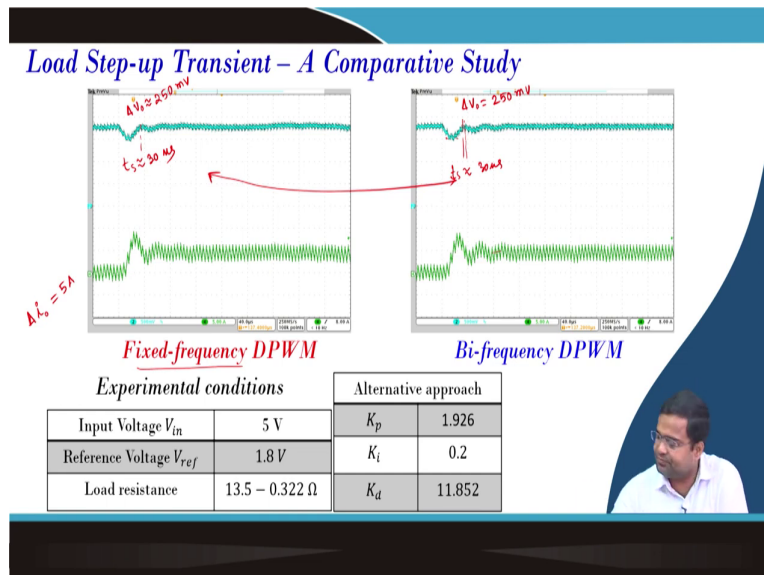
And what we have used? We have hopped between 2 switching frequent periods; that means, Tsw1, which is nothing, but Tsw 1 which is 5.1 microseconds, and Tsw2 is our 4. 9 microsecond and we have discussed that this Tsw1 is nothing, but the Tsw nominal plus delta Tsw and this one is nothing, but 5 microsecond and we have discussed that Tsw is nothing, but 2 percent of Tsw nominal ok.

So; that means, T_{sw1} is $T_{sw \text{ nominal}} + \Delta T_{sw}$ and this is nothing, but $T_{sw \text{ nominal}} - \Delta T_{sw}$. And this and the effect this we are changing T_{sw1} for a 20 switching cycle and this is also followed by a 20 switching cycle. So, every 20 switching cycles we are changing the time period for the case of bi-frequency DPWM. Here the time period is fixed.

And you can see, the spectral spreading is happening. So, their base point is 200 kilohertz, but the power spectrum is getting distributed and it is creating also slowly these things have created a side loop. You can see the side loops are created. So; that means, the spectrum the power spectral density I mean the peaks are going down and this can improve EMI, but interestingly if you see this ripple because they are changing periodically, this impact is not significant compared to the unmodulated case; that means, this is under.

So, this is a periodic frequency modulation, right? We are using periodic frequency modulation and this is like an unmodulated or fixed frequency. So, there is an insignificant impact now our next question interesting point how it is going to affect the transient performance because this technique a closed loop is on all the time and this was proposed in the research paper that we have presented I mean this research paper we have presented this result. So, you can get a detail in this paper.

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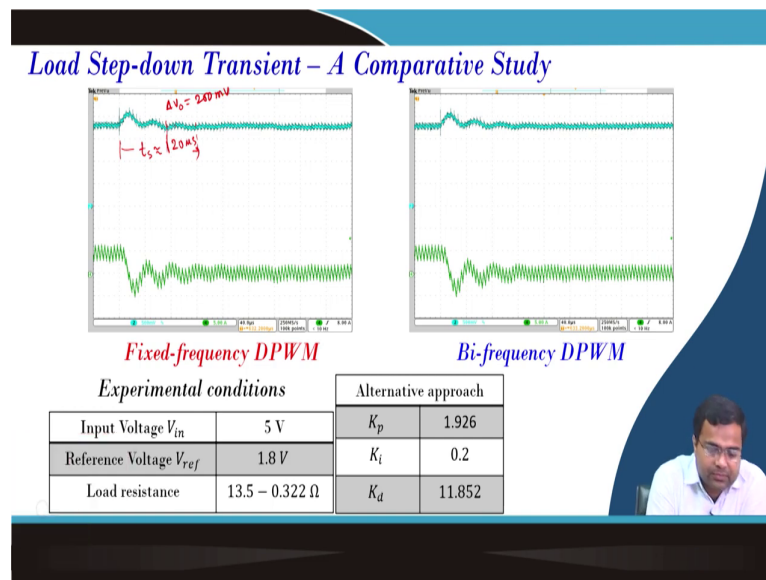


Next, if we go to the transient performance. We want to see you see this is a load step-up transient under fixed frequency modulation for a load step-up of almost 5 ampere load step and how much is the undershoot, because this division is around 0.5 volt. So, the undershoot

delta V0 is roughly around how much it is around 250 millivolt. And what is the settling time? So, the settling time is 40 microsecond. So, it is roughly around T settling is like 30, 30 microsecond you can think of.

And there is a current overshoot also now if you compare the same thing with the bi-frequency DPWM you see that effect is insignificant, because of the same. The delta V0 here is also 250 millivolt and there is slight oscillation, but here also settling time is you can see that ts is almost thirty microseconds. So; that means, the transient step-up transient performance is almost unaffected you can see slight oscillation because this periodically it is changing ok otherwise the response looks quite similar.

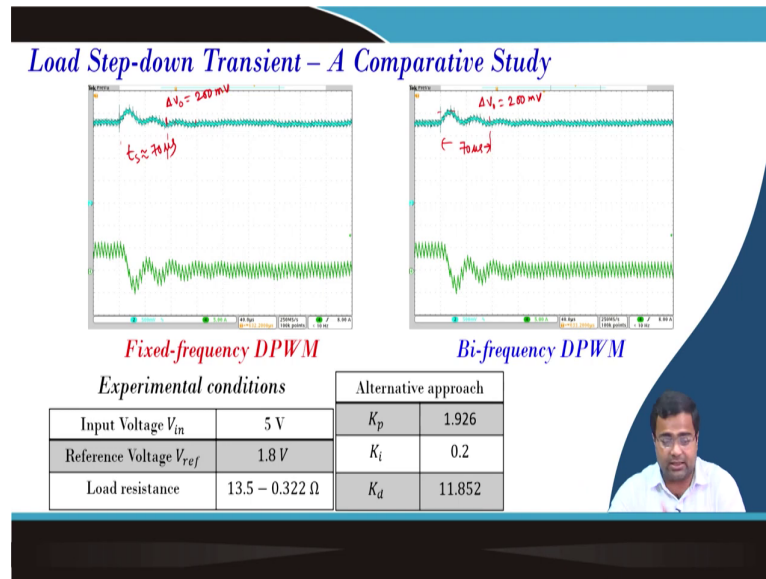
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Now, the step-down transient response. So, this is a step-down transient response for fixed frequency PWM. So, we are getting almost 200 overshoots almost 200 millivolt and the settling time you can say it is taking up to this cycle because there is some sort of slow damping or even if you consider this. So, settling time is coming around 40 almost 3; that means, 120 microsecond.

Now, if we talk about this you can see that even this is getting settled fast. I mean, if you take this as a settling time I would say if you take this as the settling time this is more or less settled here.

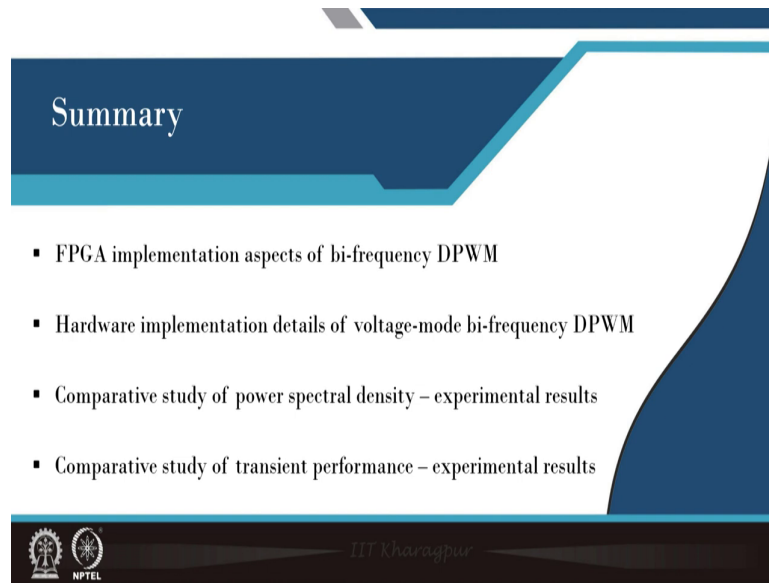
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That means the settling time is nearly you can say 40 like a 70 microsecond. Here also it is settled. So, it is like a 70 microsecond is a settling time and overshoot is also the same as this 200 millivolt.

That means the bi-frequency for two percent has hardly any effect on the transient performance. So, what we can conclude is that if we can do it properly then there will be an insignificant impact on the transient performance, which is very important for us, but at the same time it can achieve you know kind of considerable spectral spreading peaking the peaking can be reduced and by spreading the spectrum and that is the interesting part.

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Summary

- FPGA implementation aspects of bi-frequency DPWM
- Hardware implementation details of voltage-mode bi-frequency DPWM
- Comparative study of power spectral density – experimental results
- Comparative study of transient performance – experimental results

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So, in summary, we have discussed the FPGA implementation aspect of bi-frequency DPWM. We have shown the hardware implementation detail and we have made a comparative study of power spectral density we have shown also what is the impact on the transient performance and that performance impact was insignificant, but we got a considerable reduction in the spectral peak by this bi-frequency DPWM. That is it for today.

Thank you very much.