Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 11
Design and Validation Case Studies using Digital Voltage and Current Mode Control
Lecture - 110
Need for Multi-Mode Digital Control and Design Requirements in SMPCs

Welcome to this lecture we are going to discuss the Need for Multi-Mode Digital Control and some of the Design Requirements. And in the last week 12th week, we will consider multiple implementations as well as hardware case studies of multi-mode control.

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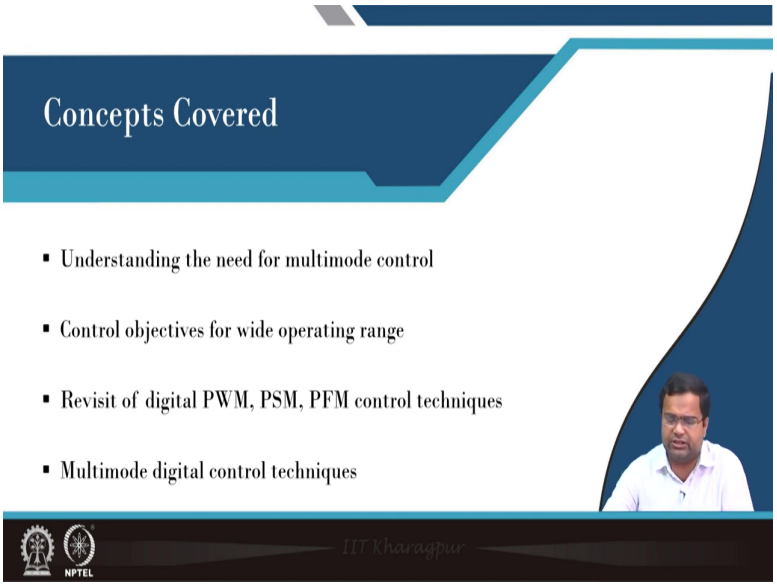

So, in this lecture, we will first talk about we need to understand the need for multi-mode control, and what are the control objectives for a wide operating range like wide input voltage and load current range. Then we want to revisit digital PWM PSM and PFM control techniques and we want to do you know consider a few multimode digital control techniques.

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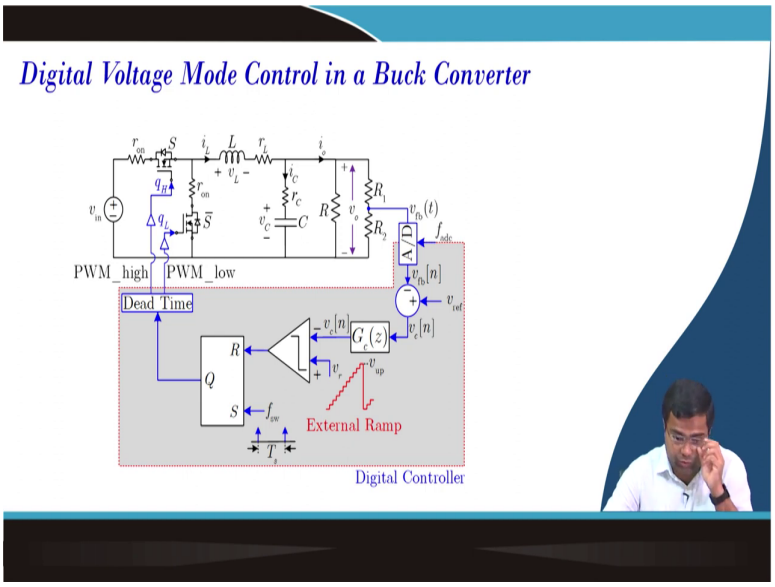

So, we have discussed digital voltage mode control in a buck converter in sufficient detail both in week 2, and week 3 in MATLAB simulation as well as in week 8 we implemented with hardware implementation Verilog HDL-based coding.

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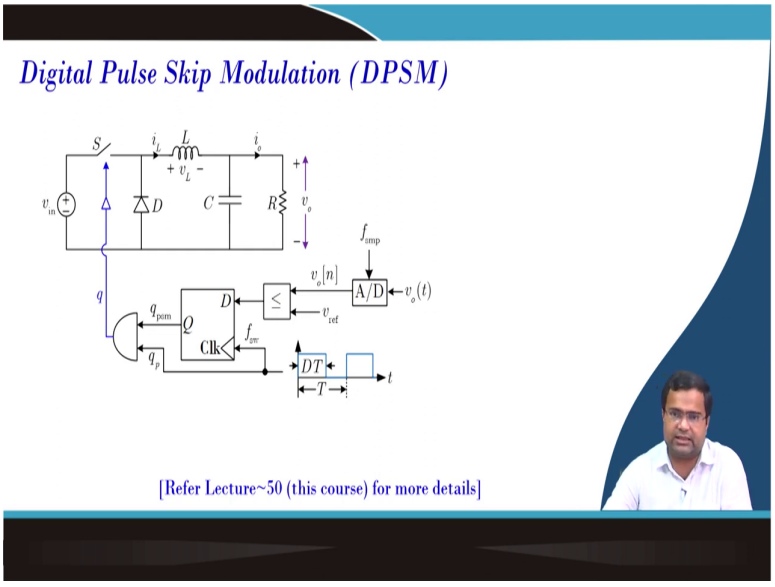

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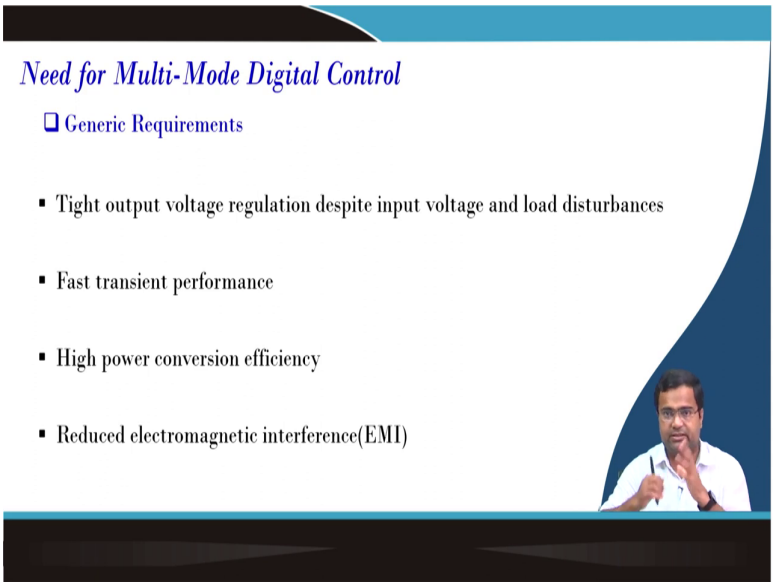

And we have also discussed digital pulse skipping control pulse skip modulation in lecture number 50 we are not going to repeat. And now what is the need for multi-mode control? Some of the generic requirements include a tight voltage regulation when there is a change in input voltage or load current, then we need to achieve very fast transient response, we need to achieve very high power conversion efficiency and then we need to also reduce EMI; that means, these are the generic objective.

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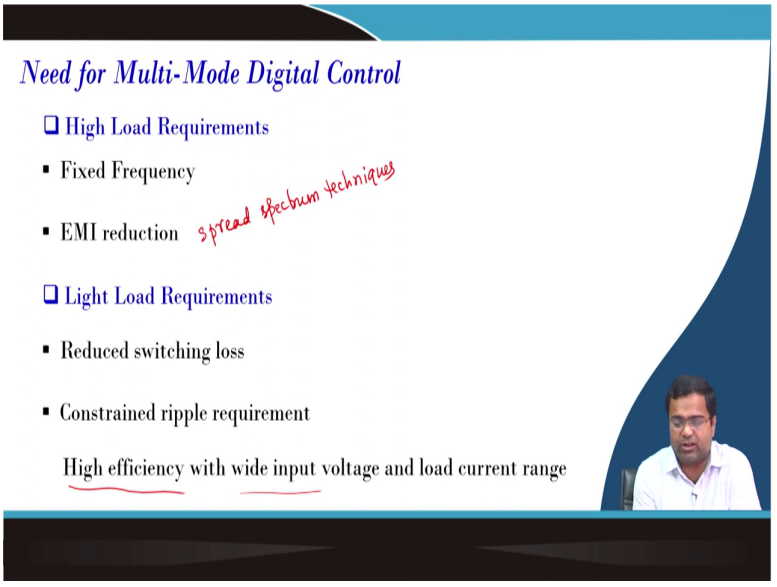

And if you go for high load current then we need to achieve most of the commercial required products requiring some fixed frequency because of some filter design aspect point of view. And we also want to achieve some EMI reduction or spectral space spread spectrum technique. So, this is linked with some spread spectrum technique and then light load requirement we want to reduce switching loss, then we want to also consider the constraint in the ripple voltage it should not exceed too much it should be within the limit.

And finally, for all cases particularly in light load also we need to achieve high efficiency with wide input voltage and load current range.

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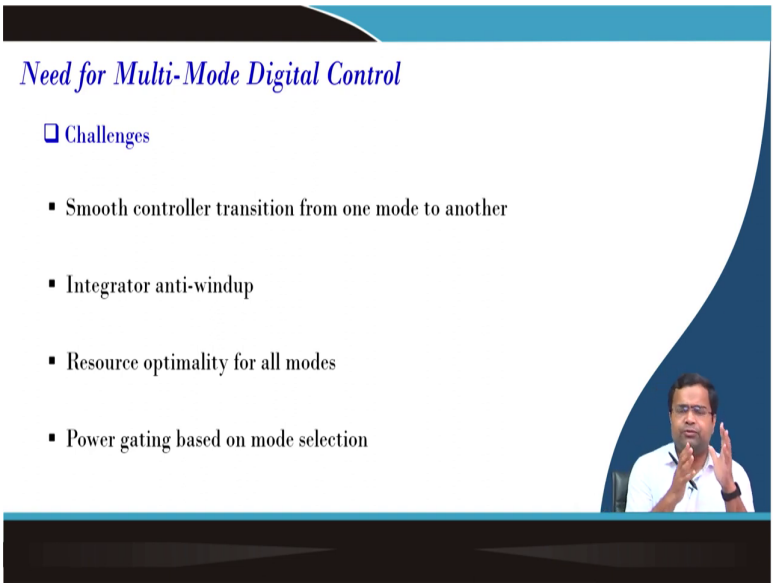

So, now what are the difficulties? The challenges are how to achieve smooth controller transition suppose we are using a PWM and PSM or PWM or PFM, and how to make sure to have a smooth transition between PFM and PWM like that.

Next how to avoid integrator windup? Suppose you are operating PFM or PSM, but you have a PWM running in the background let us say and there is an integrator. Then there is a possibility of an integrator windup problem. Similarly, if you are going from PSM to PWM. So, at that time also the error can be large and that may cause the integrator to wind up with the problem.

So, you need to make some anti-windup arrangements for the integrator. Then we need to optimize the resources. Because if there are the two-three controllers and each controller if

each controller requires dedicated resources then the resource requirement will go up and that may require more silicon area, more power consumption, and more cost. So, we need to keep in mind the resource constraint.

And finally, we need can do power gating. Suppose we are using PWM and PSM if you are operating at a light load condition when the power output is already low. So, we need to save battery power. So, that time we should not burn power because we should not activate the PWM mode it should be disabled; which means, we can say power because it is operating under PSM. So, this power gating is possible based on mode selection.

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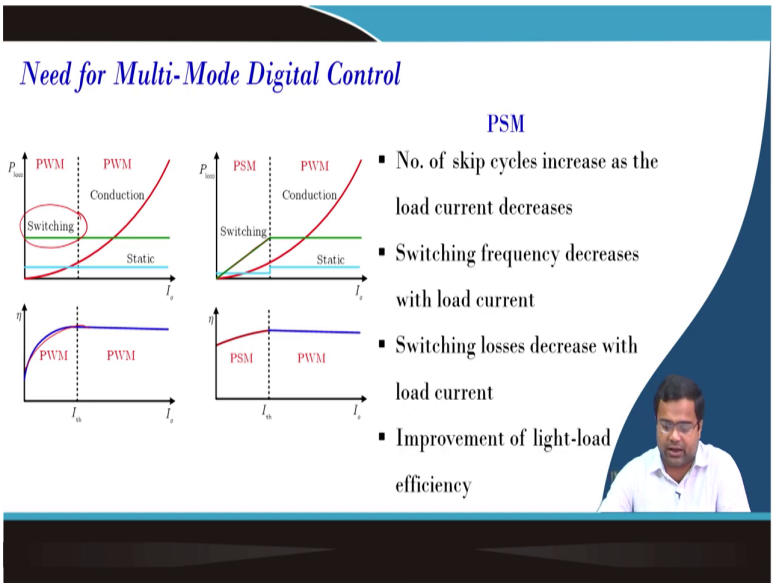

So, let us consider if we are operating in PWM and if you operate continuously PWM then the switching loss which is mainly the driver loss that will remain fixed. So, as a result, the losses component of some static loss will be fixed. So, if you continue to operate in PWM there will be a drastic reduction in efficiency and that is not desirable.

But if we use a PSM then the switching frequency is getting reduced because the pulse skipping the number of skip cycles is increasing or you can use PFM also. That way your static loss is also getting reduced. So, you can save power and you can improve efficiency.

So, if you use PSM the number of skip cycles increases as the load current decreases. Then the switching frequency decreases effectively with the load current and the switching loss decreases with the load current and we can improve the light load deficiency.

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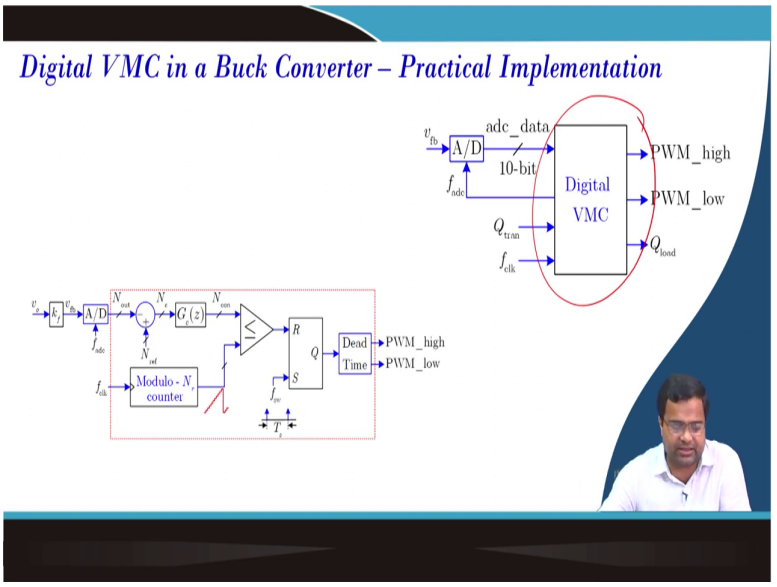

Then how to make the practical implementation of this multi-mode control? So, we can start with the digital PWM that we have discussed in sufficient detail I think in lecture week 8, week 9 week 8, and week 10 we have discussed it in sufficient detail.

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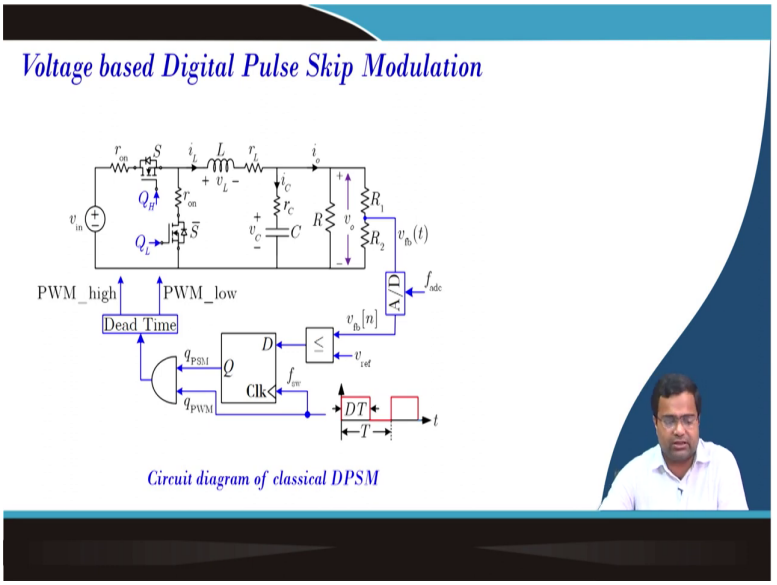

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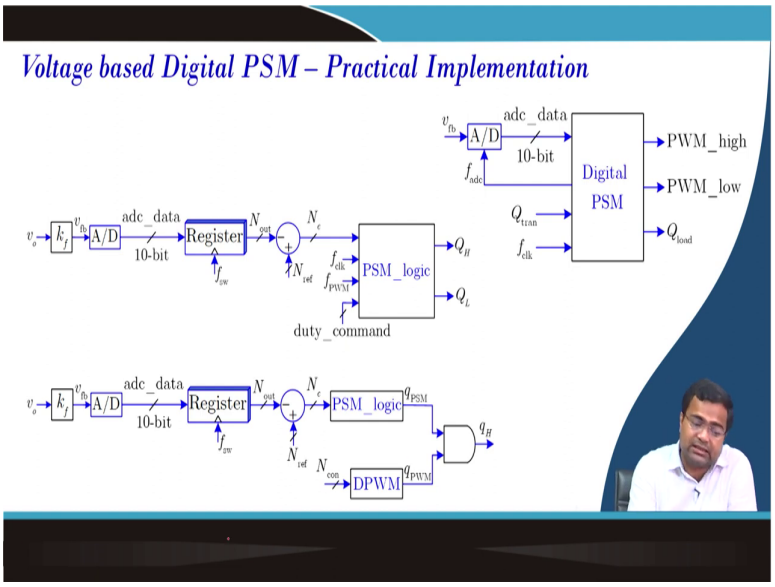

Then we also discussed digital pulse skipping modulation which is the basic architecture. Then how to implement digital pulse skipping that also we have discussed in sufficient detail because there is a PSM logic DPWM logic. So, this whole thing can be enabled to make this multimode control.

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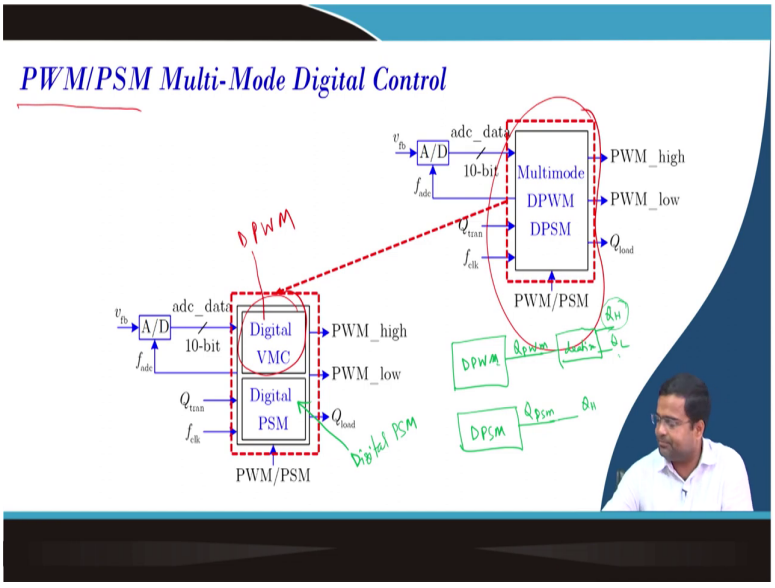

Suppose we want to design a PWM PSM multi-mode control. So, this is our overall block and in the subsequent lecture we are going to consider this multimode control with the Verilog implementation program also we are going to do this, but let us take we want to

implement this PWM MPa. So, if you go inside, then this consist of digital voltage mode that is your PWM this is like your PWM DPWM. And this part is your digital PSM.

So, what do you have to do? Both of them will generate a gate signal; that means, digital let us say if it is a DPWM. So, it will generate a QPWM and if it is a digital PSM, DPWM let us say it is generating a QPSM.

So, how to get a gate signal? So, for this case, we will use a dead time circuit. Because to generate Q H and Q L and this will be standard Q H. So, your effective high side gate signal can be taken as Q H for this case if you use DPWM or it can be marked with this PSM and Q L either can be taken from dead time for synchronous complication or it can be set to 0 for DCM.

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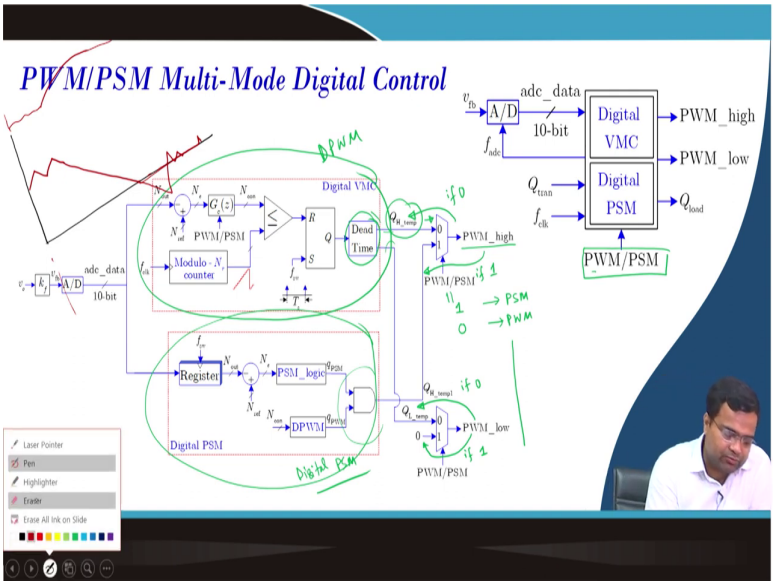

So, this can be done and this is something similar; that means, this block is DPWM this is your DPWM. If you say this output is coming from a dead time circuit and it has a high and low and we are calling a temporary then there is an earmark if this signal is selected as 1 then it will take PSM. If it is 0 then it will take PWM.

And you see when it is 0; that means, it is taking this channel. So, your high side gate signal will be simply connected to the dead time output, the output of the dead time circuit related to the DPWM clock for the high pulse. And if it is 1, 0 you see your low pulse will be taken to the dead time circuit output which is a low side pulse.

But suppose if it is 1, then this will be connected to this if 1 it is if it is 0. If 0 and this will be simply connected to this one if it is 1 and this is nothing, but the PSM. And this block we have implemented is our digital PSM. And this circuit we are going to implement this in the subsequent lecture in Verilog and we want also first want to synthesize it and then we want to implement using an FPGA prototype.

So, this is one example of multi-mode control where you can make an external assessment; that means, I want to enable either PWM or PSM. So, that is the user's choice because sometimes what happens? Suppose we are talking about a load transient response. So, let us consider a scenario where the converter is undergoing a load transient response.

So, it was under high load conditions suppose it has undergone a load transient response. So, if you use PWM let us say directly go to DCM, then what will happen? If you draw the if you draw corresponding output voltage waveform. So, this time to this point there will be a large overshoot it will remain.

So, one way to cut down the overshoot you may enable this and then come back and then go to your DCM operation. So, there whenever we will consider this case study we will discuss it in detail. So, maybe we will wait for this case study to come, and then we can show what is the effect that is coming. So, for the time being, we are only giving the concept of the PWM, and PSM. So, this is just a select line either it will take PWM or PSM.

But here there is still further scope for optimization because if you use a common DPWM block, let us say we will show it may be needed here. So, you can minimize (Refer Time: 09:54), but the control part is something that must be there for normal PWM and this will be replaced by a constant voltage for this. And we will try to optimize some aspects in the subsequent lecture on Verilog implementation.

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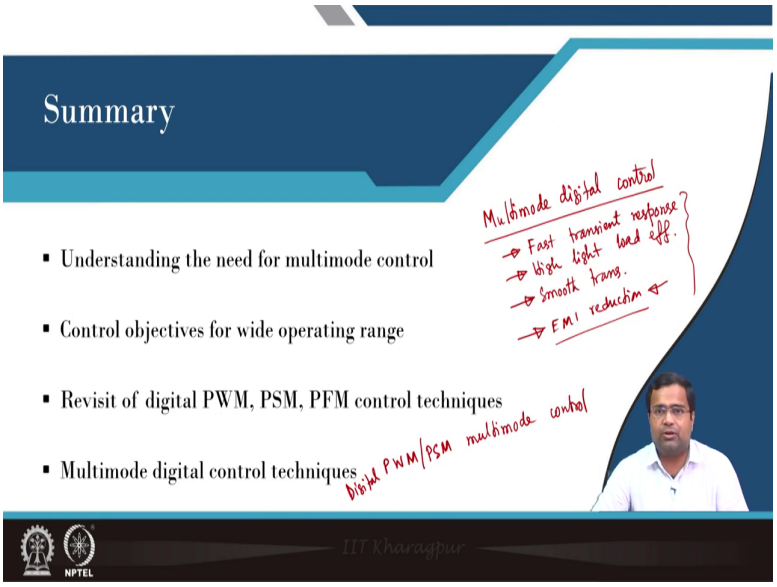

So, in summary, we have discussed the need for multi-mode control, we have discussed control objectives for a wide operating range and we have revisited some digital architecture that we already presented for digital PWM, digital PSM, and digital PFM control technique and we have discussed PWM, PFM, PWM, PFA, PSM the digital; that means, that digital multi-mode control that we have just block diagram, we have discussed.

So, in the subsequent lecture, we are also going to consider what is called EMI reduction, or spectral spreading as another feature. So, in the multi-mode, what will be our objective? In the subsequent week, we are we will be taking multi-mode digital control. So, what will be our objective? Your objective gate is a fast transient response, high light load efficiency, smooth transition, and also EMI reduction.

So, this feature we have not yet discussed. So, first, we will explore this feature, and then we want to incorporate all these to come up with a multi-mode control technique in the subsequent lecture. And we will also want to write Verilog programming as well as we want to implement using an FPGA device that is it for today.

Thank you very much.