Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 02
Fixed and Variable Frequency Digital Control Architectures
Lecture - 11
Basics of Sampling under Fixed and Variable Frequency Modulation

Welcome. So, in this lecture, we are going to talk about some Basics of Sampling under Fixed and Variable Frequency Modulation in Switch Mode Power Converter.

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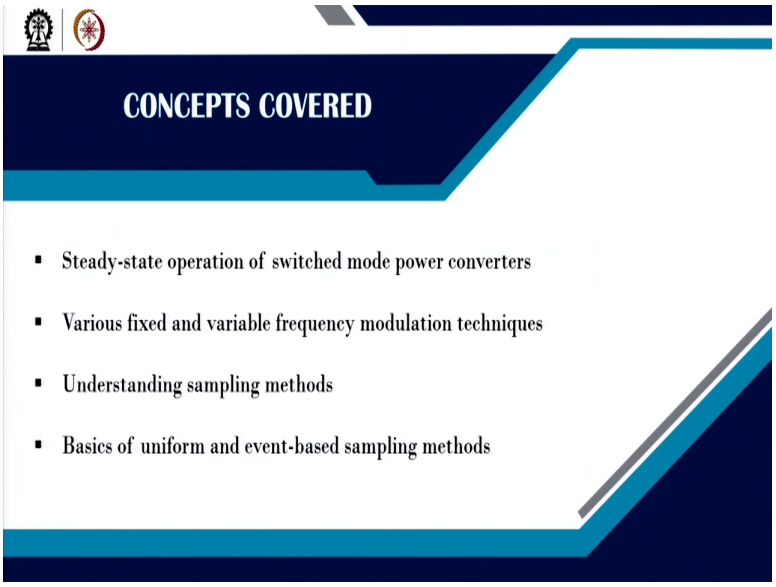

So, in this lecture you know we want to show the steady-state operation of the switch mode power converter, primarily we will focus on the buck converter as well as the boost converter. Then we will discuss various fixed and variable frequency modulation techniques. And then understanding the sampling method, how do you know if you want to sample a particular signal?

Let us say we want to sample the output voltage and when the converter is running under let us say fixed frequency modulation then how to sample and where to sample what should be the sampling rate. Similarly, when it runs under variable frequency operation then how to sample?

So, this basic concept will be discussed in this lecture. So, this will you know to create a path. So, that the next lecture we can go deeper into the actual control architecture and then the basics of uniform event base sampling.

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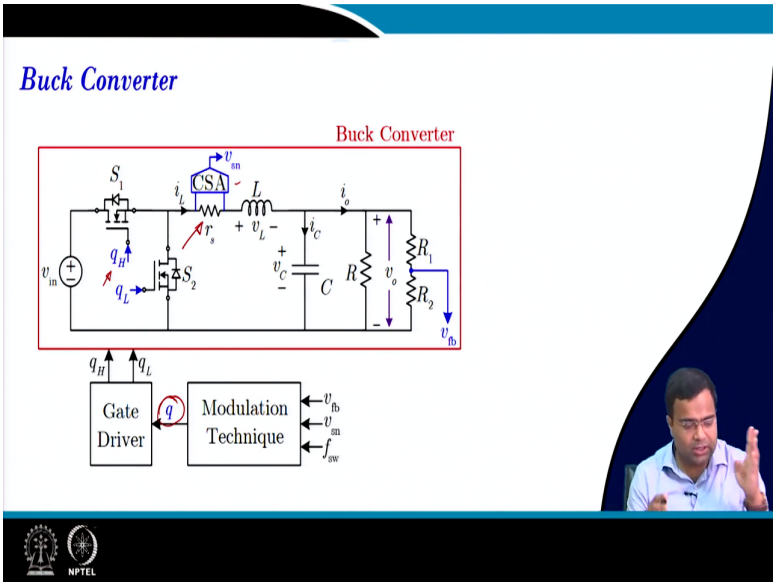

So, first, we will consider the DC-DC buck converter and in this converter, it is a more or less realistic buck converter with you know sorry it is an ideal buck converter, and here we are sensing the sense resistor; that means, current inductor current through a sense resistance RS and there is a current sense amplifier.

So, we may or may not use this current feedback in actual control implementation, but in this lecture, we want to show if, suppose it is a buck ideal buck converter then this q H is nothing but the same as q this gate signal and q L is just the complement of q. But in a practical buck converter or any DC-DC converter, we need to consider some dead time.

That means, then there should be a gap time difference between the turn off of this low side fet and turning on the high side felt there should be some difference in time otherwise there will be shoot through operation and it may short the supply to the ground.

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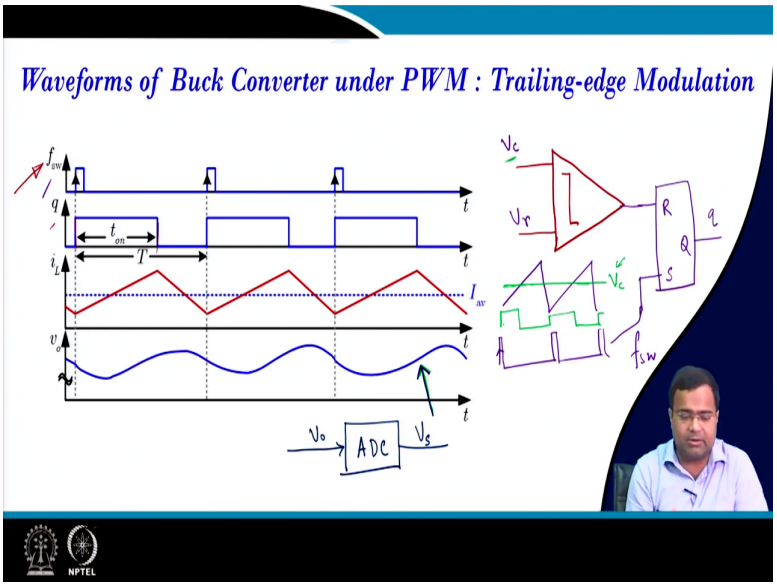

Now, to start with let us consider that under trailing edge modulation. That means, what is trailing edge modulation? The trailing edge modulation, means we generally turn on the converter this is an external switching clock fsw and this will decide the switching frequency of the converter.

Then the q which is the gate signal will be turned on or it will go high when the rising of the clock comes and it will be turned off. So, suppose we use a fixed duration. So, how do I generate this signal one way you can very easily generate suppose you consider a comparator ok and there are two inputs to the comparator, and if you take here a shorter waveform like this.

And here if you take a control voltage VC and this is a ramp signal and this control voltage can be a number and then you can add an RS flip flop R and S Q this is your gate signal. And this one supposes if sync with the switching frequency clock. So, this is my this signal; that means, this is my new clock which is shown here.

So, now, here if we use this control voltage let us say we are talking about this is my control voltage which is my v c. So, naturally, this will you know and this will generate this on-time like this. So, in that way, we can generate this on time. So, here it is an open loop; that means, we can provide a fixed voltage and we can compare the shorter waveform to generate the on-time of this and this is under pulse width modulation.

Next question I want to discretize this signal output voltage signal ok. So, I want to pass through; that means, we need to pass through an A to D converter; which means, this is my v 0. So, I want to pass this v 0 to an A to D converter. Initially, I am not considering you know it is like sample voltage.

Initially, I am not considering the quantization effect I am assuming that the quantization effect is neglected, I am just talking about the sample signal. That means, what should it look like? So, let us say here again the same waveform, but now we are sampling this voltage once per switching cycle.

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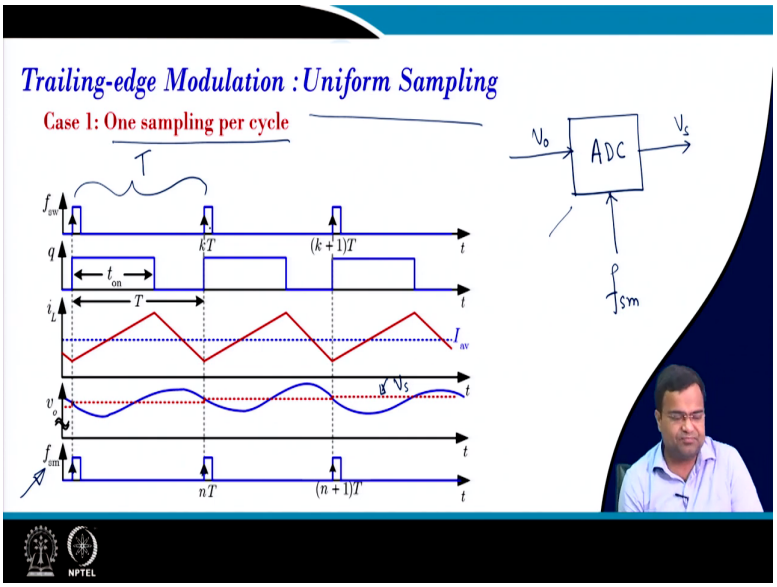

Because there is a switching cycle this is the duration of the switching cycle and the period is T. So, we are uniformly sampling because this is under uniform sampling we are sampling once per switching cycle using a fixed frequency clock. So, you can see this is a sampling clock; that means if we consider an A to D converter ADC and this is my analog output voltage and this red dotted one lets us say it is the sample voltage.

So, this ADC requires a clock and which is my fsm ok. So, this is a sampling clock. So, here is the clock edge at the edge of this sampling clock you will capture a sample. Now here I am talking about the ideal sampler, but practically there will be a delay because every ADC should have some conversion time. So, here if we sample the voltage then it will sample like this; that means, it will be a zero-order hold effect; that means, after sampling A to D converter will also have a register.

So, it will hold value. So, it will behave like a zero-order hold and it will again update when the next sampling edge comes. Here we are sampling the signal it is a periodic signal and we are sampling in synchronism with the switching clock at the same edge. So, you can see that voltage is getting updated at this edge and which is also the switching frequency clock edge.

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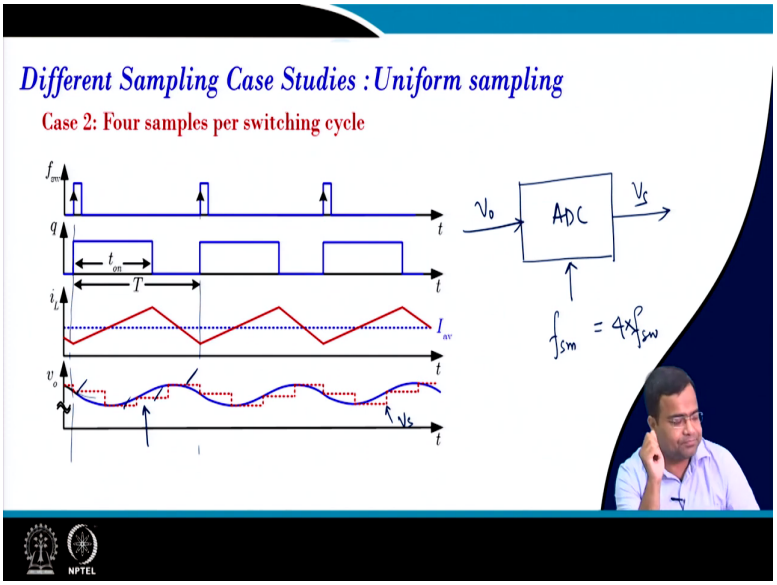

But earlier we took only one sample per cycle, but you can also increase higher sampling rate if you increase the sampling rate. So, high eventually it will become like a continuous-time signal. So, if you keep on increasing you take 10000 cycles and 10000 samples per cycle it will almost behave like a continuous-time signal. That means inter-sample duration is very very small.

So, here I am just showing a four sample case where in between two edges; that means, you know this is the switching clock edge and this edge. So, you can get one two three four you are updating four times. So, it is four samples per cycle.

Now you may ask; that means if we use again this ADC and this is again your v 0 and this is your v sample again this is my v sample. So, this f sm if you take the frequency it is like four times f SW the switching frequency.

Now, the question is whether we should choose four-time should we choose 5 times, 10 times, 1 time or can we go even fraction; that means, we can take 1 per 5 cycles is it possible. So, this thing we will discuss is when the architecture will come because you will see in

digital control under steady-state that the control variable which is coming out of the controller we have not yet started that. It will become a fixed number.

So, if it is a fixed number and if there is no change in the output voltage, and if there is no change in the control output then I can say why should I sample. So, I can just keep watching the digital ADC and I can even not sample at all it will behave like an open loop system. So, in that case, we can reduce the sampling rate just to save power; that means, we are taking the sample, but we are not computing the digital controller we were just keeping it idle and holding the value.

So; that means, there are many possibilities that we can discuss. So, four samples are one case study where the sample rate can be higher than the switching rate, but whether it is desirable or not. So, we will show some MATLAB case study in going forward. So, what can be the implication in the stability when such four samples are considered you will find there can be any small deviation in the duty ratio.

It may lead to a high periodic non-linear behavior, because of this multi-sample. But generally, the multi-sample since you are taking more number of sample, naturally the voltage update rate is high. So, you can reduce the delay so; which means, this multi-sample can be helpful to reduce delay loop delay. But at the cost of more powerful processing and all and there are many research papers on how to even interpolate the intermediate information.

Because you are not getting the information between this and this point. So, you can interpolate, so this possibility can be there so, but we are not going into detail we are just you know throwing. So, that you can think about this whether it is possible to 4 or 5 we will discuss when we consider the MATLAB study.

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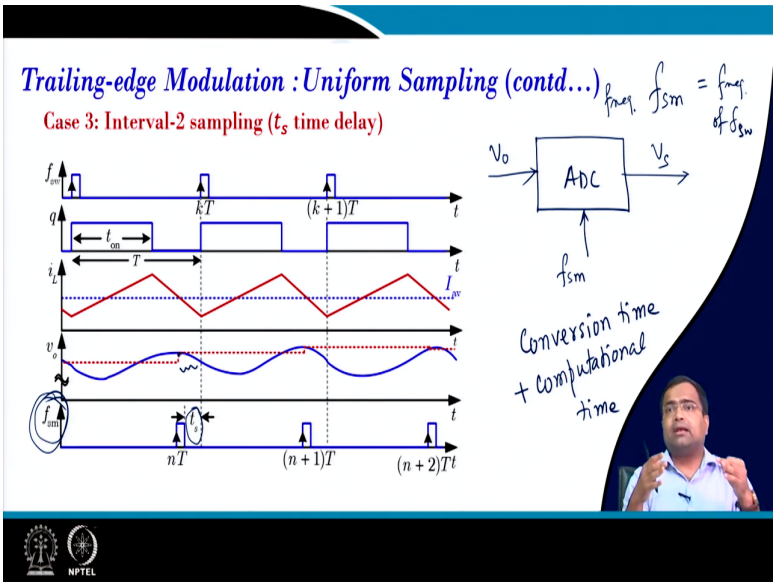

Next, but as I said the delay; means, if you consider a simple ADC A to D converter which is my v 0 and this is my v sample.

And this is my sampling clock this one is now I 1 you can see here as if we are providing the sampling clock here, why? Because we are still not considering the delay of the conversion we are just showing the sampling clock. It is just for the concept because here we are using the sampling frequency and the switching frequency the same.

They are the same, but there is a time shift. That means, sampling is occurring earlier than the switching event takes place, why you are showing that? Why not same time? Now, what is the problem with the same time we will see in the subsequent lecture, that you will have some time required some time for the conversion? That means, an ADC DC requires some conversion time right conversion time this is for the ADC plus you also need some computational time for the digital controller.

And this delay which is t s delay this delay is provided to accommodate the total conversion time. So, your actual control voltage or control current whatever architecture we take should be available. That means, sending the command to the ADC for getting the sample at this point, but the actual sample may be available after some delay.

And then taking into account the controller computation your actual reference current for the current mode control or the voltage for the voltage mode the actual control voltage may be

available after some time. So, taking that into account we need to play with this sampling clock; that means, this sampling clock is the frequency wise the sampling clock the frequency if you take the frequency.

It is the same as the frequency of f SW, but there is a time shift and we have to play with this time shift to accommodate this practical delay this time ship will introduce this delay which can vary. If you are going for low power it may so happen because we need to save efficiency this delay can be a few switching cycles, or it can be more than one switching cycle.

And there are different kinds of hardware, as well as software control architecture. For hardware control if you go for ASIC you may try to reduce the delay by optimizing the hardware, but when you are talking about a digital system solution. Suppose, you are using a microcontroller from one vendor then you are using ADC from another vendor, but you need to interface.

So, to make the whole thing you know work taking into account different computational times. Sometimes the software control may take one switching cycle delay and that is exactly what it is the one cycle delay.

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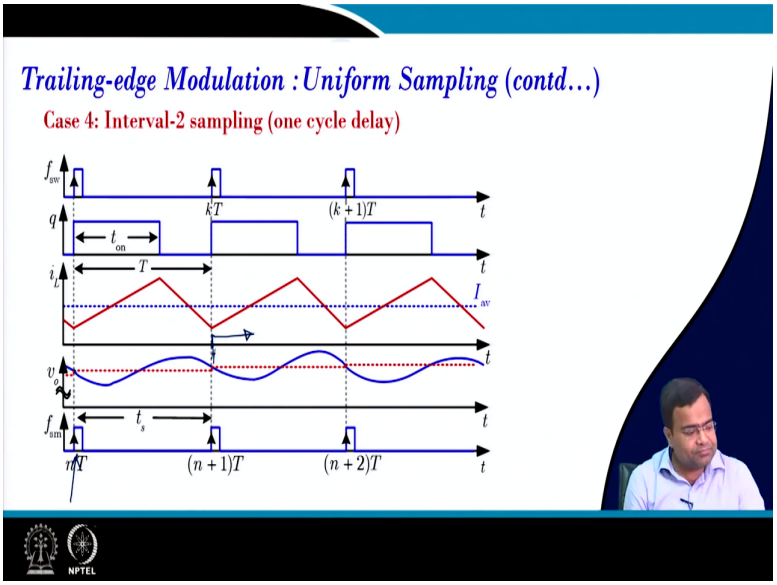

Here you can see the voltage is getting updated, but it will it is you are getting a sample here, but you may use that data in the next cycle. That means, if you take the sample during the nth

switching cycle at the beginning you will need to use the data; that means, the conversion time and computation time.

After that, the data will be ready at this time onward this cycle and that is called one cycle delay. So, unless we close the loop we will not see the effect of one cycle here as if we are just showing the sample version, but we have to use this sample information in the controller then only we will get the full picture of the one cycle delay. But the bottom line is this one-cycle delay is used to accommodate sufficiently accommodate the conversion time and the computational time.

But this will also penalize in terms of loop delay, this will penalize heavily in terms of non-linear phenomena and we need to tackle how to make sure your design can make you can make your design stable even with this delay. And then what could be the alternative arrangement even with this delay because you may not need a very fast ADC one possibility you may increase the sampling rate when there is a transient or you may create an additional path to bypass to avoid such a large delay during a large time gap.

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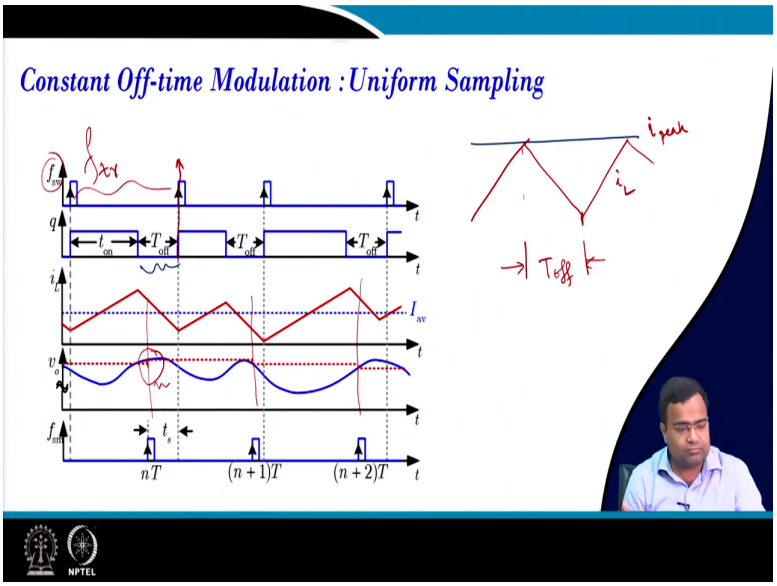

So, many possibilities exist now coming back to constant off-time modulation where the off-time is constant, but on-time will vary because we have learned this thing on-time varies based on the feedback comparator. So, that means feedback means constant of time means generally if we implement a peak current mode control version of the constant on-time inductor current is rising and then it is falling rising-falling.

So, you see this is my off-time; that means, this is this duration is my T off and if we keep the off-time constant then once the off-time is elapsed, we generally implement using a monoshot timer. And in this course, we will implement this monoshot timer using SDL code it will be very interesting it will be a counter-based approach. So, we can implement once this timer is elapsed then your switch turns on.

And switch will continue to turn on and remain turned on until this inductor current hit the peak current limit this is my peak current limit and this is my inductor current. Once it hit the peak current again switch turns off and it again the monoshot timer is activated. Now since this is a variable frequency modulation because your off-time is constant, the on-time will vary based on the variation in the initial condition variation in the peak reference or any disturbance.

How to sample because the period can vary even with a small perturbation the time period can vary. If you use uniform sampling then you see some sometimes sampling can happen here, sometimes the sampling can happen close, sometimes sampling can happen here. So that means, the duration between the sampling point and the turn-on-time that will differ.

Because there is a mismatch between the sampling instant and the switching instant. It is natural because you are using a fixed frequency sampling clock where your switching clock is whatever I will not say switching clock. Because there is no switching clock, it is a trigger clock, I will say trigger clock because this trigger clock is enabled once the off-time is elapsed. That means, once the timer completes the timing then this trigger pulse comes.

So, this trigger pulse is it is an event it is not associated with any fixed frequency synchronized clock. But now the question is if this time period varies then a fixed sampling rate naturally there will be always a mismatch between the timing; that means, the sampling timing and the switching period. Sampling period and the switching period there will be always variations and we will see such control when you implement it in MATLAB.

It will lead to something called multiple limit cycle oscillation and that is not desirable, because there will always mismatch in the timing. But how do reduce that effect one way you can have a very high sampling rate so that you can effectively reduce the time, and commercial product use that ok.

They use an over-sampling for constant off-time or off-time, but you are essentially increasing the sampling rate means your computational rate is also increasing.

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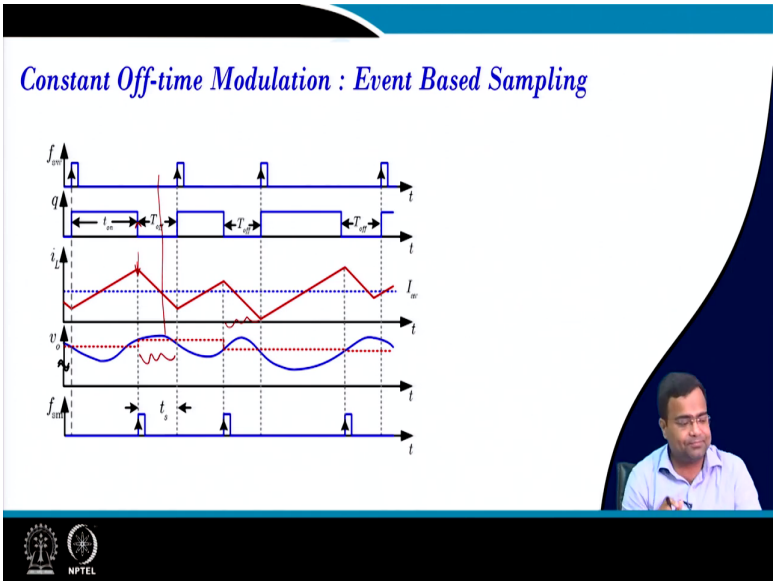

So, your power consumption will increase to do that, there is a way to avoid it called event-based sampling.

So, instead of using a fixed frequency clock you can detect an event and this is an ideal conditional drawing. So, the event will be triggered once you know either once the off-time is; that means when the starting of the off-time or it can be even taken at the end of the off-time. That means, we can associate this event with the timer either activation or deactivation.

That means activation means when the timer is enabled monoshot timer or when it is your counting is over or it can be in between anywhere. And you may ask what will happen first of all you cannot exactly take the sample right at the point of switching because that will introduce a lot of noise. So, you should avoid that switching, so you need to shift the sampling rate and we will discuss this practical aspect in the subsequent architecture.

Then the next question is what will be the impact of stability. So, we have not gone to that level and we may not discuss many stability aspects in this course, but we want to give you some basic thought, particularly we want to highlight the fixed frequency modulation. If one understands thoroughly then he may try for the variable frequency for going into detail ok.

So, event-based sampling will synchronize with the event rather than time. So, you will eventually get one sample per cycle and you can see always there is a fixed interval between the sampling point and the on-pulse trigger pulse. So, the delay will be fixed because you are taking concerning the event.

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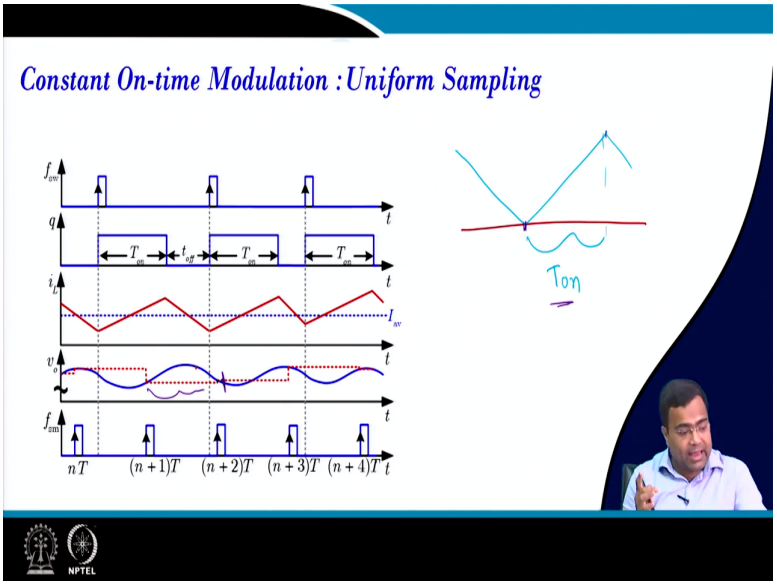

Similarly, if we talk about constant on-time where the on-time is fixed, but off-time varies based on. Because if you take the valley current mode control, and this is a very very popular method for commercial products ok.

So, here this time is fixed this time is on-time this is fixed and originally take the sample where you should take it, we can take a sample here or a sample here. So, if you use uniform sampling then you can see this is the duration between intervals and here it is sampling.

So; that means, sometimes it is sampling the on-time it is sampling at the off-time the duration between the sampling point and the switching point varying. So, naturally, this will lead to multiple limit cycle oscillation.

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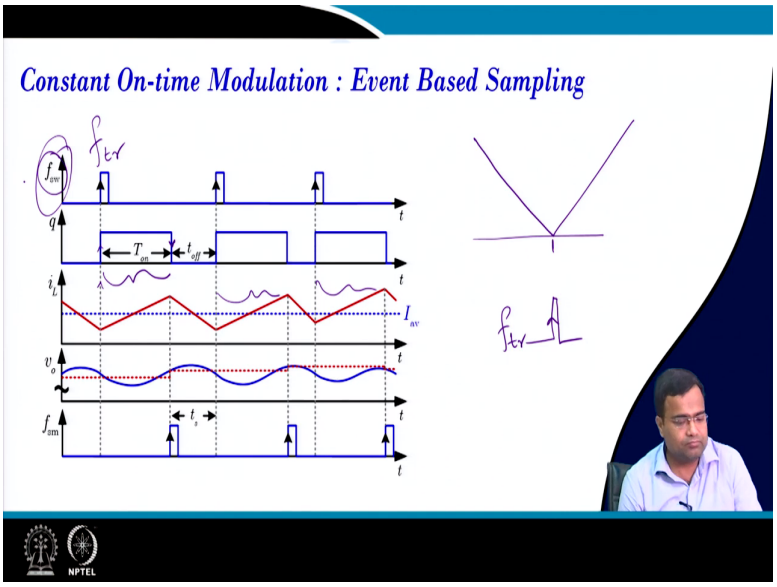

But again to stabilize you we can synchronize with the timer; that means, here we are taking the sample when the timer finishes the counting, so it is synchronized.

For the other case also we could take when the timer is enabled or disabled, but we need to check which one is best in terms of stability point of view ok. So, this is like a constant on-time it is event-based sampling. So, by taking the right event we can in this case since you are taking the sample after the one time is elapsed. So, you see this difference; that means, the difference between the turning on of the switch and the sampling point is always constant.

So, this is the event that we have selected if you select this event also so, they are synchronized with this clock trigger clock. So, again this is not a switching clock it is a trigger clock because this trigger clock is enabled when the monoshot timer is enabled. That means when the current will touch the valley currently, this is the event that will generate this trigger pulse. This trigger pulse will be enabled here, so this trigger pulse.

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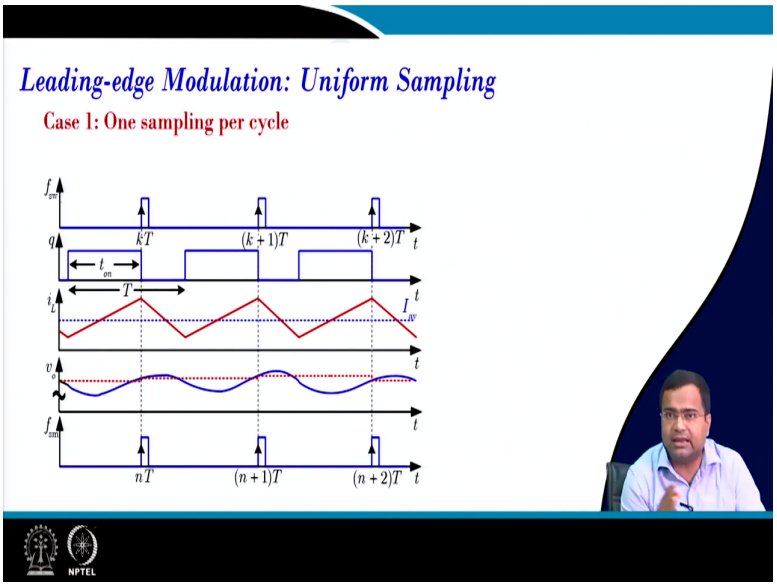

Leading edge modulation we have discussed trailing edge modulation, leading-edge what happens? Generally, at the rising edge of the switching clock, we turn off the switch. And our valley current mode control is a good example of leading-edge modulation and for leading-edge modulation again if you take one sample per cycle you can take the sample right when the switch is getting turned off ok.

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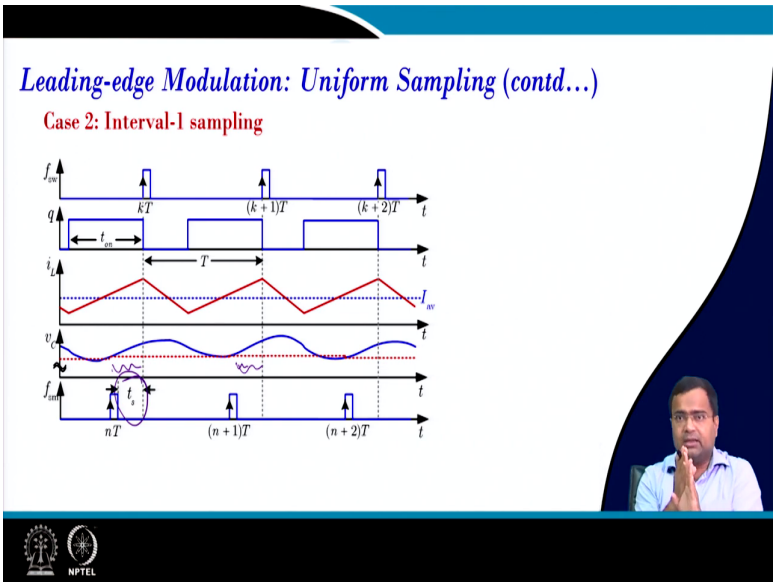

And again you can insert a delay ok interval one sampling. So, you can insert a delay. So, here we talk to call it an interval one sampling. So, this delay is inserted; that means, we have

inserted a delay this is to accommodate the conversion and the computational time and we will go for a practical converter example then we will be very clear. But in this lecture, we are emphasizing the typical waveform the voltage, and where to sample.

So, it is equally important the rate of sampling as well as the timing of sampling is very important and that will affect in terms of regulation terms of stability in many aspects will come.

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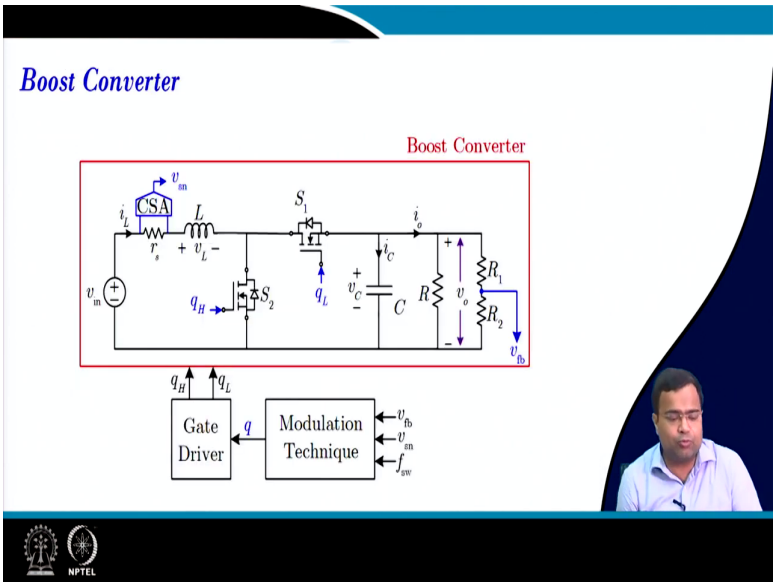

Then you take a boost converter.

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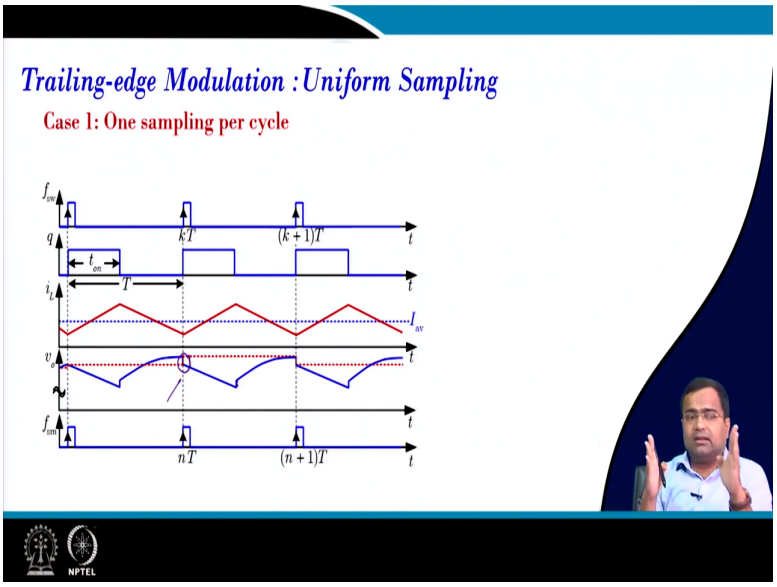

If you take a boost converter trailing edge modulation. So, ideally, if you sample at this point then this is a practical boost converter. Now the practical boost converter has an ESR jump. So, it is not recommended that you take the sample here, but it is just for starting the concept we are taking one sample per cycle.

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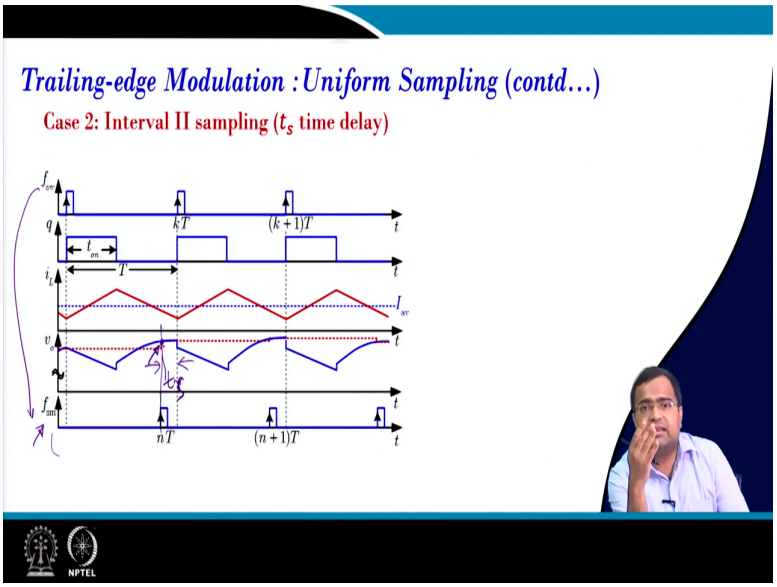

But practically you should introduce a delay; that means, you should take the sample earlier than switch turns off. That means, before the switch turns off we should introduce a delay and this delay can be easily inserted in your SDL code because you will have a fixed period.

And after this time period every time you actually; that means, you have to create this sampling clock and you need to create a phase shift, time shift concerning the switching clock and then you can just send the comment. So, this clock will be sent to your A to D converter and then after this time of you know delay time this is a t s delay time t s delay time, you can it should complete both conversion of the ADC as well as the computational time.

So, that is why we have to vary the delay based on what sampling you are using. What is the conversion time? And the conversion time of the ADC also varies based on the architecture of the ADC. If you are using pipeline ADC then the conversion time depends on the number of pipeline cycles. If you are using flash ADC it is very simple, but it is rarely used in a commercial product, because of a high resource cost right, which means the cost is high.

Or you can use simply successive approximation ADC. So, there are many architectures of ADC, but the only thing we need to know there should be sufficient sampling delay. So, that it can compute the conversion as well as the computation in the digital controller. Another interesting point in the boost converter is if you take the sample here the boost converter suffers from the right (Refer Time: 25:43) 0.

So, should we take the sample point at the peak voltage or the valley voltage that may slightly affect the (Refer Time: 25:51) effect there are research papers on this. But we are not going to discuss when we come to boost converter this current mode sampling we will discuss some aspects there. But the selection of the sampling point is also very important for a boost converter in terms of its small signal performance as well as in terms of the first scale stability.

And what do you mean by first scale stability that we will discuss when we go to mathematical modeling I will show in subsequent lectures some MATLAB simulation case studies, to give you an idea of what you mean by first case stability.

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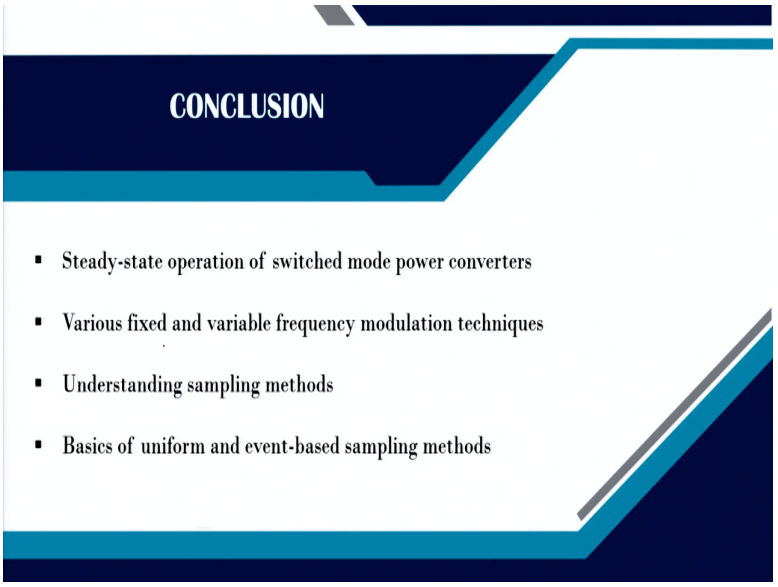

So, in summary, we have shown the steady-state operation of a switch mode power converter, and various fixed frequency and variable frequency modulation techniques are discussed.

We have shown some basic sampling mechanisms whether it is a uniform sampling or event base sampling, then where should we sample because you need to accommodate the delay for the conversion and computation time? Then we have also discussed some uniform and event-based sampling methods. So, in the coming lecture, we will be talking about how can we incorporate this and come up with the architecture.

Today I think we got some basic idea about the sampling mechanism, that is it for today.

Thank you very much.