Digital Control in Switched Mode Power Converters and FPGA-based Prototyping Dr. Santanu Kapat Department of Electrical Engineering Indian Institute of Technology, Kharagpur

Module - 11 Design and Validation Case Studies using Digital Voltage and Current Mode Control Lecture - 107 Hardware Case Studies and Transient Performance in a Digital CMC Buck Converter

Welcome. So, this is the continuation of the previous class here we are going to demonstrate a Hardware Case Study for and Transient Performance of a Mixed Signal Digital Current Mode Control Buck Converter.

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| CO | NCEPTS COVERED |
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| | |
| Design case | studies of mixed-signal CMC buck converter |
| Experiment | al load transient performance |
| Experiment | al reference transient performance |
| | |

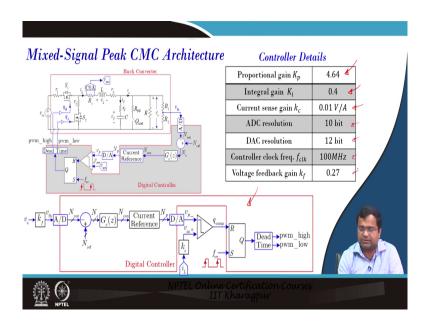
So, we will be talking about you know we have already considered a design case study of mixed-signal current mode control. We will show experimental load transient as well as reference transient performance.

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| $\frac{\left[\begin{array}{c} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 $ | nal Peak CMC Architecture | |
|--|---|--------|
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | $\frac{SA}{L} \begin{bmatrix} r_i & i \\ r_i & \cdots & i \\ r_i & \cdots & r_i \end{bmatrix} + \uparrow$ Inductance L 1.8 | ιH |
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| $\begin{array}{c c c c c c }\hline \hline & & & & & & & & & & & & & & & & & &$ | $ \underbrace{\mathcal{Q}_{int}}_{-} \underbrace{\mathcal{Q}_{int}}_{+} \underbrace{\mathcal{Q}_{in}}_{+} \underbrace{\mathcal{Q}_{int}}_{+} \underbrace{\mathbf{Input Voltage } V_{in}}_{+} 3.1 $ | V |
| Load resistance (R_c, R_{sw}) (13.5 Ω , 0.33 Ω) | $\underbrace{V_{ref}}_{ref} = V_{ref} \varepsilon [1]$ | 1.1] |
| | $\frac{v_{s}}{v_{s}} \frac{D_{A}}{D_{A}} \frac{f_{s}}{v_{s}} \frac{G_{z}}{V_{s}} \frac{N_{r}}{G_{z}}$ Switching Frequency f_{sw} 200 | Hz |
| | | 0.33Ω) |
| | | |

So, again we have discussed mixed signal peak current mode control architecture multiple times and this is a power stage that we are going to consider.

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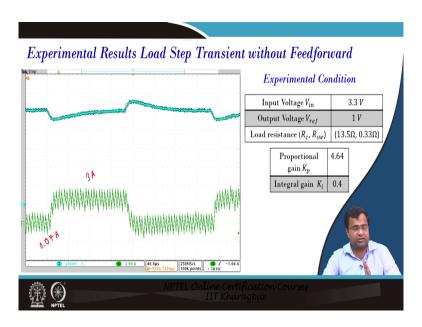


And here we are we have designed this thing using FPGA. These things are also discussed and we have also discussed that proportional gain we are going to consider 4.64 and integral gain is 4.4 that will be plugged into the FPGA. And we have also discussed the current sense gain ADC resolution, DAC resolution, controller gain, and voltage feedback gain. (Refer Slide Time: 01:18)

| Digital PI Controller Ga | ins |
|---|--|
| $\begin{array}{c} c \\ c$ | $\frac{\sum_{k=1}^{N_{w}} \sum_{k=1}^{N_{w}} \sum_{k=1}^{N$ |
| //PI controller gains {parameter K_p=10'sb0100_101000; {parameter K_i=10'sb0_0110011; //Q | |
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Now, we are using a digital PID controller. So, this is our FPGA parameter setting which is nothing, but 4.64 and four-point 0.4.

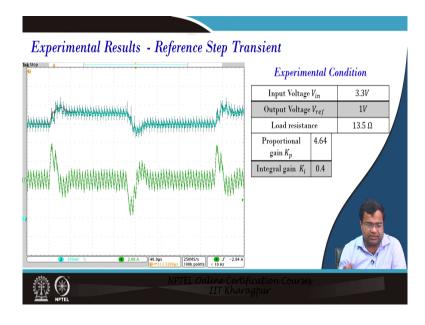
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And now we are going to show experimental results without feed-forward. That means we are also going to consider with and without feed-forward. So, here we are not talking about any load feed-forward term. So, here you can see at 3.3 volt input, 1 volt output we are making a load transient of almost nearly 3 ampere. So, it is changing from 0.07 ampere to roughly 3 ampere load.

So, roughly a three-ampere load step and this is a design based on our criteria which is FSW by 8 you can see it is a faster response than we saw in the last class when you presented the simulation result it is sluggish. Because the current mode control behaves like a fast order system.

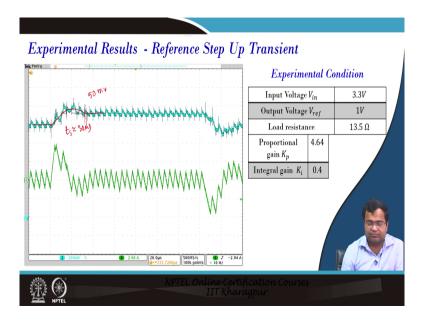
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Then if we talk about the reference transient performance we have seen that it is reasonably good for the reference transient. You can see a slight overshoot there and then the response is settling almost in 40 I mean 30 microseconds.

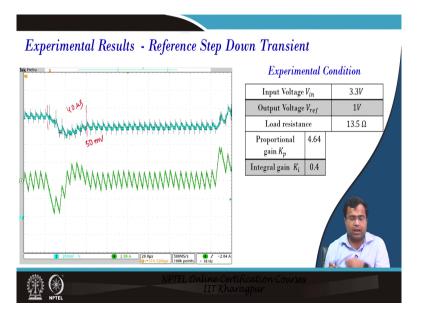
I mean 20 to 30 microsecond which is a few cycles maybe 4, or 5 cycles here time period is 5 micro second. And step-down performance is also nice I mean it is settling in around 30 microsecond with slight undershoot and overshoot for both step-down and step-up consideration.

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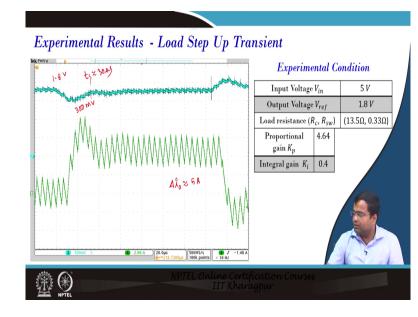


Now, here we are talking about the reference step up transient in the zoom version. So, if you see here the 1 volt is changing to 1.1 volts. If you take the average so here we have not tapped the output voltage right across the capacitor which is why the spikes are coming. Otherwise, the spike will go and you will get a very nice clean waveform here as if this time is roughly around 30 microsecond. So, the settling time is roughly 30 microseconds and there is an additional overshoot of around 50 millivolt ok.

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And if you go to step down transient here to here you will get around I would say 40 micro second is the step-down and on additional overshoot of undershoot of 50 millivolt undershoot ok.



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So, now load step-up transient we are now changing the 5 volt to 1.8. We have kept the same I would say the load resistance and the same PI controller gain. But now the load step here we are making almost like you see it is a 2 ampere. So, 1, 2, 4, 5. So, it is like almost load step size of nearly about 5 ampere load step size and undershoot here it is 1.8 volt and the division is 0.5 volt.

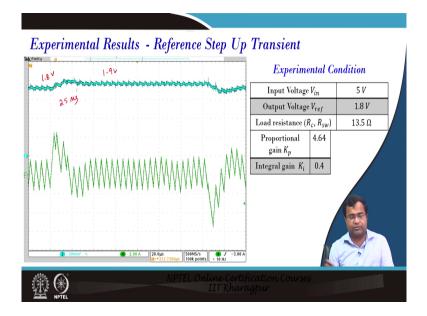
So, we are getting around 30, 300 millivolt; that means, we are getting around roughly 250 to 300 millivolt undershoot, and the settling time here it is coming to be around settling time again 30 microseconds.

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| Experimental Results - Load Step Down T | ransient | |
|--|--|----------------|
| α α <i>γ</i> ση π ^{, γ} | Experimental Co | ondition |
| HARA BRANCHARD ARADINA A HARDINA HARADAN | Input Voltage V_{in} | 5 V |
| | Output Voltage V _{ref} | 1.8 V |
| | Load resistance (R_c, R_{sw}) | (13.5Ω, 0.33Ω) |
| MMM | Proportional 4.64 · gain K _p | |
| N N N | Integral gain <i>K_i</i> 0.4 | |
| | | |
| 2.00 A 2.00 A 2.00 A 2.00 A 2.00 A (10 Hz 151.9200µs (10 Hz (| | AT LE |
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And if we take the zoom step-down version then we are getting an overshoot of 200 millivolt overshoot and the settling time will be almost 30 micro second. So, this is for the design using so it is a sluggish response because we know that current mode control behavbehaves a fast order system and it is for this gain.

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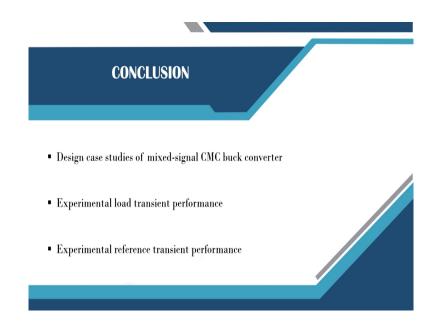
Now, reference steps up transient at 5 volt, now it is the even better response we are changing from 1.8 volt to 1.9 volt. So, it is coming and there is almost very negligible understood

overshoot extra overshoot and the recovery time is coming around 25 micro second, 25 to 30 micro second.

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| K PreVu | · · · · · · · · · · · · · · · · · · · | Experimental C | Condition |
|-----------------------|--|--|-----------|
| 1.9V | .8 v | Input Voltage V _{in} | 5 V |
| - Addite and a second | agaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa | Output Voltage Vref | 1.8 V |
| 20M) | | Load resistance (R_c, R_{sw}) | 13.5 Ω |
| | | $\begin{array}{ c c c }\hline Proportional & 4.64 \\\hline gain K_p & \\\hline Integral gain K_l & 0.4 \\\hline \end{array}$ | |

And if you step down transient if you see the undershoot is insignificant. So, it is 1.9 volt to 1.8 volt and it is coming around 30 microseconds. So, it is a pretty fast transient response for reference step up and step-down transient performance.



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So, in summary, we have discussed the mixed-signal design case study with current mode control and we have discussed the load transient performance. And we have discussed experimental reference transient performance also. So, in the subsequent lecture, we are going to see the effect of load current feed-forward that is it for today.

Thank you very much.