Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 11
Design and Validation Case Studies using Digital Voltage and Current Mode Control
Lecture - 106
Design and Simulation Case Studies in a Mixed-Signal CMC Buck Converter

Welcome. In this course, we are going to talk about the design of mixed-signal current mode control in a buck converter with some simulation MATLAB simulation case studies.

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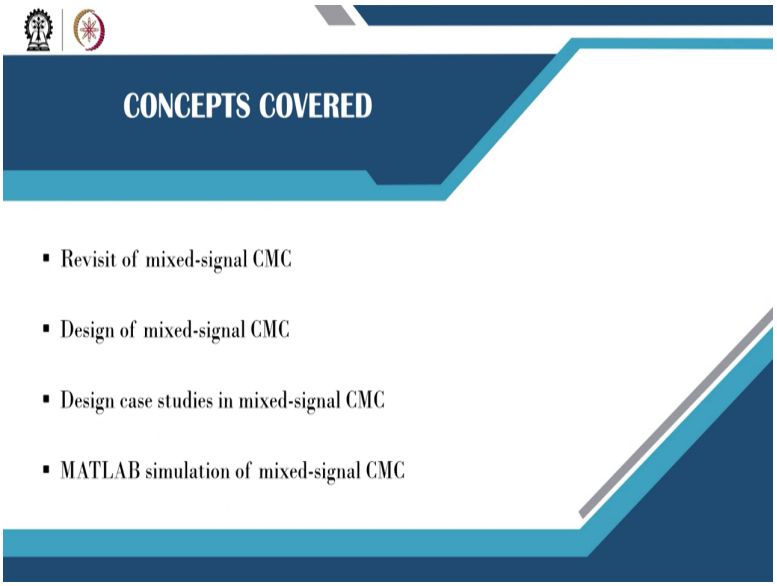

So, here we will first revisit the mixed signal current mode control. We will discuss the design of mixed-signal current mode control we will take some design case studies with our realistic hardware parameter values and will make some MATLAB simulation case studies.

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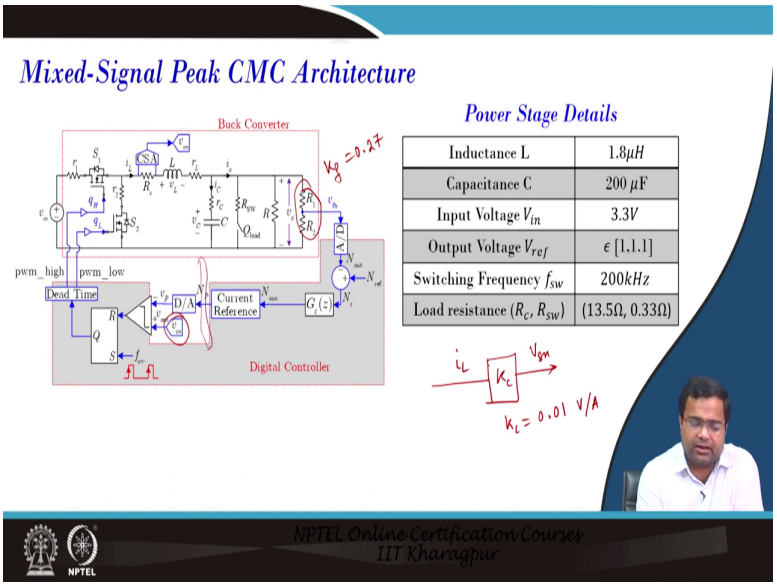

Then if we consider this mixed signal peak current mode control we have discussed multiple times we week 3. As well as we made MATLAB simulation week 3. Here we are talking about inductor-capacitor input voltage output voltage switching frequency. This thing also we have discussed multiple times our hardware prototype and their power stage parameters.

Now, if we go for implementing what we are using in our deck. Here we have a Vsense; that means, our Vsense has that is your iL, we have considered some Kc which will give Vsense, and this Kc we have considered you know 0.01 volt per ampere.

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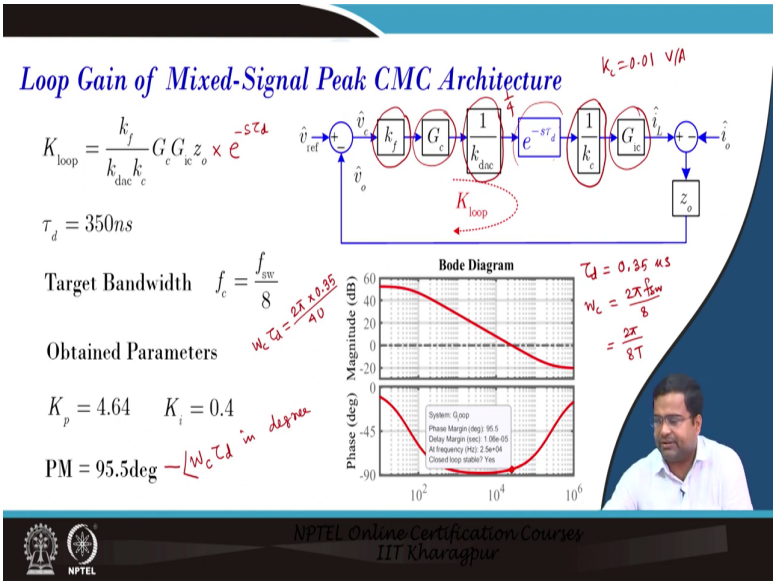

And if we take the loop transfer function here also we have used a feedback gain due to the resistive divider. So, this kf is 0.27 that we found, and yeah and we also got some gain here when there is a binary transformation and I will discuss this deck.

So, I mean if you write the loop transfer function the effective loop transfer function. So, if the feedback gain due to the voltage resistive divider 1 by k DAC is the deck gain and which is 1 by 4 and then we are getting 1 by kc, which is like because kc is how much kc is 0.01 volt per ampere and then this is our traditional current to the control current to inductor current transfer function and Gc is the controller that you are going to use.

So, if you write the loop transfer function here then in this loop transfer function if you want to achieve. We should have an additional e to the power minus s tau d that term will come here in the loop transfer function because it is part of the loop. And then the target bandwidth is fs by 8 then if we draw the bode plot you will get a phase margin slightly less than 95 degrees because here there will be an additional drop due to the cross-over frequency into tau d and that phase will also come in degree.

And since our tau d is we are getting like a 0.35 microsecond and what is our cross-over frequency it is 2 pi fsw by you know what is fsw by 8 and what is fsw 2 pi by T into 8; that means, into 8; that means, 8T. I would say it is 8T, 8 T. So, then what is omega c into tau d? It will be t is a pi microsecond. So, it will be 2 pi divided by 0.35 sorry divided by 8 into 5 40 ok.

So, this term is quite small; that means, we can consider this as very small than omega c into tau d. So, as a result, the phase contribution will be very negligible and insignificant.

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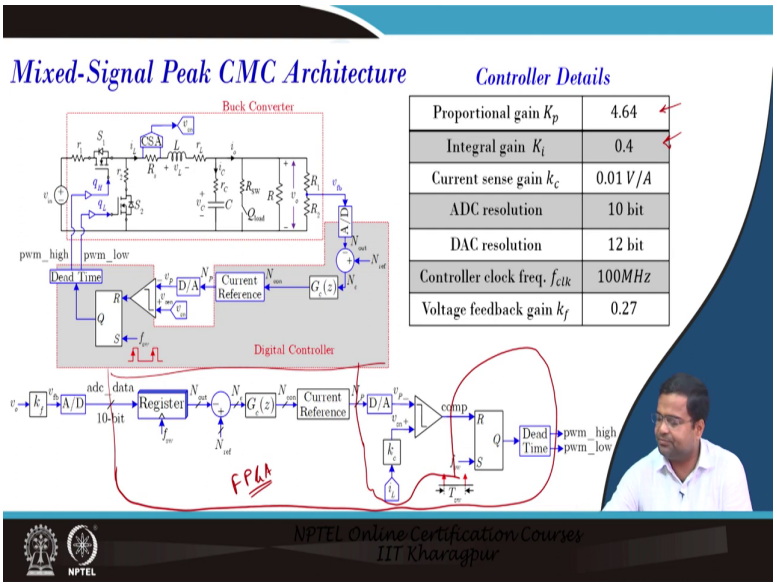

And if we design the peak current mode control for this gain we found that Kp is coming to 4.64 and Ki to be 0.4. This is a discrete-time integral gain to achieve a bandwidth of fs by 8. And this is what we are going to implement first we made a simulation and will also show the hardware experimental results as well for the same configuration. Same proportional gain, same integral gain.

And now and this is what we have made the FPGA we have up to this point we have in FPGA then again this comparator output to this block is the part of this we kept inside the FPGA digital implementation.

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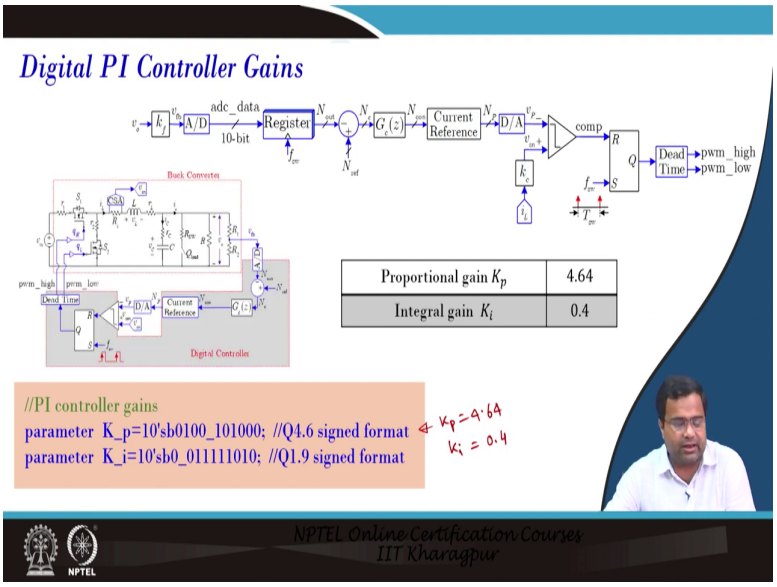

Now, digital pi controller we have used this 0.4 you know what you got 4.7 6 4 and this is Ki equal to 0.4. So, this corresponds to Kp equal to 4.64 and Ki to be 0.4 and this is a gain we are getting.

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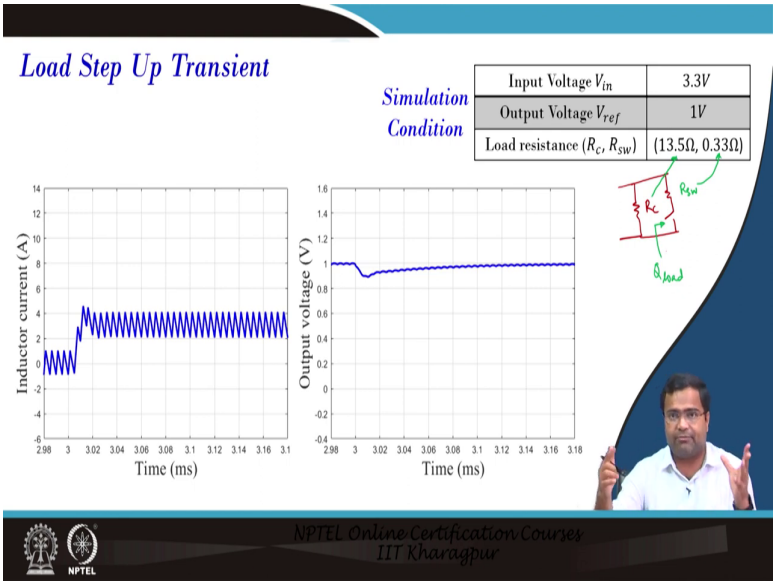

Now, we want to show the load step-up transient. Here input voltage is 3.3, the output is 1 volt and we are making a load transient by changing this resistance we know that there is a continuous resistance which is RC and there is a switch resistance where there is a switch.

And this gate signal we are using is like a gate signal that is our Q load and what is this RSW this is nothing, but this, and RC is nothing, but this.

So, we have to make. So, if you turn on the Q load and make it high it will make a load step of the transient. If you make it 0, it will be a load step-down transient. So, this is the load step-up transient, and we are making it almost like a 3 ampere load step since it is a current mode control and we are making 1-8th of the switching frequency, because if we try to go beyond one-eighth then there will be a model validity issue which we have discussed in our earlier NPTEL course.

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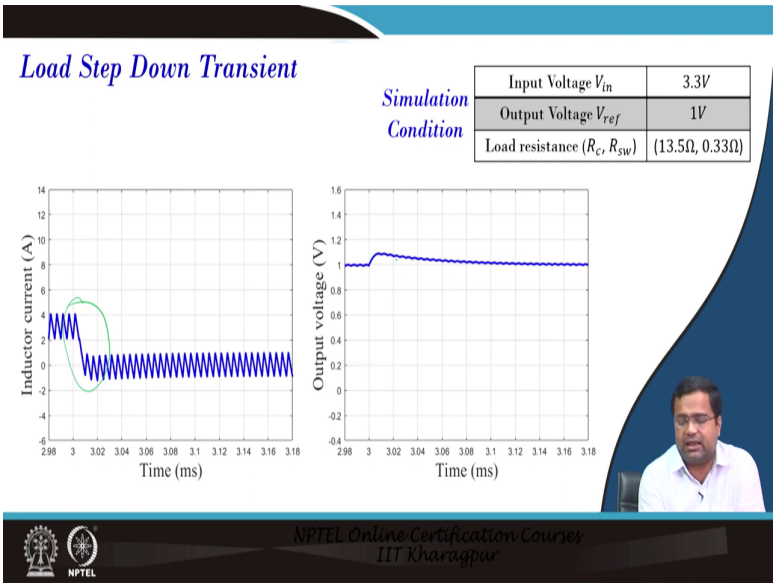

And current mode control is sluggish because it looks almost like a fast order system. As you can see from the response or both step up and step down the response changes very nicely, but after that, it takes a lot of time to come back.

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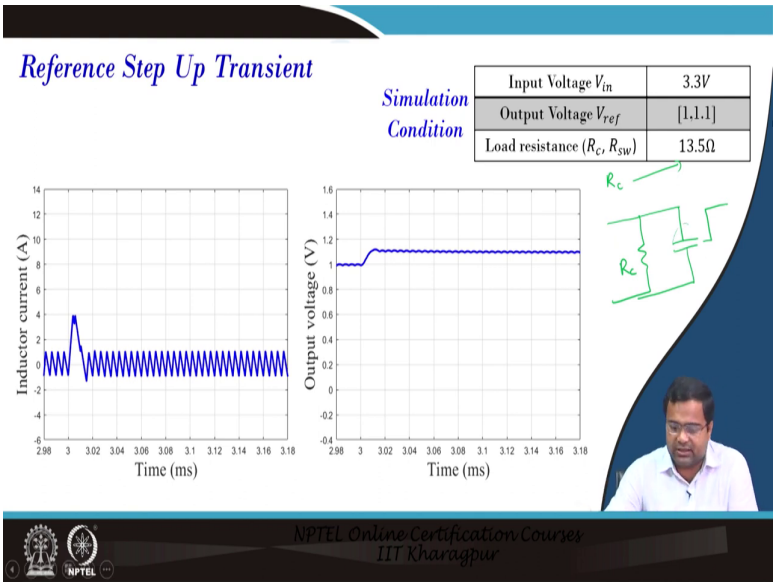

And if you go for reference step transient. It is very fast and the same control again what we are doing? Here we have used only the continuous resistance. That was we are not changing any now; that means, this is the configuration RC and we are making changes to this voltage; that means, we are changing this output voltage by changing the reference command. Only 0.1 volt.

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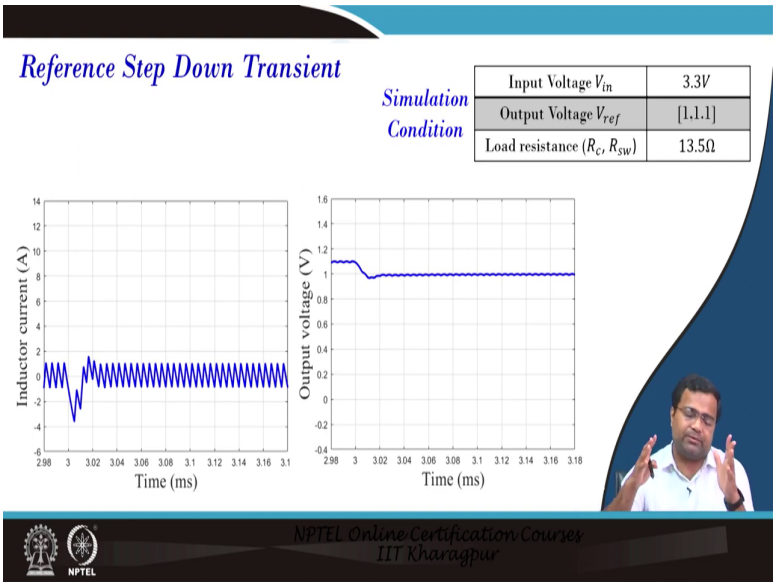

This response is pretty fast and we can see the step-down transient response and this is I would say it a nicely designed because we made it for fsw by 8.

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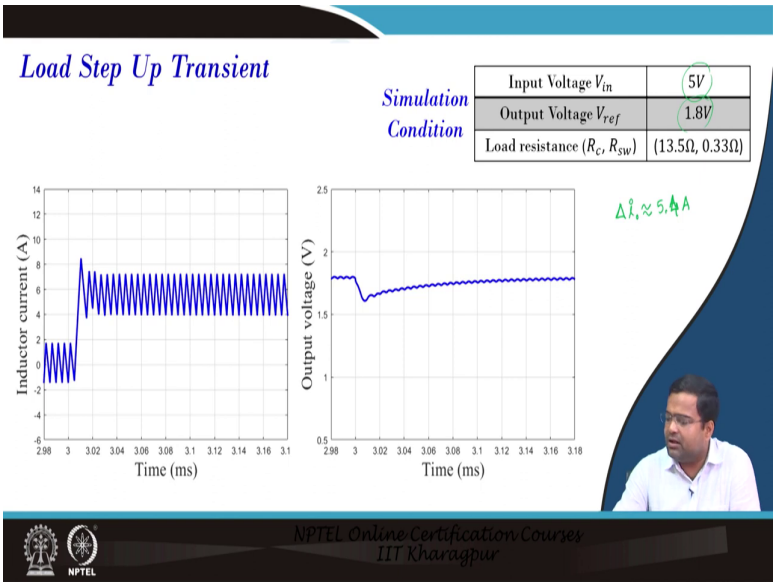

And the load step-up transient if we take with if we take a higher input voltage and higher output voltage then the step size will in this case load step size be almost 5 ampere or here it is like a 5.4-ampere load step size because we have increased the voltage by 0.8 or it is 1 volt this is now 0.8 volt.

So, you can see the response is a bit sluggish, because of the first-order nature of the current mode control the step-down response is also a bit sluggish and if you see the reference transient performance for 13.5 for higher input voltage these are the response this looks fast.

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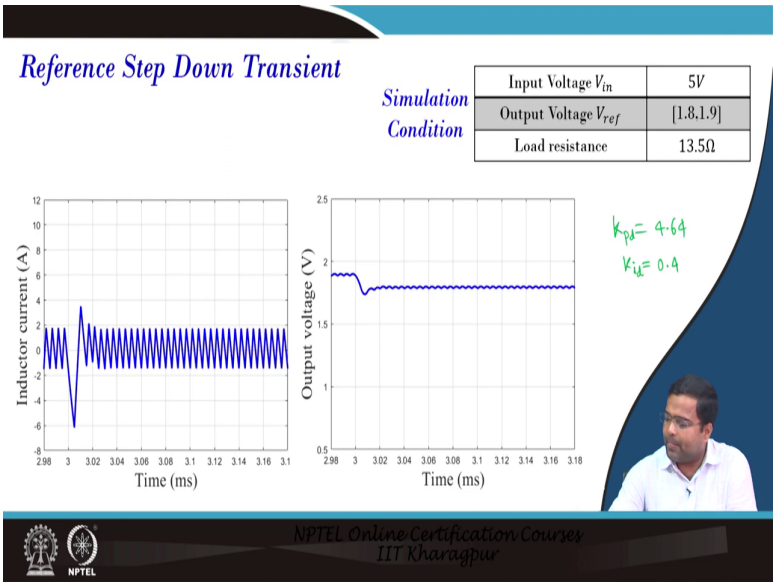

So, we can get a reasonably fast transient response, and in all cases, we are using Kp to be 4.64 and discrete time integral gain that is Kid is 0.4, and for Kpd and Ki Kp continuous time and discrete time are the same.

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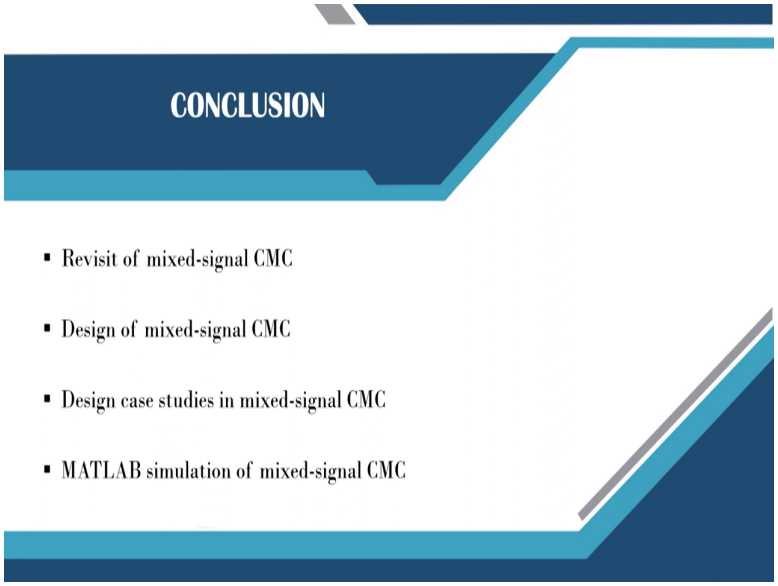

And in the subsequent lecture, we are going to show a hardware case study. So, in summary, we have discussed the mixed signal current mode control design aspect. Then we can we have considered some MATLAB simulation case studies for the design of mixed-signal current mode control. And in the subsequent lecture, we are going to show the hardware experimental result related to a similar you know hardware configuration. That is it for today.

Thank you very much.