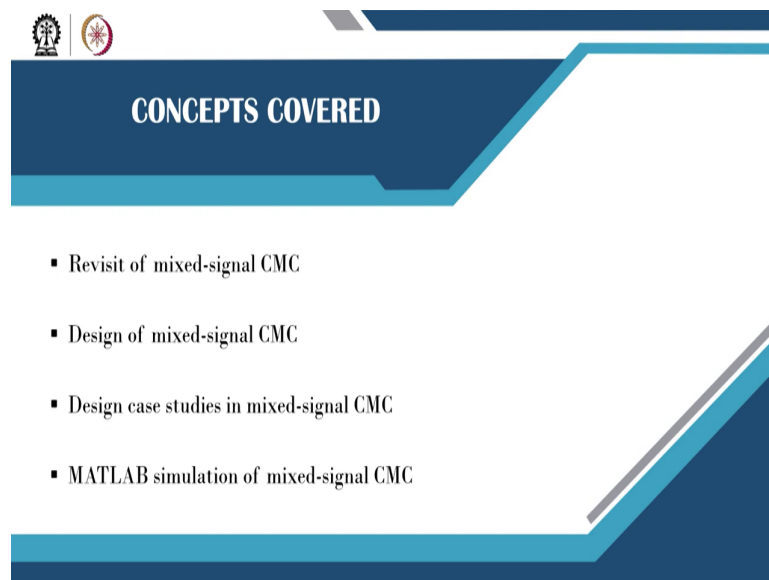


Digital Control in Switched Mode Power Converters and FPGA-based Prototyping
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Module - 11
Design and Validation Case Studies using Digital Voltage and Current Mode Control
Lecture - 106
Design and Simulation Case Studies in a Mixed-Signal CMC Buck Converter

Welcome. In this course, we are going to talk about the design of mixed-signal current mode control in a buck converter with some simulation MATLAB simulation case studies.

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The slide features a dark blue background with a light blue geometric shape on the right side. At the top left, there are two small circular logos. The title 'CONCEPTS COVERED' is centered in white text. Below the title, a bulleted list contains four items.

- Revisit of mixed-signal CMC
- Design of mixed-signal CMC
- Design case studies in mixed-signal CMC
- MATLAB simulation of mixed-signal CMC

So, here we will first revisit the mixed signal current mode control. We will discuss the design of mixed-signal current mode control we will take some design case studies with our realistic hardware parameter values and will make some MATLAB simulation case studies.

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Mixed-Signal Peak CMC Architecture

Inductance L	1.8μH
Capacitance C	200 μF
Input Voltage V_{in}	3.3V
Output Voltage V_{ref}	ε [1.1.1]
Switching Frequency f_{sw}	200kHz
Load resistance (R_c, R_{sw})	(13.5Ω, 0.33Ω)

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Then if we consider this mixed signal peak current mode control we have discussed multiple times we week 3. As well as we made MATLAB simulation week 3. Here we are talking about inductor-capacitor input voltage output voltage switching frequency. This thing also we have discussed multiple times our hardware prototype and their power stage parameters.

Now, if we go for implementing what we are using in our deck. Here we have a Vsense; that means, our Vsense has that is your i_L , we have considered some K_c which will give Vsense, and this K_c we have considered you know 0.01 volt per ampere.

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Loop Gain of Mixed-Signal Peak CMC Architecture

$$K_{loop} = \frac{k_f}{k_c k_{dac}} G_c G_{ic} z_o \times e^{-s\tau_d}$$

$$\tau_d = 350ns$$

Target Bandwidth $f_c = \frac{f_{sw}}{8}$

Obtained Parameters

$$K_p = 4.64 \quad K_i = 0.4$$

$$PM = 95.5deg \quad -|w_c \tau_d| \text{ in degrees}$$

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And if we take the loop transfer function here also we have used a feedback gain due to the resistive divider. So, this k_f is 0.27 that we found, and yeah and we also got some gain here when there is a binary transformation and I will discuss this deck.

So, I mean if you write the loop transfer function the effective loop transfer function. So, if the feedback gain due to the voltage resistive divider $1/k_{DAC}$ is the deck gain and which is $1/4$ and then we are getting $1/k_c$, which is like because k_c is how much k_c is 0.01 volt per ampere and then this is our traditional current to the control current to inductor current transfer function and G_c is the controller that you are going to use.

So, if you write the loop transfer function here then in this loop transfer function if you want to achieve. We should have an additional $e^{-s\tau_d}$ that term will come here in the loop transfer function because it is part of the loop. And then the target bandwidth is $f_s/8$ then if we draw the bode plot you will get a phase margin slightly less than 95 degrees because here there will be an additional drop due to the cross-over frequency into τ_d and that phase will also come in degree.

And since our τ_d is we are getting like a 0.35 microsecond and what is our cross-over frequency it is $2\pi f_{sw}/8$ by you know what is $f_{sw}/8$ and what is $f_{sw} 2\pi/T$ into 8; that means, into 8; that means, $8T$. I would say it is $8T$, $8T$. So, then what is $\omega_c \tau_d$? It will be t is a π microsecond. So, it will be 2π divided by 0.35 sorry divided by 8 into 540 ok.

So, this term is quite small; that means, we can consider this as very small than $\omega_c \tau_d$. So, as a result, the phase contribution will be very negligible and insignificant.

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Mixed-Signal Peak CMC Architecture

The diagram illustrates the architecture of a Mixed-Signal Peak Current Mode Control (CMC) system. It is divided into three main sections:

- Buck Converter:** A power electronic circuit with an input voltage v_a , a switching network (MOSFETs S_1, S_2 and diodes D_1, D_2), an inductor L , and an output capacitor C . It produces an output voltage v_o and current i_o .
- Digital Controller:** A block that receives a reference current N_i and a feedback signal N_o . It contains a digital filter $G(z)$, a DAC, and a current reference generator. It outputs a PWM signal N_{ref} to the converter.
- FPGA Implementation:** Shows the digital controller's internal structure, including an ADC (10-bit), a register, a DAC (12-bit), a comparator, and a dead-time block. The output is a PWM signal N_{ref} that drives the buck converter.

Controller Details

Proportional gain K_p	4.64
Integral gain K_i	0.4
Current sense gain k_c	0.01 V/A
ADC resolution	10 bit
DAC resolution	12 bit
Controller clock freq. f_{clk}	100MHz
Voltage feedback gain k_f	0.27

And if we design the peak current mode control for this gain we found that K_p is coming to 4.64 and K_i to be 0.4. This is a discrete-time integral gain to achieve a bandwidth of f_s by 8. And this is what we are going to implement first we made a simulation and will also show the hardware experimental results as well for the same configuration. Same proportional gain, same integral gain.

And now and this is what we have made the FPGA we have up to this point we have in FPGA then again this comparator output to this block is the part of this we kept inside the FPGA digital implementation.

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Digital PI Controller Gains

Proportional gain K_p	4.64
Integral gain K_i	0.4

```
//PI controller gains
parameter K_p=10'sb0100_101000; //Q4.6 signed format
parameter K_i=10'sb0_011111010; //Q1.9 signed format
```

Handwritten notes: $K_p = 4.64$, $K_i = 0.4$

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Now, digital pi controller we have used this 0.4 you know what you got 4.7 6 4 and this is Ki equal to 0.4. So, this corresponds to K_p equal to 4.64 and K_i to be 0.4 and this is a gain we are getting.

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Load Step Up Transient

Simulation Condition

Input Voltage V_{in}	3.3V
Output Voltage V_{ref}	1V
Load resistance (R_c, R_{sw})	(13.5Ω, 0.33Ω)

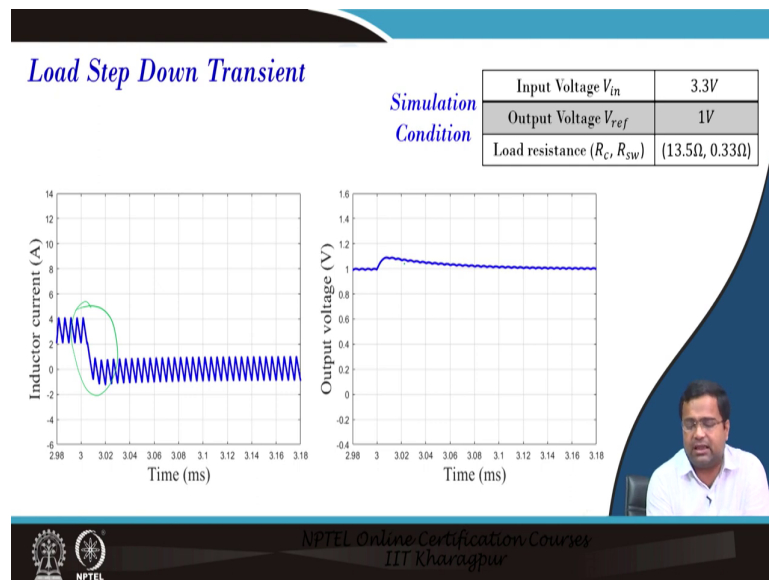
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Now, we want to show the load step-up transient. Here input voltage is 3.3, the output is 1 volt and we are making a load transient by changing this resistance we know that there is a continuous resistance which is RC and there is a switch resistance where there is a switch.

And this gate signal we are using is like a gate signal that is our Q load and what is this RSW this is nothing, but this, and RC is nothing, but this.

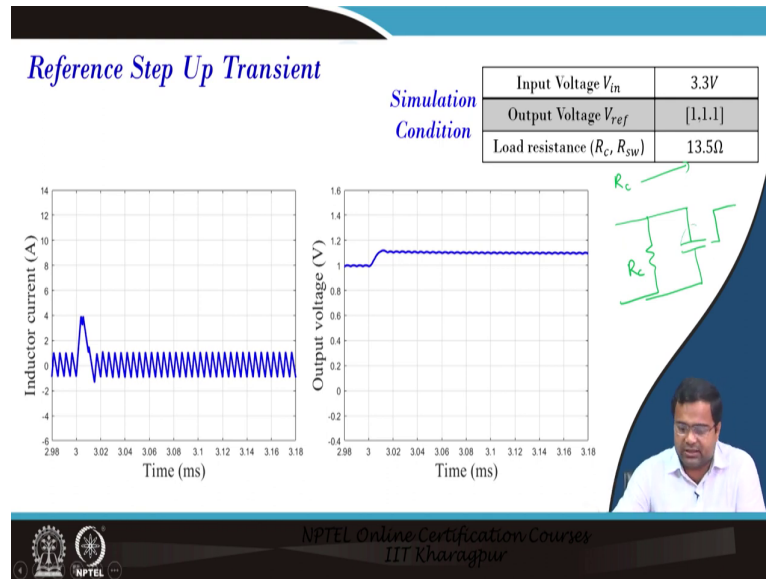
So, we have to make. So, if you turn on the Q load and make it high it will make a load step of the transient. If you make it 0, it will be a load step-down transient. So, this is the load step-up transient, and we are making it almost like a 3 ampere load step since it is a current mode control and we are making 1-8th of the switching frequency, because if we try to go beyond one-eighth then there will be a model validity issue which we have discussed in our earlier NPTEL course.

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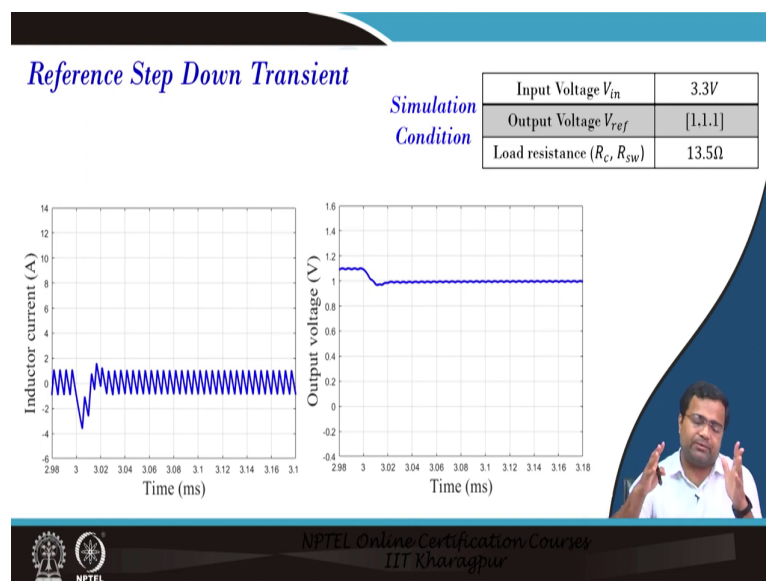
And current mode control is sluggish because it looks almost like a fast order system. As you can see from the response or both step up and step down the response changes very nicely, but after that, it takes a lot of time to come back.

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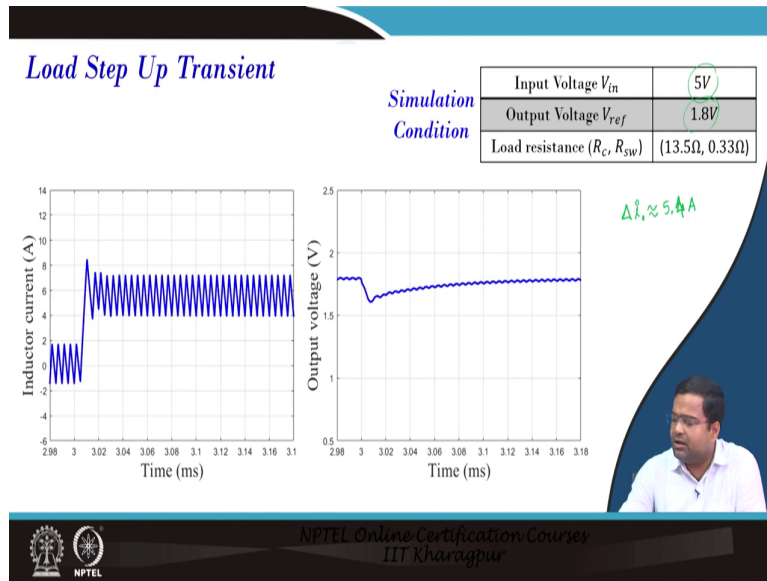
And if you go for reference step transient. It is very fast and the same control again what we are doing? Here we have used only the continuous resistance. That was we are not changing any now; that means, this is the configuration RC and we are making changes to this voltage; that means, we are changing this output voltage by changing the reference command. Only 0.1 volt.

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This response is pretty fast and we can see the step-down transient response and this is I would say it a nicely designed because we made it for fsw by 8.

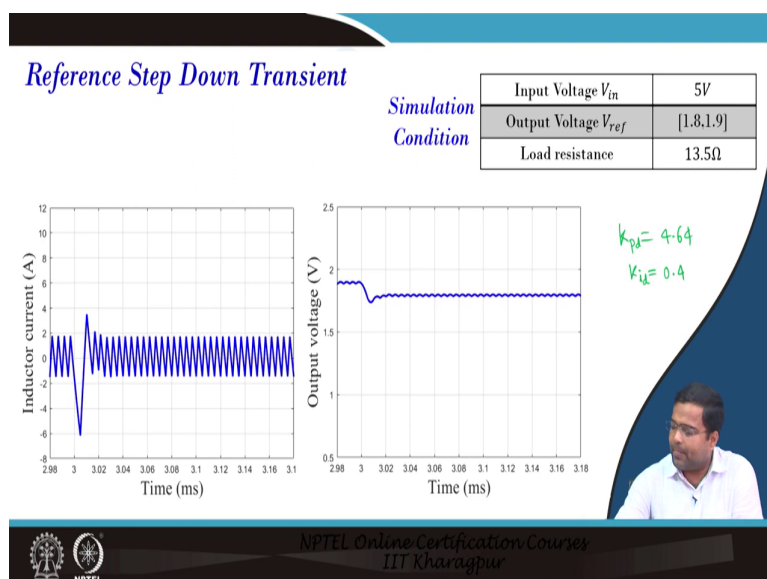
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And the load step-up transient if we take with if we take a higher input voltage and higher output voltage then the step size will in this case load step size be almost 5 ampere or here it is like a 5.4-ampere load step size because we have increased the voltage by 0.8 or it is 1 volt this is now 0.8 volt.

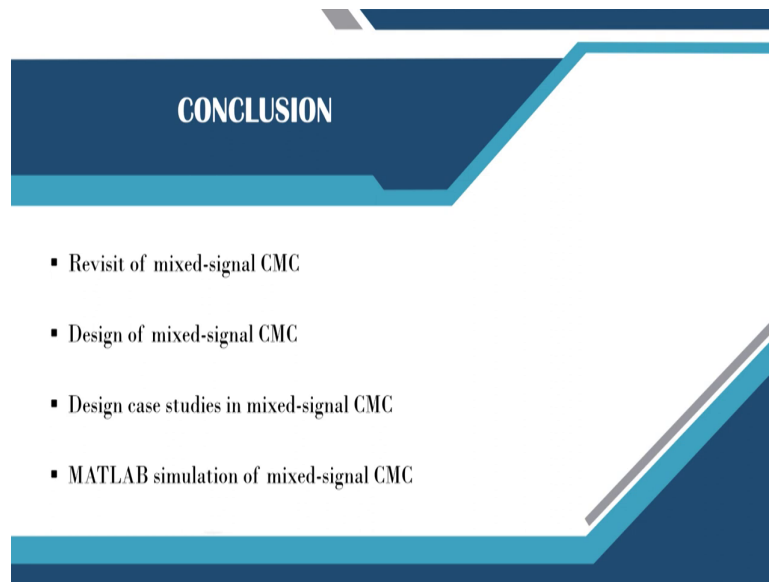
So, you can see the response is a bit sluggish, because of the first-order nature of the current mode control the step-down response is also a bit sluggish and if you see the reference transient performance for 13.5 for higher input voltage these are the response this looks fast.

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So, we can get a reasonably fast transient response, and in all cases, we are using K_p to be 4.64 and discrete time integral gain that is K_{id} is 0.4, and for K_{pd} and K_i K_p continuous time and discrete time are the same.

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CONCLUSION

- Revisit of mixed-signal CMC
- Design of mixed-signal CMC
- Design case studies in mixed-signal CMC
- MATLAB simulation of mixed-signal CMC

And in the subsequent lecture, we are going to show a hardware case study. So, in summary, we have discussed the mixed signal current mode control design aspect. Then we can we have considered some MATLAB simulation case studies for the design of mixed-signal current mode control. And in the subsequent lecture, we are going to show the hardware experimental result related to a similar you know hardware configuration. That is it for today.

Thank you very much.