Digital Control in Switched Mode Power Converters and FPGA-based Prototyping
Dr. Santanu Kapat
Department of Electrical Engineering
Indian Institute of Technology, Kharagpur

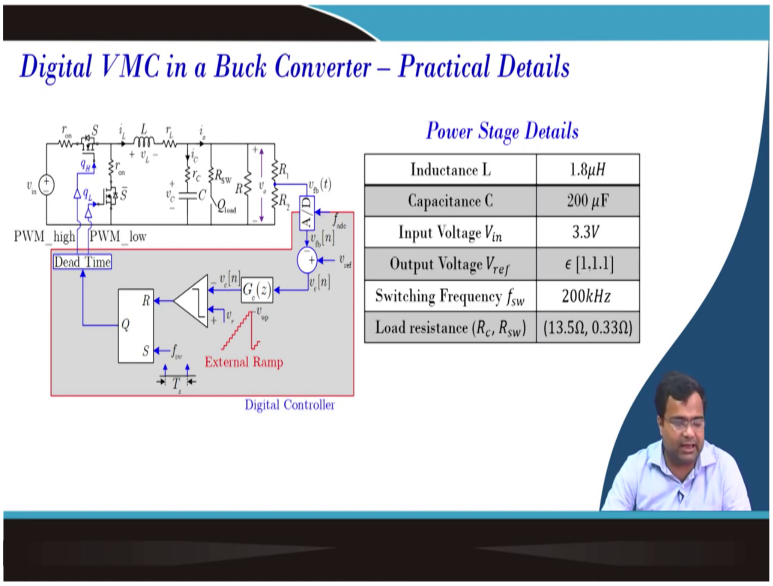
Module - 11
Design and Validation Case Studies using Digital Voltage and Current Mode Control
Lecture - 105
Hardware Case Studies and Transient Performance in Digital VMC Buck Converter

Welcome, in this lecture we are going to talk about Hardware Case Studies and Transient Performance in Digital Voltage Mode Control Buck Converters.

(Refer Slide Time: 00:32)

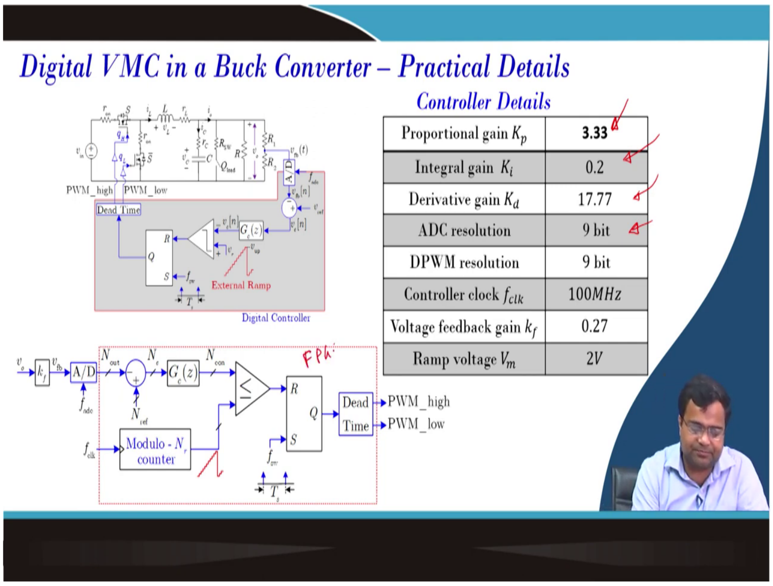
So, we are first going to consider the design case study of the digital voltage mode control, experimental load transient performance with case studies, and experimental reference transient performance.

(Refer Slide Time: 00:43)



So, in the digital voltage mode control buck converter, we have discussed in detail. These are the power stage detail that we have discussed multiple times.

(Refer Slide Time: 00:53)

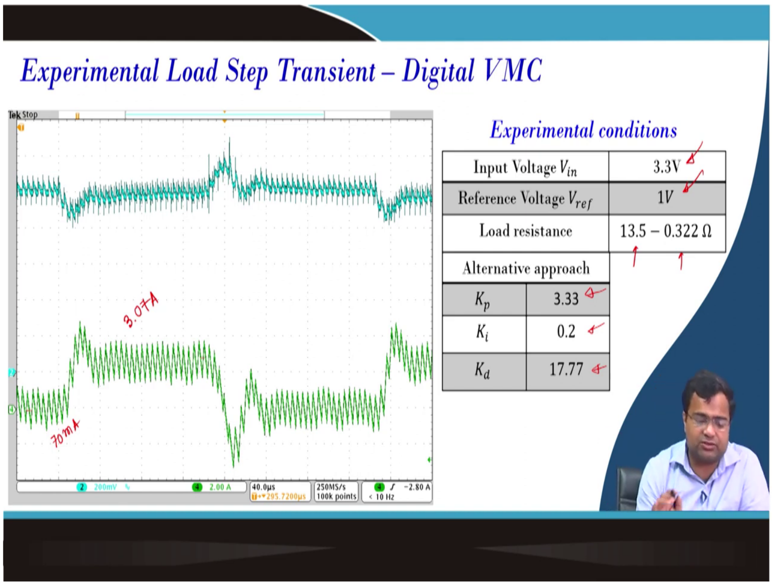


And initially, we are considering you know the 3.3 volt input and this is the design parameter for 3.3 volt input which we have discussed in the previous lecture which was considered the simulation case study derivative gain. Only we have reduced the integral gain because you know otherwise in hardware there are some other un-modeled dynamics and delays.

So, we have reduced the integral gain to avoid you know under like an otherwise it will lead to a lot of damping issues it will become more under damp. So, we have reduced the integral gain we have kept the same proportional derivative gain ADC resolution. Effectively we have taken 9 bit though it is an 8 bit, 10 bit ADC.

And then controller frequency 100 megahertz that we have discussed ramp 2 volt, voltage feedback gain 0.27. We have discussed multiple times the digital voltage mode control of this architecture which will be inside an FPGA.

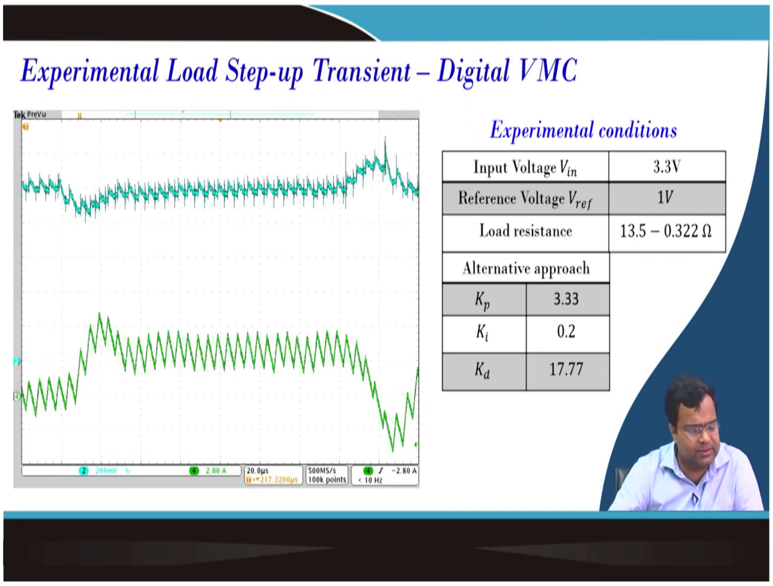
(Refer Slide Time: 01:53)



Now, we are first considering a first case study of load step transient where 3.3 volt input and 1 volt output and the load resistance is changing from 13.5 to 0.322 ohm and back because this is step up and step down. And we are designing using an alternative approach K p and K d are coming from the design which we made in the previous lecture only you have reduced K i and limited it to 0.2.

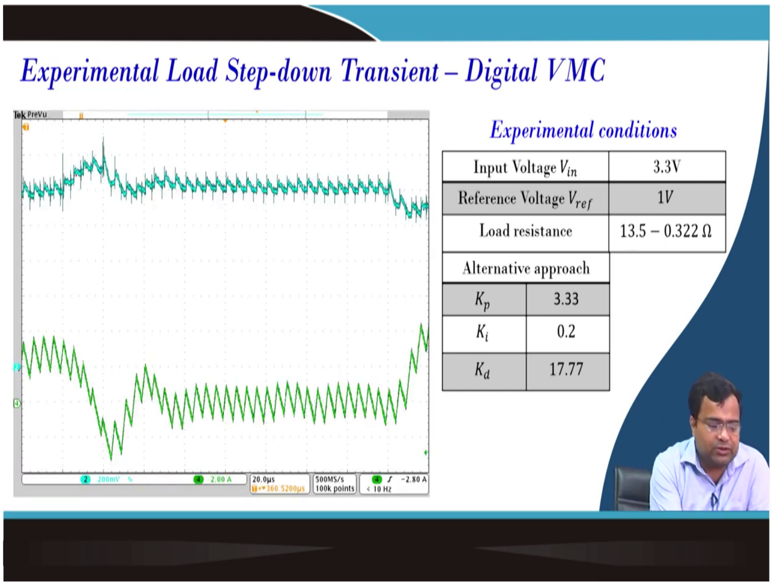
And this is the load transient performance and you can see that it is a nicely damp system for the load which was like it is changing from roughly 70 milli ampere to 3.07 ampere and where the load step size is roughly around 3 ampere. So, the undershoot and overshoots are much within the limit and it is a more or less well-damped response.

(Refer Slide Time: 02:45)



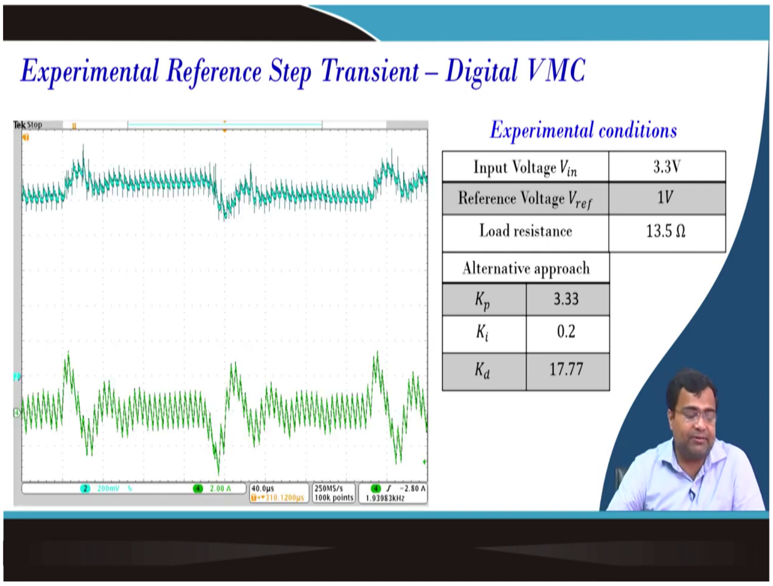
This is a zoom version of this and you can see that undershoot is if we consider this average it is roughly 100 milli volt and the settling time is coming to be around 25 microseconds which are reasonably fast like a 5 cycle or so ok.

(Refer Slide Time: 03:05)

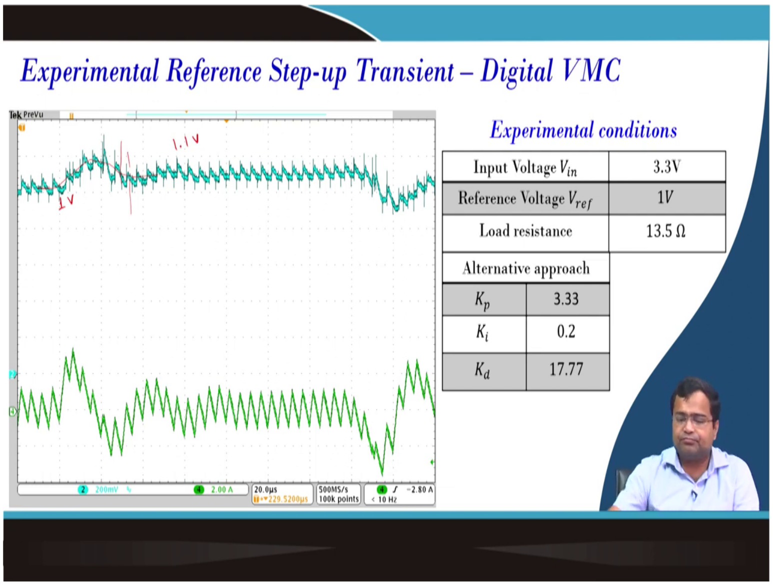


And if we take the step down the overshoot is also going around I think if you take the average value. Because of the measuring point if we measure right across the capacitor then you will see this spike will get reduced and you will get more or less the average value. So, this average value if you see this overshoot will be around you know 130 milli volt or so and it is the response time is coming within like you know half of this. So, it is like 30 microsecond which is 6 cycles.

(Refer Slide Time: 03:38)

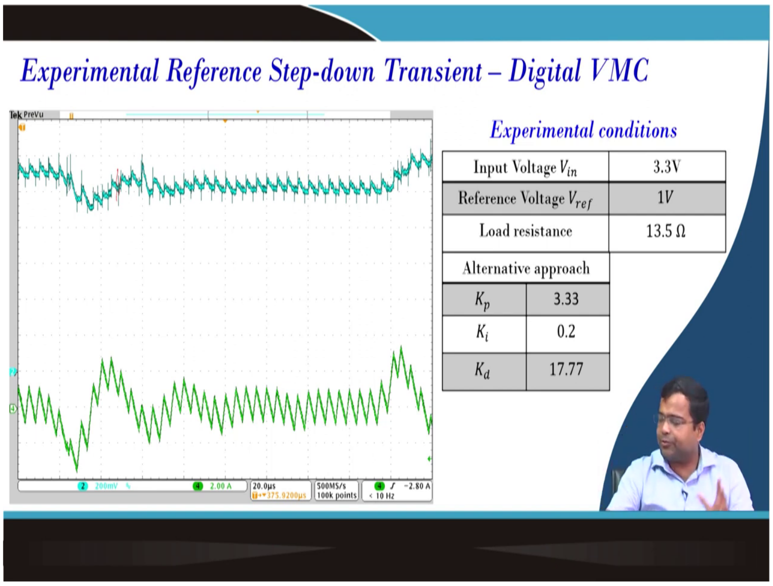


(Refer Slide Time: 03:43)



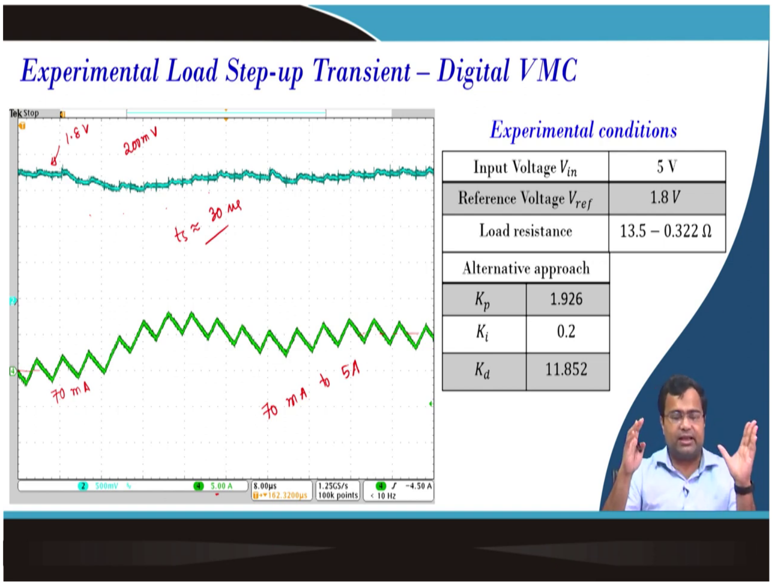
Now, we are talking about reference step up transient the reference step up transient if we take the zoomed version of this. So, this is the reference step-up transient in the average sense. So, there is an additional overshoot of around 50 milli volt and it is changing from 1 volt to 1.1 volt and this is happening as you know like an around 25, 30 microsecond.

(Refer Slide Time: 04:05)



And the step down it is like coming in within this time period. So, which is around 30 microsecond with an additional undershoot of roughly around 100 milli volt ok. So; that means, we have designed this both step up and step down we have designed the voltage mode controller using our alternative approach.

(Refer Slide Time: 04:25)



Now, here we are considering 5 volt and 1.8 volt where the load step again load resistance remains the same. But now there is a step up transient from 70 milli ampere because it is a 5 ampere scale and it is going to around 5. So; that means, it is changing from 70 milli amp to roughly 5 ampere, but you see the undundershootis is you know if you consider 5 volt.

So, this voltage is 1.8 volt, and each division if it is 0.100 milli volt. So, it is going around 20 milli volt. That means, additional like it is coming up to you know where it is 5. So, 1, 2, 3 around 200 milli volt drop and it is reaching within 1, 2, 3, 4; 4 cycle; that means, roughly around settling time is around 30 microseconds or 6 cycles. So, it is a well-damped response even for a large load step transient. So, we can achieve a very nice transient performance with this alternative approach.

(Refer Slide Time: 05:40)

So, in summary, we have discussed a design case study of digital voltage mode control. We have shown experimental load transient performance as well as experimental reference transient performance with case studies that are it for today.

Thank you very much.