Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 11
Design and Validation Case Studies using Digital Voltage and Current Mode Control
Lecture - 104
Digital VMC Design for Shaping Output Impedance in a Buck Converter

Welcome to this lecture we are going to talk about Digital Voltage Mode Control Design for Shaping Output Impedance in a Buck Converter.

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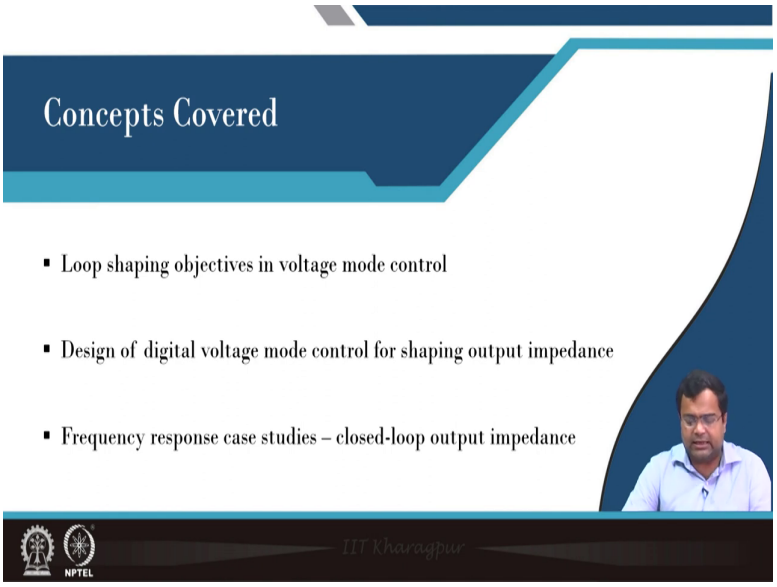

So, in this lecture, we are going to talk about loop-shaping objectives in digital voltage mode controlling these things we have already discussed. We want to show the design of the digital voltage mode control used for shaping the output impedance and the frequency response case study for closed-loop output impedance.

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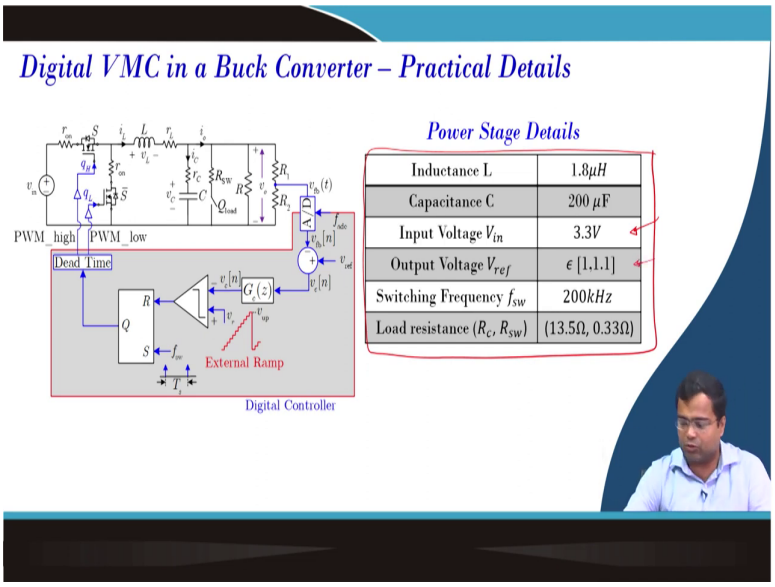

So, here the digital voltage mode control we are taking the same practical case study power stage which will be used for the experimental case study ok. And here we will take both 3.3 volt input as well as 5 volt input and 1 volt output as well as 1.8 volt output.

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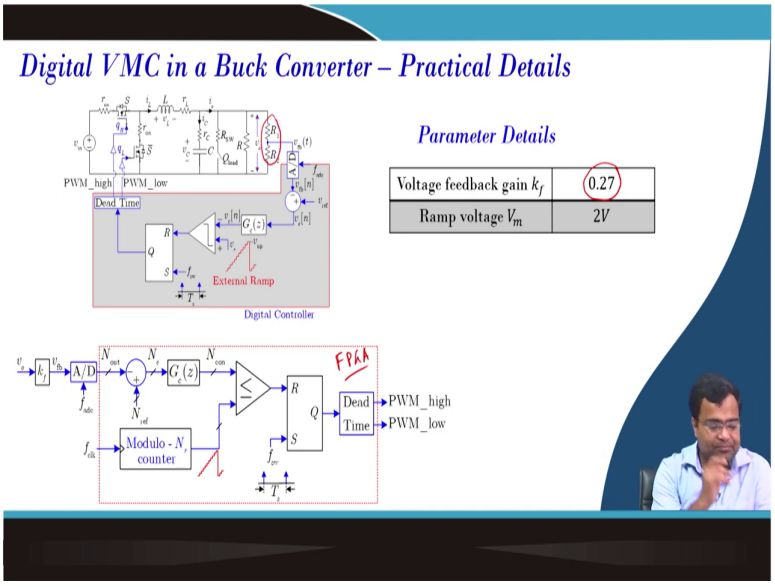

As we have discussed in our earlier that we have to implement using FPGA when you go for digital control in voltage mode control implementation this thing also we have discussed. And there is also a feedback gain in a practical converter and which is because of this resistive divider and this is also here what we have discussed.

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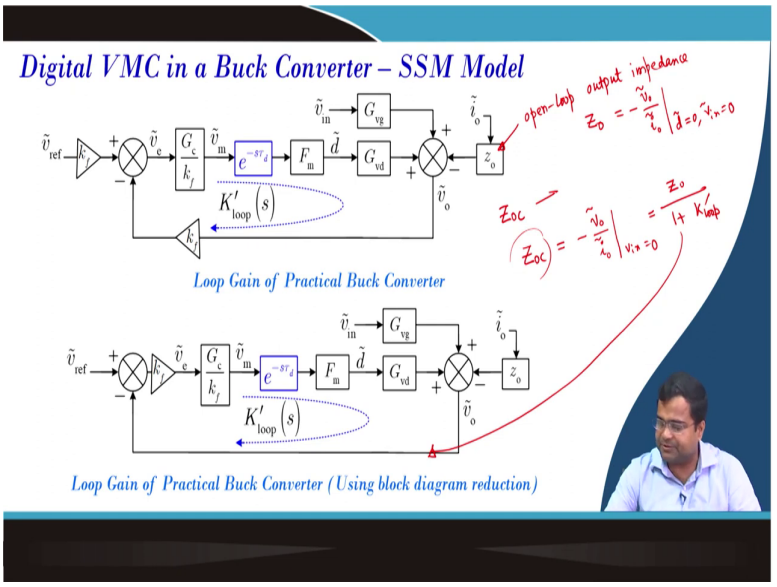

Now, we have also discussed in the previous lecture the design aspects. So, we are not going to repeat the design aspect. But here what we are going to do this is our open-loop output impedance, this is our open loop output impedance which we call Z 0 and we want to get closed-loop output impedance. That means, and what is this for open loop output impedance it is minus V 0 tilde by the external load tilde when we are considering the duty ratio to be 0, and input voltage perturbation to be 0.

But when you are talking about a closed loop then the loop is closed. So, it will be again minus V 0 to i 0, but in this case, we are only talking about input voltage 0 and it can be shown that this is 0 output divided by 1 plus loop transfer function that is this k dash loop. So, this is the loop transformation here ok. So, how can we get the closed loop output impendence which is the critical part for getting the load transient performance?

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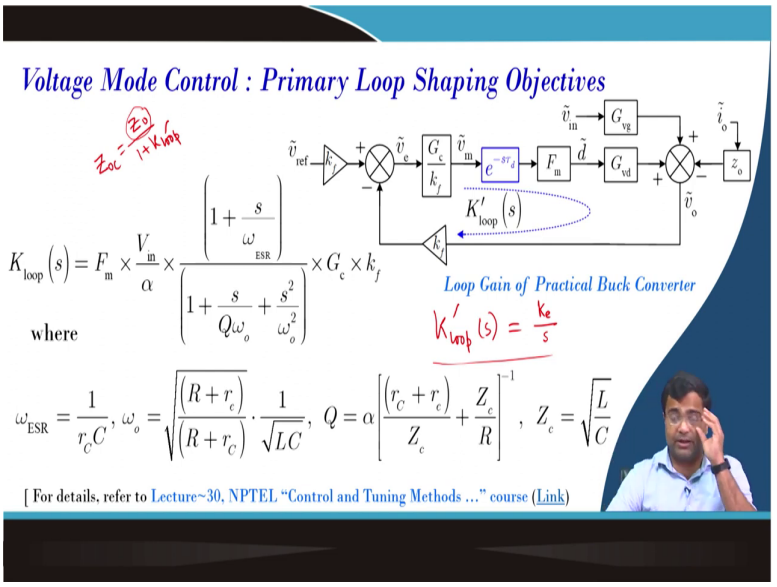

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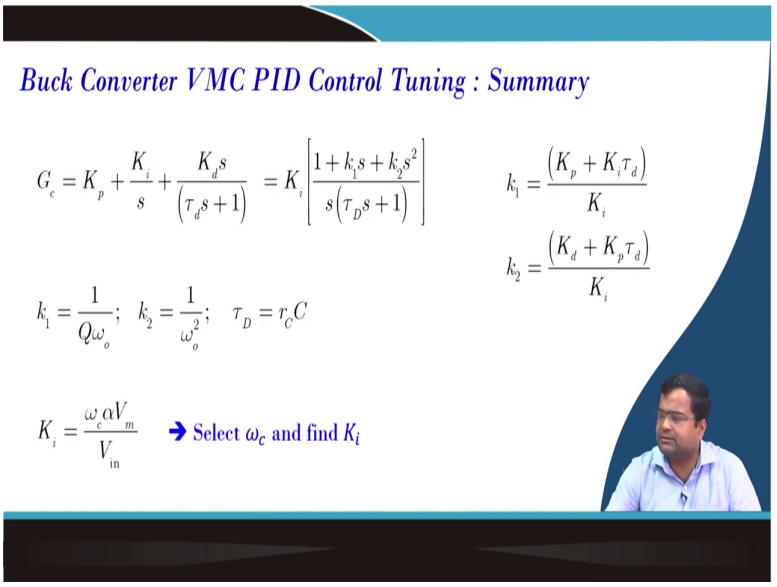

So, now we have discussed in lecture number 30 in our earlier NPTEL course that exact pole 0 stable pole 0 cancellation is very sensitive to system parameters. But when you talk about the closed-loop output impedance; that means, here we are shaping the loop transfer function to get what was our objective to get you to know our objective was we wanted to get this thing to be some gain maybe some effective gain divided by S.

That means we want to get a fast order loop transfer function, but that is we are shaping the loop. But when we talk about the closed-loop output impedance then we still have this open

loop plus 1 plus this loop dash which is here. So; that means, even though you shape the out loop transfer function you may not have direct control over the open loop output impedance.

As a result, you know there is we saw there is a difficulty in shaping output impedance closed-loop output impedance purely based so; that means, design based on pure loop shaping is not effective for shaping the output impedance.

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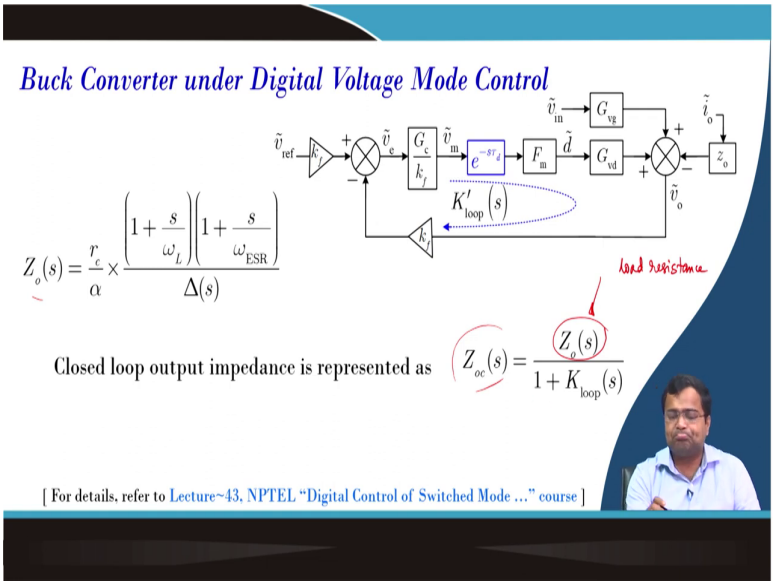

And again we are considering the loop shaping approach and we are getting the PID controller design which we have discussed in lecture number 43. So, this is open loop output impedance or closed loop. So, the pure loop shaping objective is not perfect for closed-loop output impedance shaping. Because we have no control over open loop output impedance and which is highly sensitive to load resistance because when the load resistance varies. So, it is highly sensitive.

But suppose the converter is purely driven by the output current load there is no resistive load. Then the output impedance will be purely the parasitic of the inductor and capacitor in that case it will be more or less known. But still, the output impedance by pure loop shaping objective is not the right approach.

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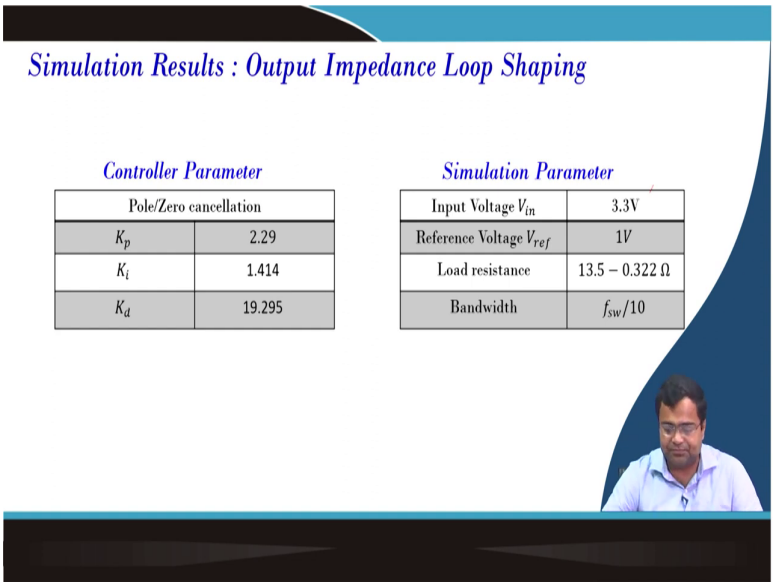

Then what to do? So, we are showing a case study if we go for pole-zero cancellation and the simulation parameter we are talking about 3.3 volt input and 1 volt output and our desired bandwidth is fsw by 10.

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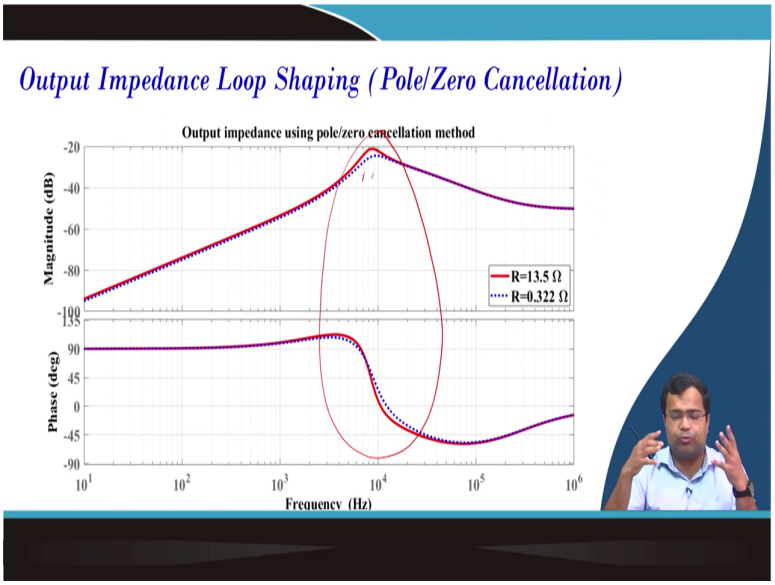

Then this is the pole-zero cancellation. So, you can see there is sort of this particular part that is sensitive to load transient overshoot undershoot ok. And if you vary the load resistance there will be kind of variation slight variation because it depends on the input voltage and

another factor. So, this is the output impedance by taking one-tenth of the switching frequency by stable pole-zero cancellation.

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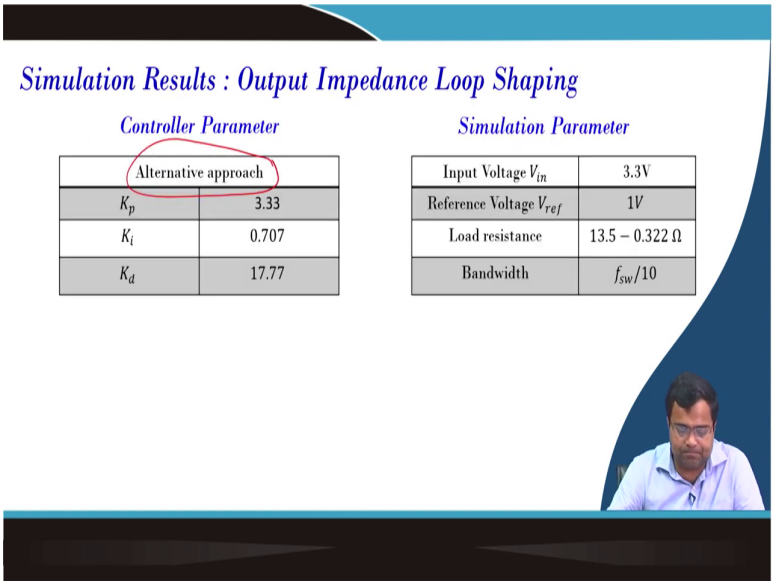

But if you go by this is the case where we are talking about the alternative approach. So, this is the alternative approach we are talking about where we are not canceling the stable pole-zero case.

So; that means, this is a more robust approach and we want to show that output impedance is sort of well damp not only that because if you go back to this slide. So, this particular thing that there is a phase roll off from 90 degree to almost close to less than minus 40 degree, 45 degree.

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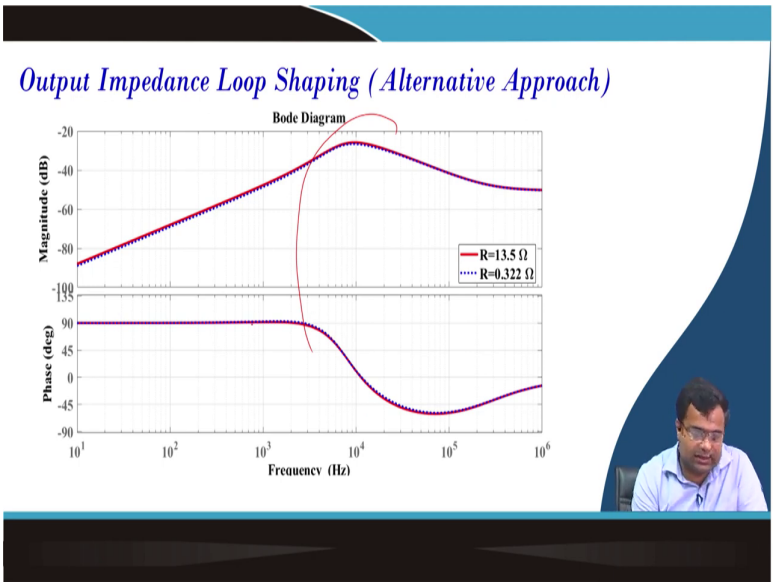

But here if you take the roll-off is not so sharp and secondly, the output impedance now become insensitive to load resistance. That means you can design this method for various load resistance, but the output impedance will be more or less the same. So, that will also that can achieve very nice load transient performance using this alternative approach.

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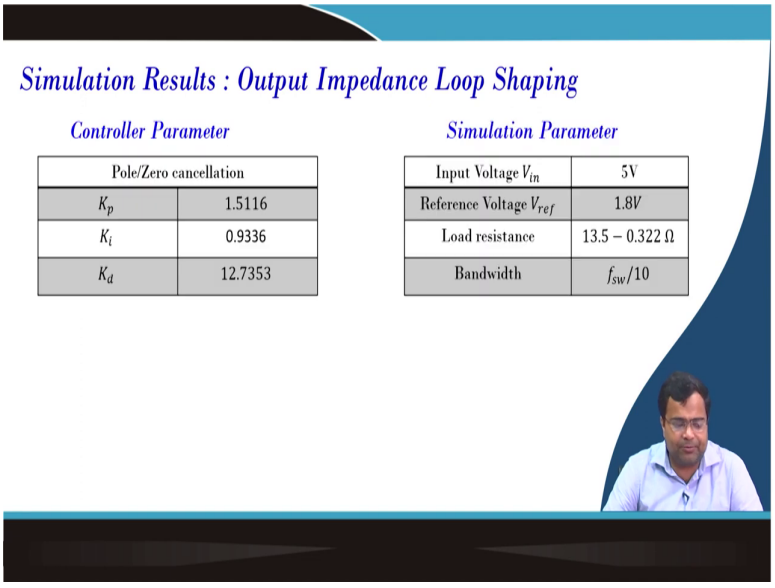

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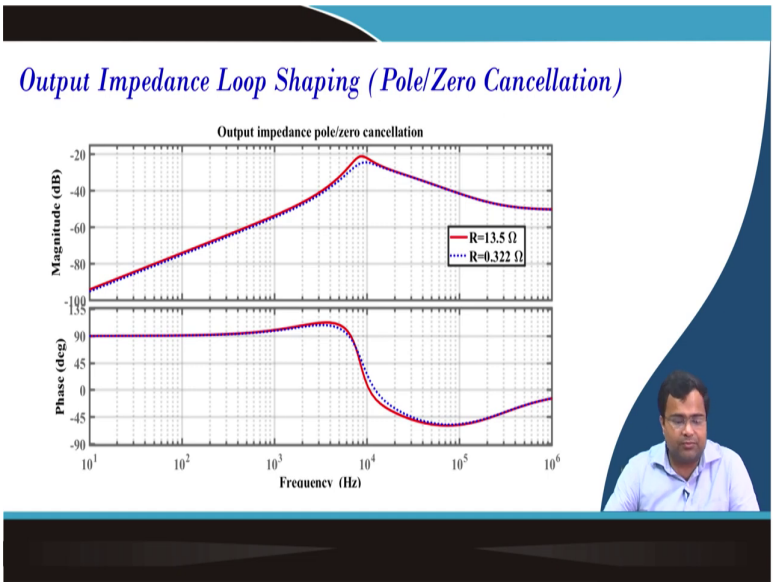

So, if we consider this pole-zero cancellation that output impedance shaping. Now for 5 volt input and 1.8 volt output, we are making a load transient. That means, we want to see the output impedance for both 13.5 and 0.32. So, you can see that there is you know this particular output impedance particular this region if you consider it.

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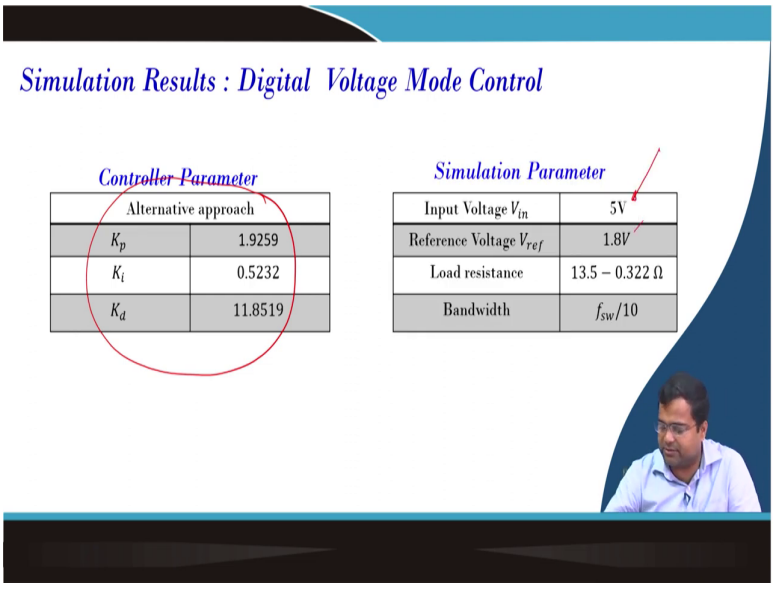

And if you go back to our alternative approach design which results in this K p, K I, K d. If you go by the method that you have discussed and these are the particular case studies 5 volt input, 1.8 volt output.

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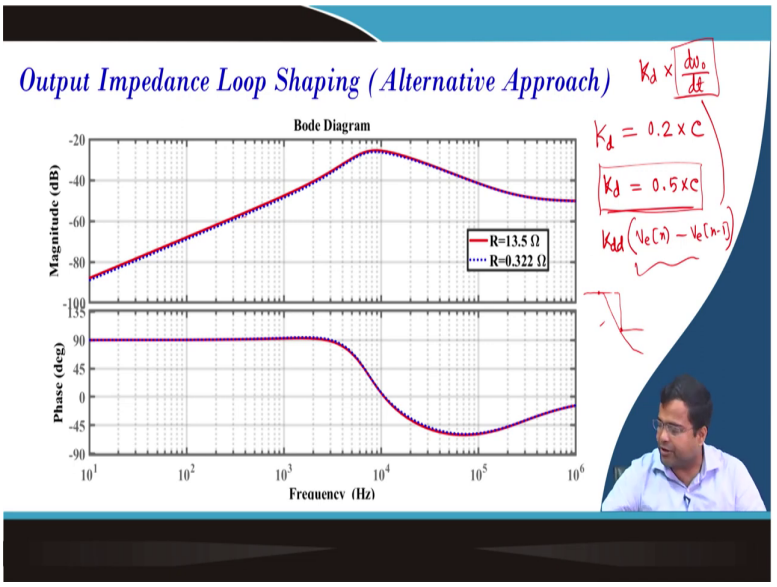

Then you see again the load resistance for two different resistance the output impedance closed-loop output impedance is more or less identical. So, it means this alternative approach can well damp the output impedance. We can further play with the shaping output impedance by suitably considering the derivative gain which is nothing, but a fraction here we took K d in continuous time to be a fraction of 2 C.

We can increase we can take K d to be maybe 0.5 point C we can play with this you can get better you know output impedance. But the only issue is if you increase too much in practical hardware it may also try to inject the noise and when you go to digital where there is no pure derivative it is a discrete function.

Because if you go to K dd actual K d into sort of d v 0 d t although there is a band-limited derivative. But in discrete time it will be V error n minus V error n minus 1. So, since there is one cycle the voltage will be constant. So, this will not be exactly this unless this sampling frequency is very high that is why we may not offer a very large value of capacitor which may create some kind of delayed effect.

Because because if the actual voltage is out deviating if you take the derivative. But if you take the sample here and here you will not get the actual derivative action ok because we are losing the information in between. So, we are keeping a conservative choice of 0.2.

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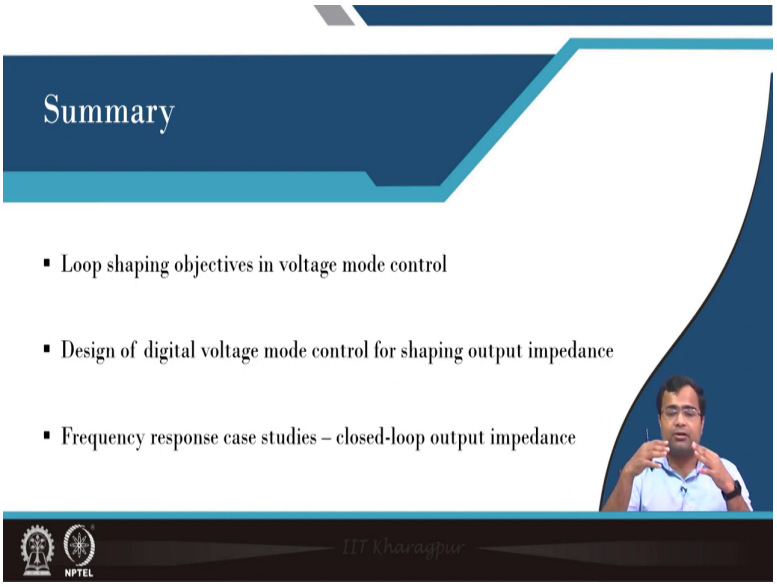

So, in summary, we have discussed loop-shaping objectives in voltage mode control. We have considered the design of digital voltage mode control for output impedance shaping and we have considered a few frequency response case studies for closed-loop output impedance.

In a subsequent lecture the next lecture we are going to show the hardware experimental result for loop shaping; which means, the output impedance shaping result. What does it look like? The load transient performance that, we are going to consider in the next lecture is for today.

Thank you very much.