Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

Dr. Santanu Kapat
Department of Electrical Engineering
Indian Institute of Technology, Kharagpur

Module - 11
Design and Validation Case Studies using Digital Voltage and Current Mode Control
Lecture - 103
Loop Shaping and Design of Digital Voltage Model Control in a Buck Converter

Welcome to this lecture we are going to talk about Loop Shaping and Design Aspect of Digital Voltage Mode Control in a Buck Converter.

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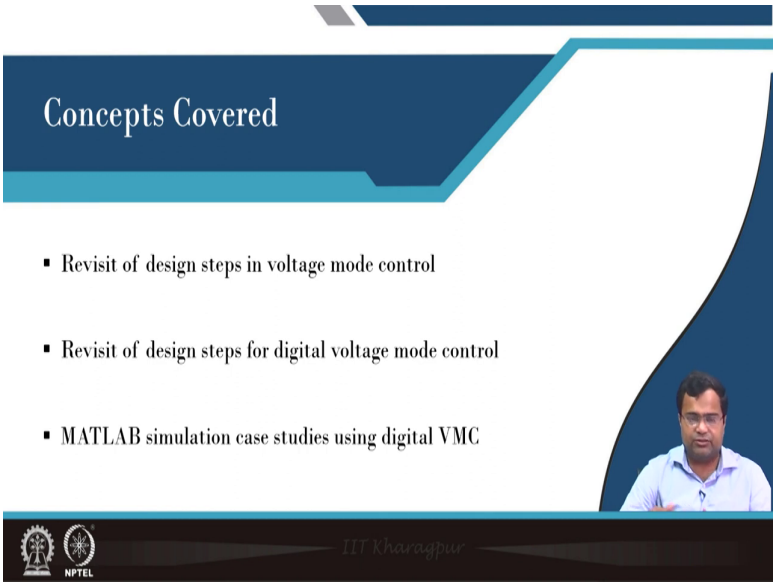

So, here we are going to talk about we want to revisit the design step of voltage mode control which we have already discussed. We want to revisit the design step for digital voltage mode control and finally, we are going to show some MATLAB case study under using digital voltage mode control.

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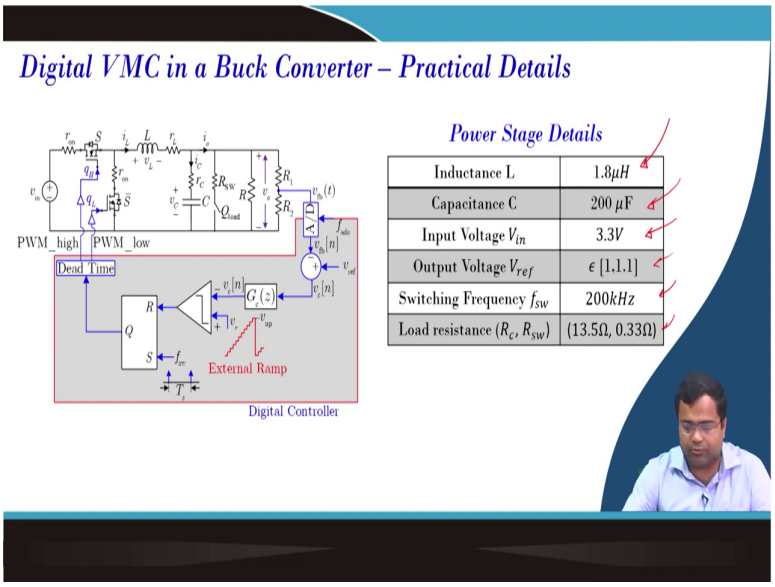

So, if we recollect our digital voltage mode control with power stage because here all the stimulation case studies will be considered consistent with the experimental case study; that means, we will take the experimental prototype inductor, capacitor, input voltage, output voltage, switching frequency, and the load resistance. And this we have discussed multiple times. And this is the architecture of digital voltage mode control.

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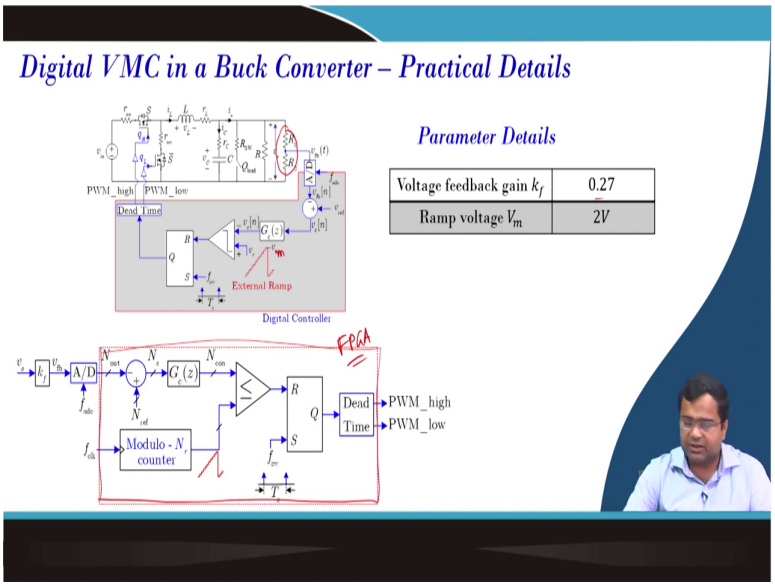

Then we also considered the feedback voltage gain which is 0.27 and we discussed a ramp with a voltage of 2 volt that ramp is the VM. The VM ramp voltage and we have also

discussed this Verilog HDL synthesis of this; that means, we have kept in an FPGA device that implementation also we have discussed multiple times with live video demonstration.

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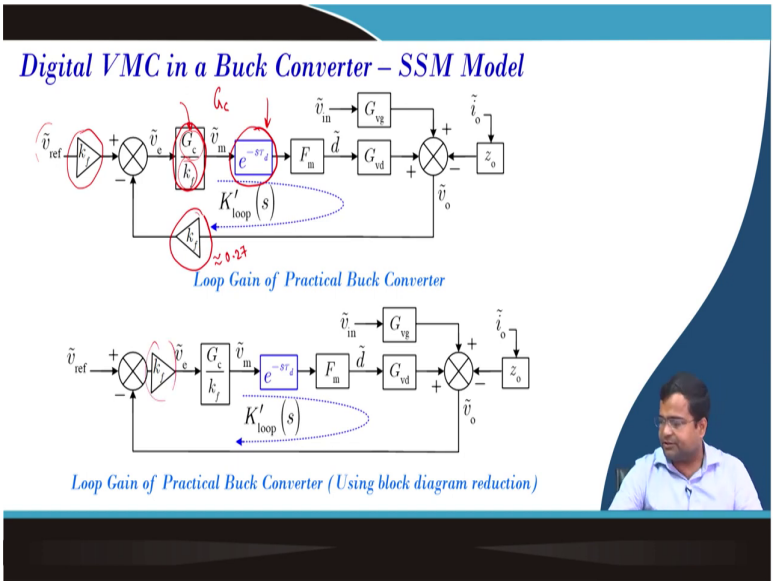

Now, here if we recollect our small signal model of a digital voltage mode control. We have discussed I think in lecture number I believe it is in the 5th week lecture where we have considered one particular thing. We have a feedback gain which is of a practical converter and this is approximately 0.27 that we have considered and we have to accordingly scale this reference voltage.

So, this is also there and this controller, because if you multiply this whole thing then k f k f will get canceled and it will be our original design which we have considered in week 5, where we have not considered any feedback gain, but here to be consistent with the hardware we have considered k. So, whatever design will come without any feedback has to be scaled by this. So, that sorry the hardware implementation; that means, this quantity inside this will go to the hardware implementation ok.

So, we have to consider this Gc. So, this Gc we are talking about will go to FPGA, and a multiplexer of this k f will be in your actual look like an original gain. And here we will consider you know this delay and this delay we have considered sampling delay conversion time everything and we have also discussed that if we consider our traditional small signal model continuous time and incorporate this delay then it will be reasonable to design the digital voltage mode control. Though it may not capture the first-scale instability.

But this is good enough when you design the control using a small signal model up to 1 10th of the switching frequency. And this is the loop transfer function for the block diagram reduction you can k f is now placed here and now we are talking about the loop transfer function.

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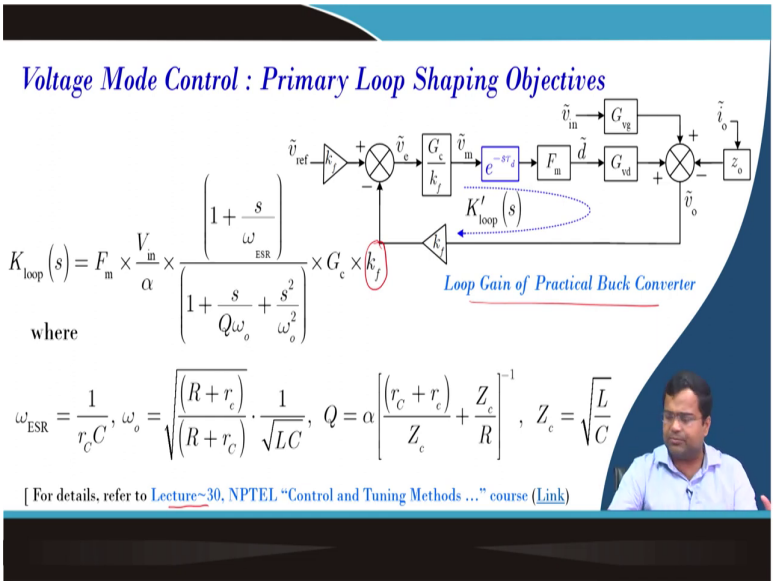

Now, if you consider the loop transfer function. Now, this k f gain comes into the picture and the practical buck converter we are talking about and we have discussed in lecture number 30 in our earlier NPTEL course the design method of digital voltage mode control.

How does the loop transfer what is the objective of the loop shaping objective all these things we have discussed already?

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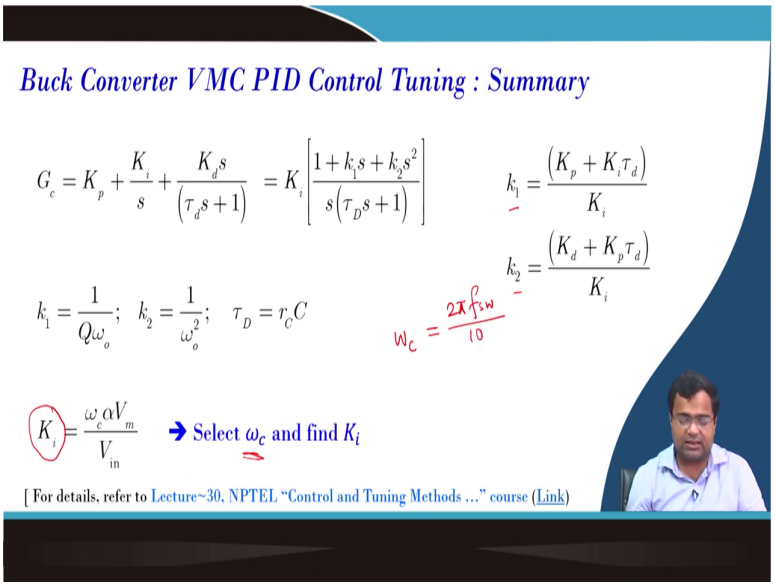

Now, we have discussed in lecture 30 also how to design a digital PID controller using stable pole 0 cancellations. And we are not going to repeat this, but if you find k1, and k2 for stable pole 0 cancellations and this Ki of the integral gain continuous time integral gain will be coming from the crossover frequency and typically for voltage mode.

We choose that 2 pi fsw by 10, 2 pi fsw by 10, and 2 pi fsw by 10 is our typical cross-over frequency.

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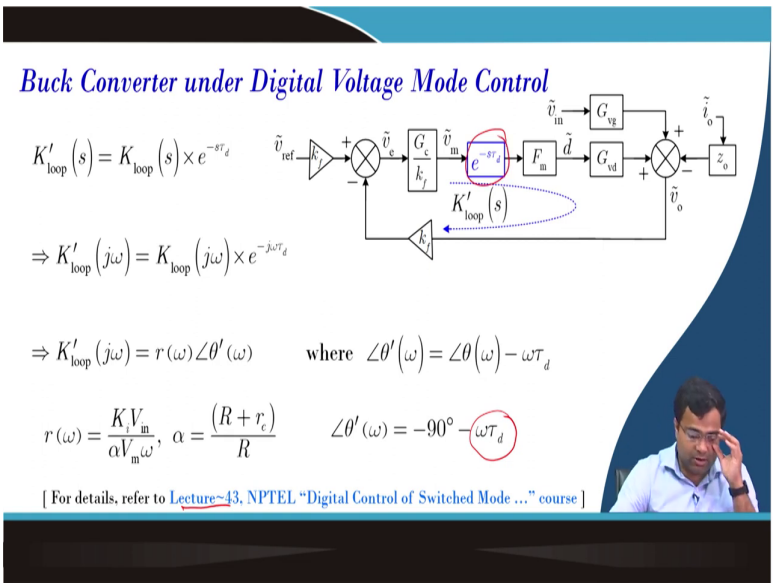

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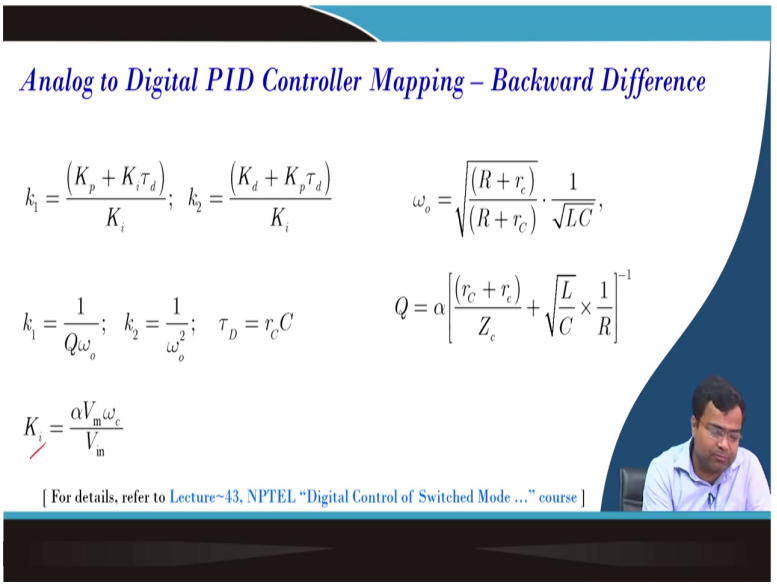

And we have discussed in lecture number 43 in this course the design of digital voltage mode control using the continuous time frequency response along with an additional delay due to this particular term and we have discussed by using both you know stable pole 0 cancellation. We have discussed in lecture number 43 how to get this Ki value.

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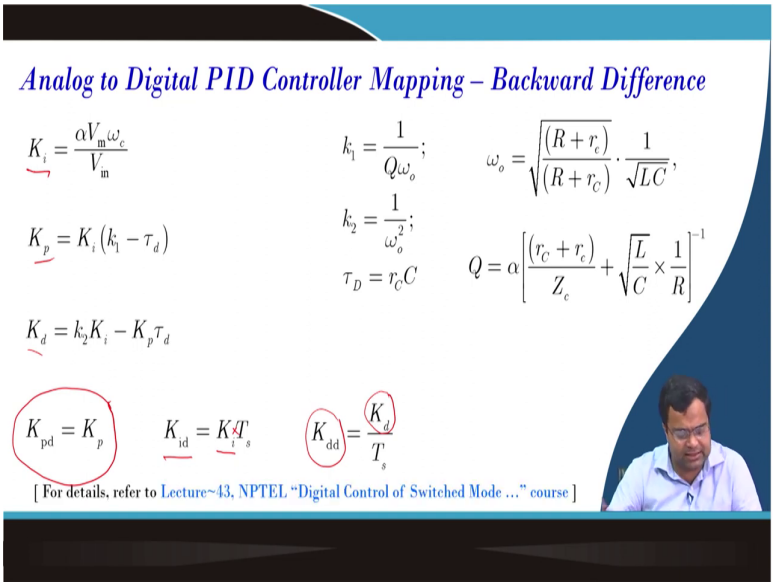

Then from this Ki and k1, k2 tau d how to get back the actual Kp, Ki, Kd and these are continuous time integral gain, continuous time derivative, gain continuous-time proportional gain then how to get back the discrete time proportional integrand derivative gain. And we

know that proportional gain will not change whether it is in continuous time or discrete time, but integral gain in discrete time will be simply integral gain in continuous time into the sampling time in this case it is the same as the switching period.

And the derivative gain in the discrete domain will be simply continuous time discrete derivative gain divided by the sampling time. And this we have discussed in lecture number 43.

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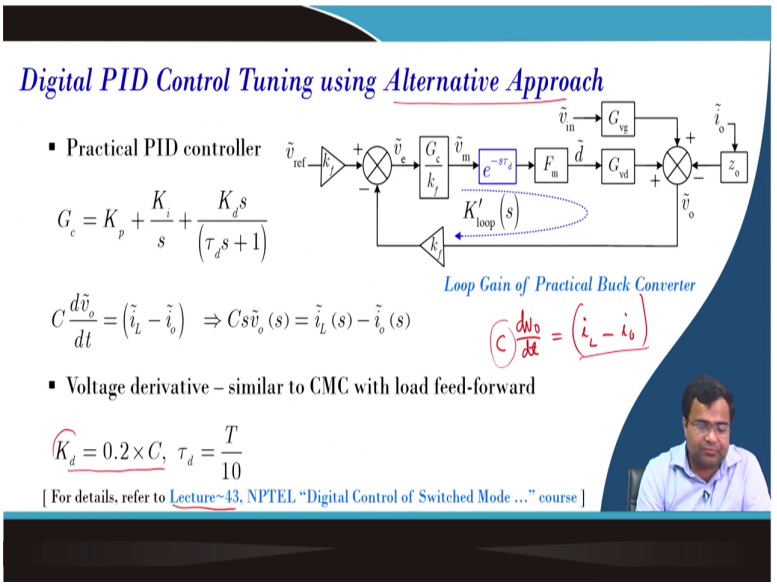

So, we have also discussed another alternative approach. So, this was an earlier stable pole 0 cancellation. And which is highly sensitive to resistance and all and we will see when you go for output impedance shaping this method may not be the right way.

Because, when we are talking about the closed-loop output impedance. In this technique, we have discussed that if we treat the voltage derivative similarly because the derivative of the output voltage in a buck converter will carry the information of both load current and the feet you know inductor and load current because we know that d V0 dt C dV it is equal to iL minus i0.

So; that means if we take some fraction of the capacitor as a derivative gain then carries a fraction of the capacitor current which is nothing, but inductance load current. And we want to utilize this concept for the design of the digital voltage mode control. And As discussed in

lecture number 43 in order to design we typically take the continuous time derivative gain mmaybe0.2 times the capacitor value. Tau d is the time constant of the derivative filter.

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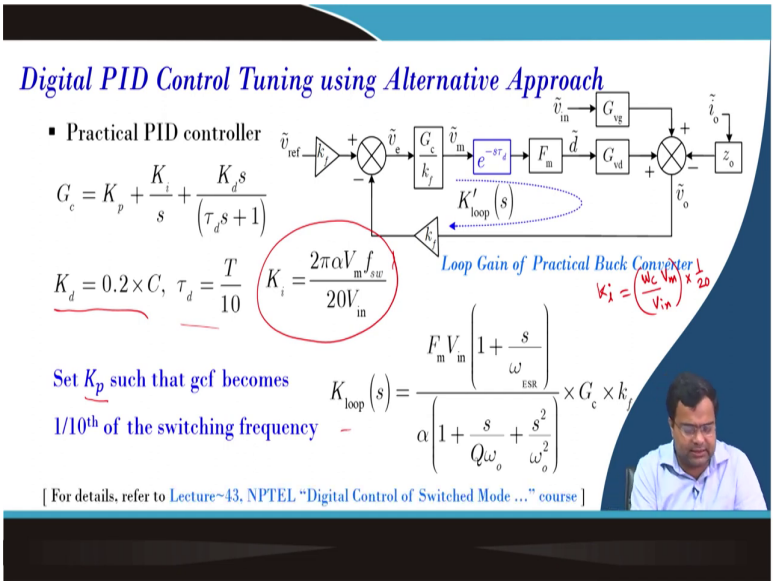

Then we have also discussed in the process of the design if we set Kd tau d and Ki to be 120th of the switching I mean you know typically Ki we take here we are taking omega C divided by I would say you know we have discussed that omega C then Vm by Vin something like that. So, this we have discussed. And here we are taking this divided by 1 20th of the switching frequency.

So, this we have discussed and this is what is coming here. And there is an alpha term. Now, if you design this then we have to choose select Kp such that the loop transfer function of the cross-over frequency reaches 1 10th of the switching frequency. So, this is the loop transfer function and this is discussed in lecture number 43.

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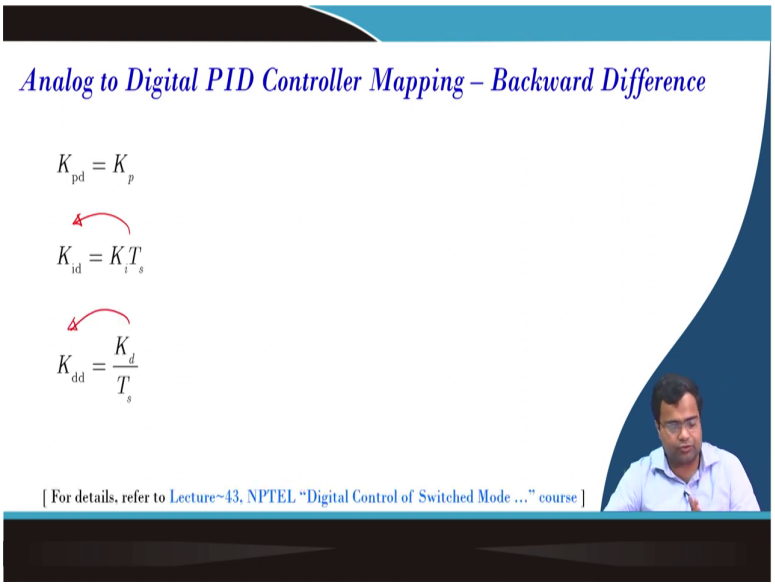

So, if we also know how to map the continuous time gain into discrete time counterparts their discrete-time counterpart for proportional gain is the same this is also discussed in 43.

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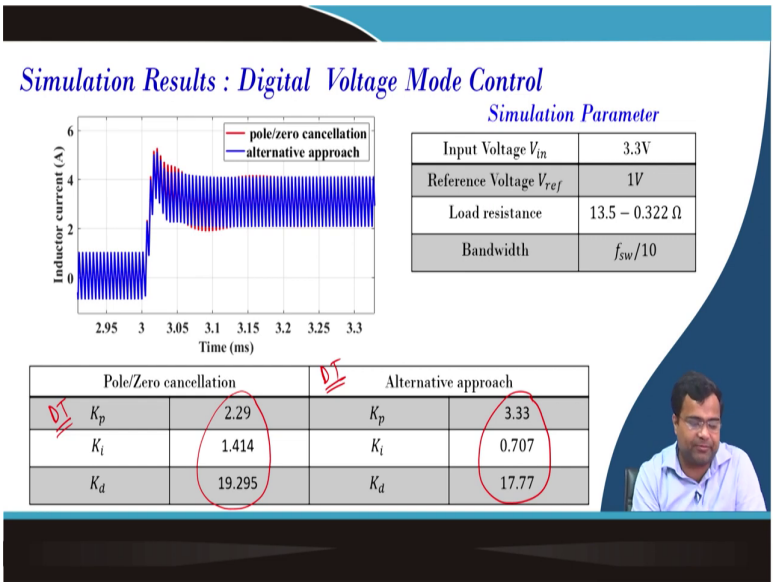

Now, we are showing a simulation case study. So, first, we are considering an input voltage of 3.3 volts. Output 1 volt and we are making a load transient from where load resistance is changing from 13.5 to 0.23 ohm; that means, a load step size of around 3 ampere and we got for pole 0 cancellation the design Kp, Ki, Kd in the discrete-time. These are all discrete-time I would say discrete time gain these are all discrete-time gain discrete time gains.

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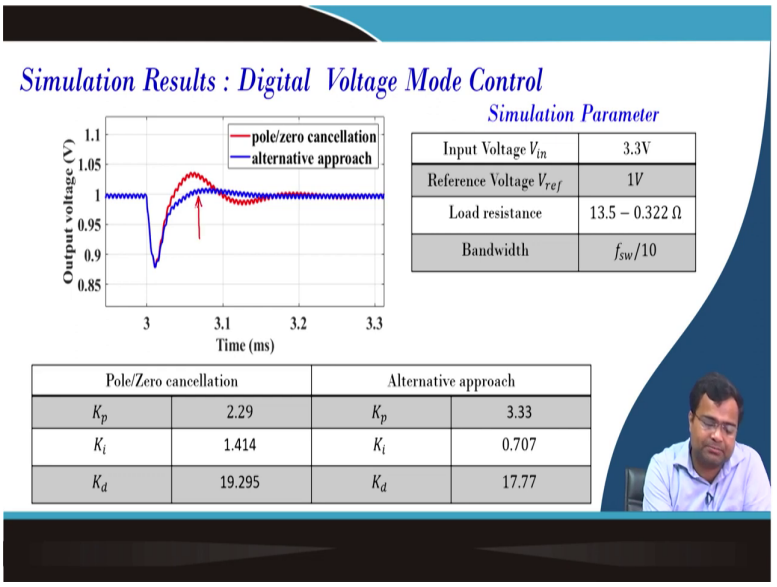

So, we are getting Kp, Ki, and Kd in pole 0 cancellations like this. An alternative approach like this and this is the load transient performance of the inductor current and if you do the same thing for output voltage you can see the alternative approach can achieve a much better load transient response because we are treating it like a current mode control with load feed forward some information. So, you can get a very nice load transient response compared to that in pole 0 cancellations.

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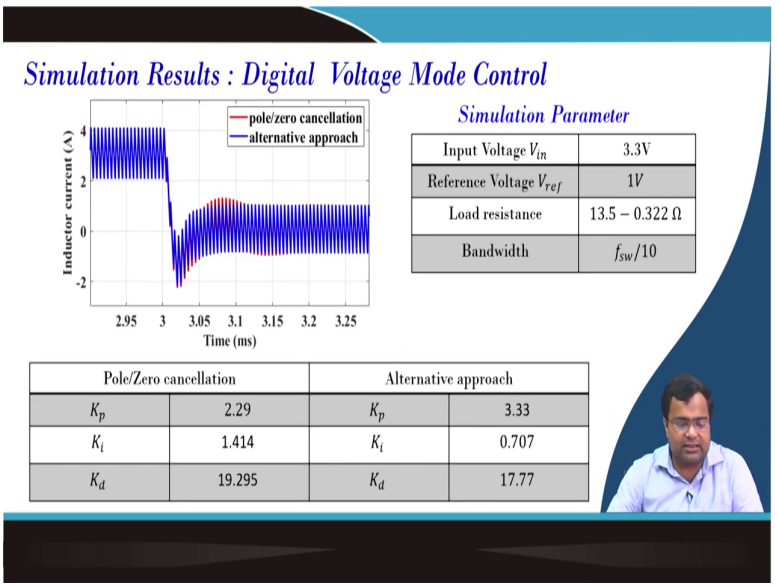

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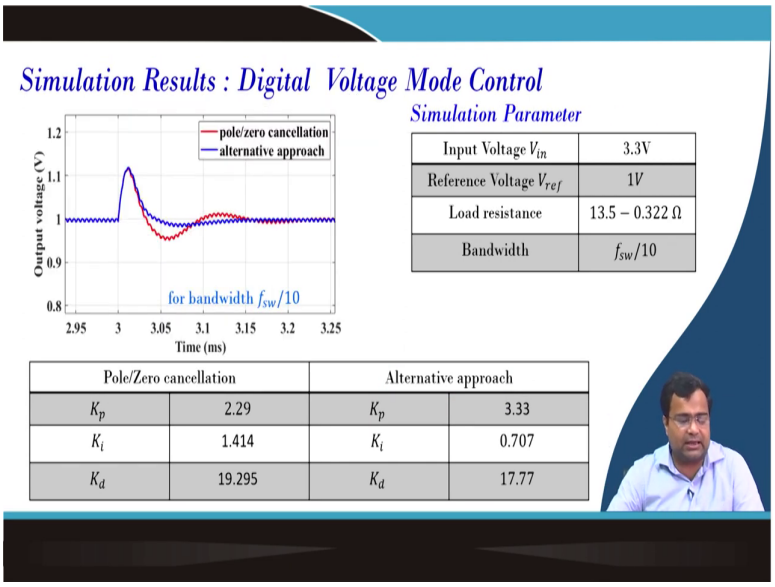

And also this method is more insensitive because it does not consider any pole 0 cancellations. And this is the step-down transient and you can see the step-down transient also alternative approaches much superior.

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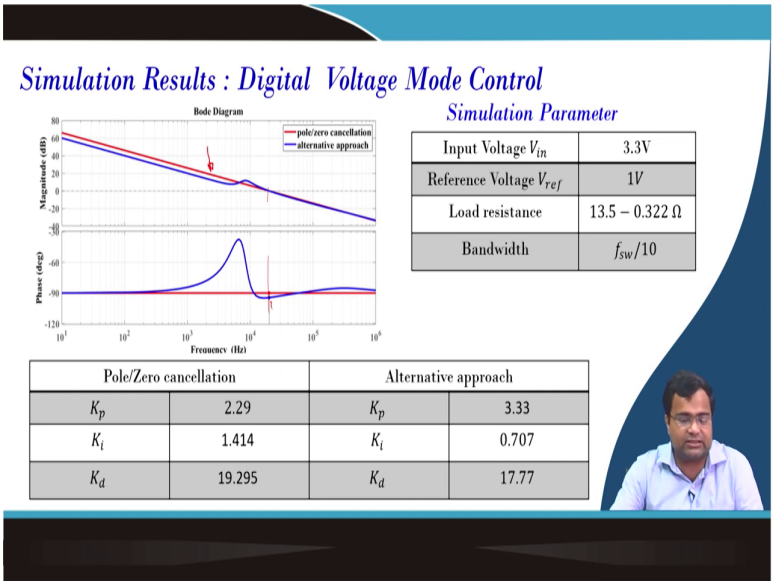

And this is the bode plot. So, in stable pole 0 cancellations, we are trying to get a first-order loop transfer function, but this is highly sensitive to load resistance and which practically is not possible.

But in the alternative design approach, we are getting more or less than 1 10th of the switching frequency and we are getting a reasonably good phase margin. And we will show in the next lecture that if you talk about the output impedance. So, this alternative approach is much superior and it is more or less insensitive to the load resistance variation.

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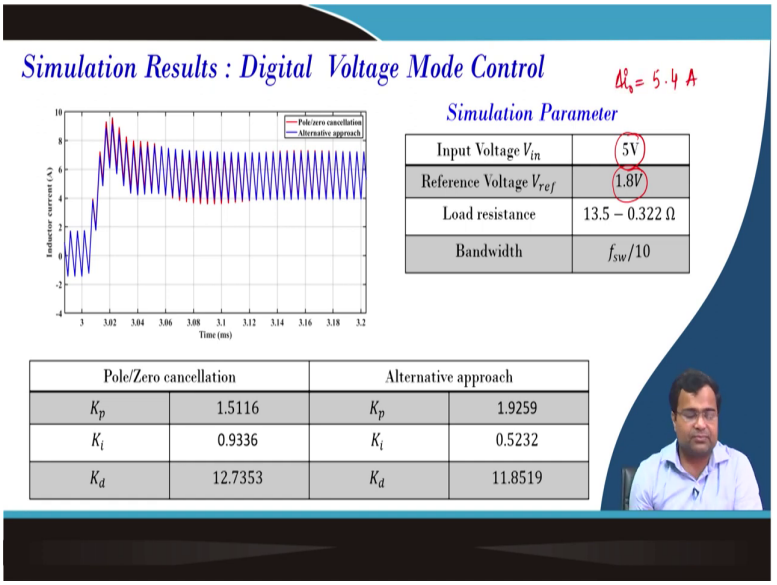

Now, if we show another case study. If the input voltage is now 5 volt and the reference voltage is 1.8 volt and we kept the same load resistance of the buck converter.

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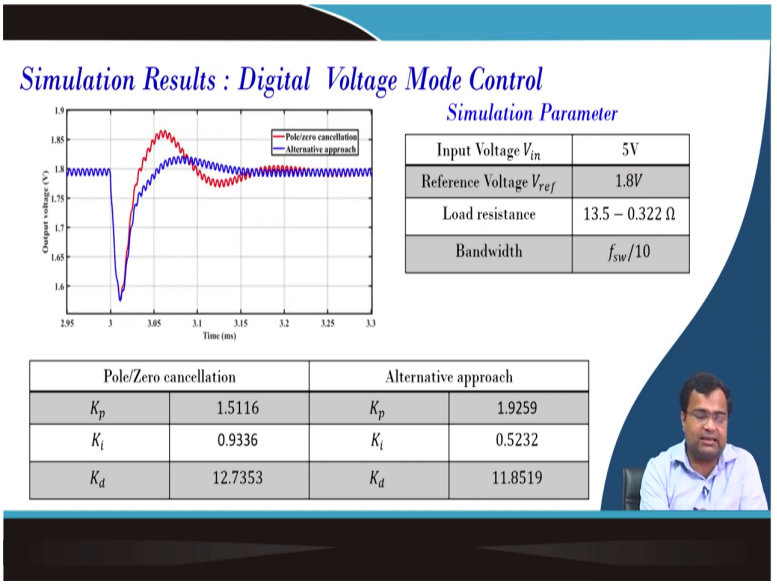

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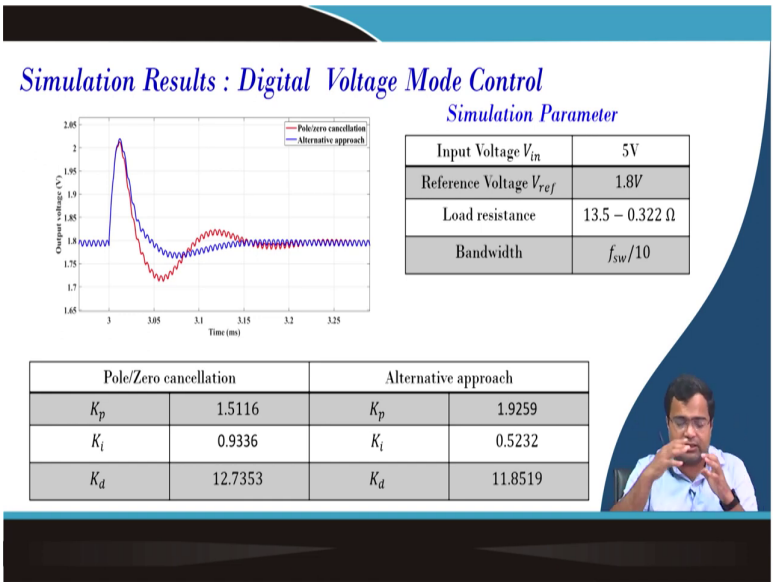

Now, in this case, the load step size will be just you know it will be 1.8 times; that means, it will be 5.4 ampere delta i0 size. And this is the load transient response in both approaches and you can see the alternative approach is much superior to the pole 0 cancellation these are the design parameter and we will be using this parameter, particularly this alternative approach for the experimental case study.

And this is the step-down transient response and it is far superior whereas, the stable pole 0 cancellation is sort of oscillatory, because exact cancellation is not possible. And it cannot dampen out properly when particularly in the light load condition when the load resistance is high.

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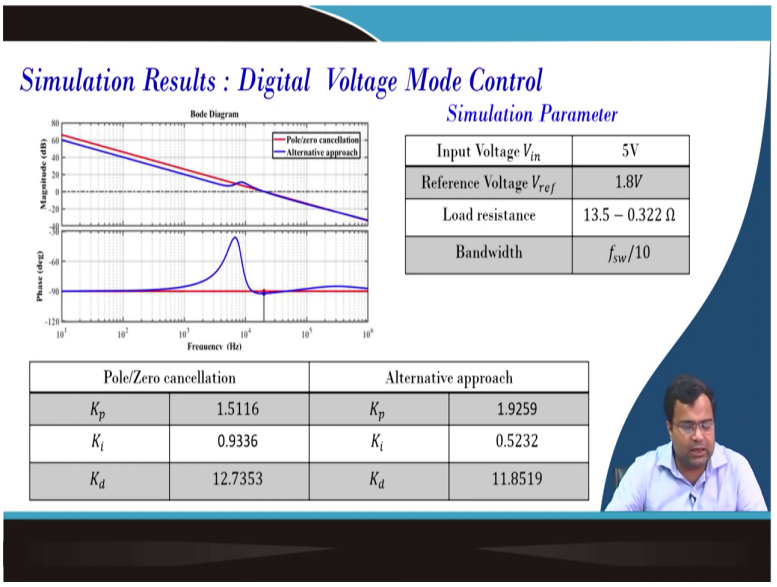

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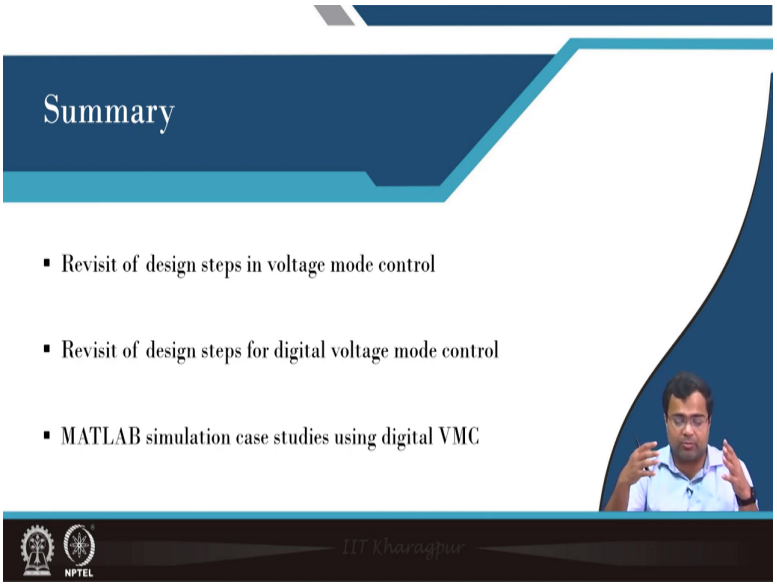

And this is again the loop transfer function. In summary, we have discussed we have revisited the design step of voltage mode control. We have also summarized the design step of digital voltage mode control and we have considered some simulation case studies of under digital voltage mode control of a buck converter with a similar parameter power stage parameter which we will be considered in the experimental case study. That is it for today.

Thank you very much.