**Digital Control in Switched Mode Power Converters and FPGA-based Prototyping**

**Dr. Santanu Kapat**
**Department of Electrical Engineering**
**Indian Institute of Technology, Kharagpur**

**Module - 11**
**Design and Validation of Case Studies using DVMC and DCMC**
**Lecture - 101**
**MATLAB Simulation of a Practical Digital VMC Buck Converter in CCM**

Welcome. In this lecture, we are going to talk about MATLAB Simulation of a Practical Digital Voltage Mode Control Buck Converter in Continuous Conduction Mode.

(Refer Slide Time: 00:33)


So, far we have shown experimental demonstrations; we have shown the steps of how to do hardware implementation or prototyping using FPGA. We have shown detail about the Verilog coding we have presented experimental results. In the previous week, if you recall a lecture in week 3, we presented the detail of the MATLAB model ok.

How to develop a MATLAB model for mixed-signal current mode fully digital voltage mode control? Now, the next question is very obvious after having so many MATLAB model and experiment what is the ultimate purpose of modeling and design? So, unless the model is used to you know predict.

I mean it helps the designer to come up with a unified way where you can you know justify stability, you can develop a strategy for controller design, you know for various control strategies. Then for a given control strategy what should be the choice of control parameter?

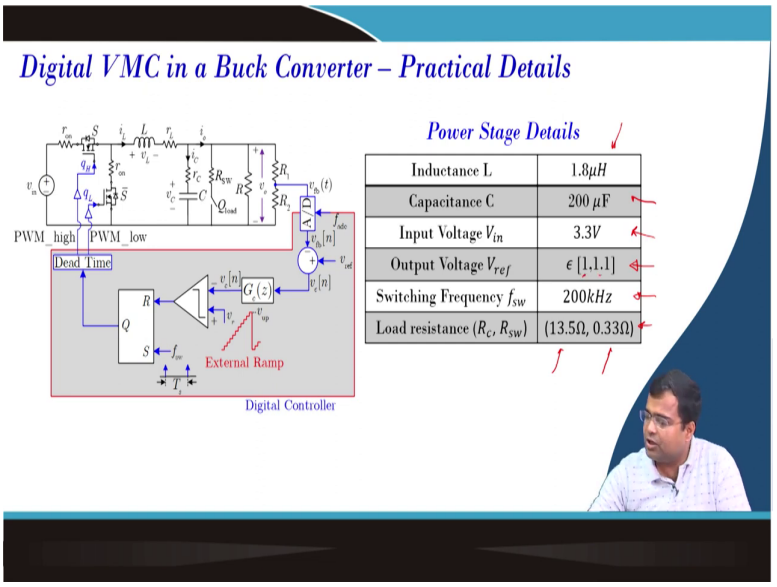
For example, in voltage mode control what should be the controller gain? Digital PID controller gain. So, to ensure, because every time we cannot go to the hardware check does trial and error. This is a very costly affair and time-consuming affair. Most of the designs one of the main requirements is saving time; that means, you need to save your know time in the process of design iteration, because everybody wants a very fast time to market.

So, this lecture is going to consider whether can we develop a realistic MATLAB model of a practical buck converter. And then can we check what the simulation result looks like when we operate under the similar condition of an experimental kit and how do you compare them are they close enough? If they are close, then before we do actual experimentation we can use our concept of modeling, we can design that part will be discussed in the subsequent week.

Then we can quickly come to the controller parameter value and then we can plug it into the actual hardware. So, that is the objective in this of this lecture we want to first consider revisiting our digital voltage mode control in some practical detail. We have to develop we have to consider all the realistic voltage gains, then what are the controller gains and we want to include this in the MATLAB model.

So, that MATLAB model now will become a more realistic buck converter, but we did the basic simulation with all ideas even practical, but we have not considered the voltage step-down gain, we have not considered the other aspect. So, this time we are going to consider. Then we want to make a comparative simulation and experimental case study. And in the subsequent lecture also want to show how to plot both simulation and experimental results in a single plot. And then only the comparison will be more useful and meaningful.

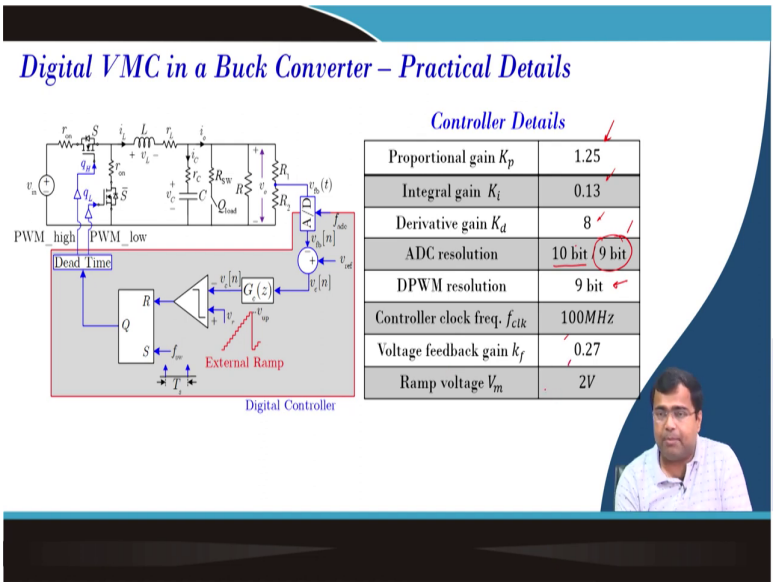
(Refer Slide Time: 03:44)




So, in this lecture I mean in the few subsequent lectures we have discussed that in the prototype we have considered to be 1.8 microhenry inductor, and 200 microwatt capacitor and we are going to test the load and reference transient performance under 3.3 volt input at 3.3 volt input for load transient we are considering nominal voltage to be 1 volt output, switching frequency is 200 kilohertz and for load transient, we are varying the load resistance between 13.5 which is a continuous resistance.

And then we are considering a switch resistance, which will be 13.5 in parallel with 0.33. So, this 0.33 resistance is the switch resistance if the Q load is high this will come in parallel with Rc, if the Q load is 0 then this will be disconnected. For reference transient, we are going from 1 volt to 1.1 volt. So, let us go into detail.

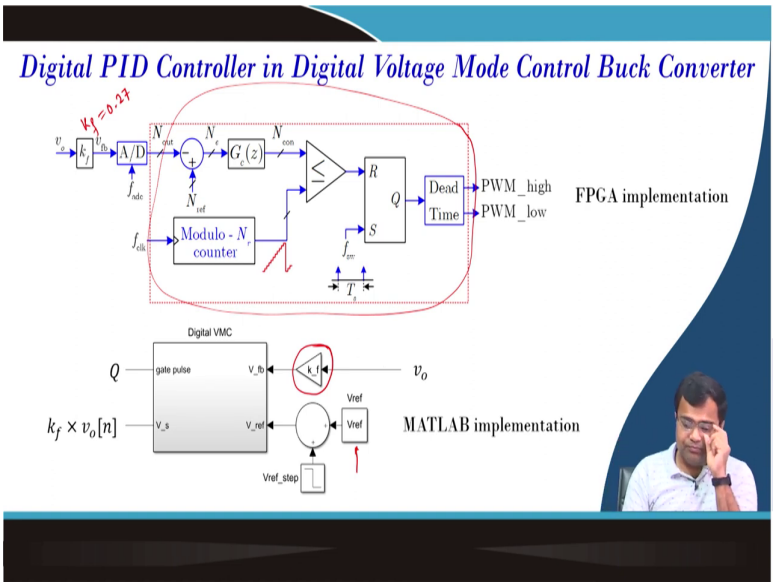
(Refer Slide Time: 04:41)




So, we are setting the proportional going to be 1.25, the integral to be 1.3 derivatives to be 8 and we have discussed the hardware implementation in using Verilog. Though we are using 8-bit ADC, but we are discarding 1 bit to avoid any limit cycling effect and the DPWM resolution is set to 9 bit.

So, here it looks like it is the DPWM resolution is the same, but you know we are not getting very significantly significant problems of limit cycle, but you should choose a DPWM resolution much higher than the ADC resolution. So, for effective resolution in the ADC we are using 9 bits we can drop one more LSB. Here, we are dropping 1 LSB from 10-bit its resolution becomes 9-bit. We are using a controller clock of 100 megahertz and voltage gain of 0.27 and a ramp voltage of 2 volt.

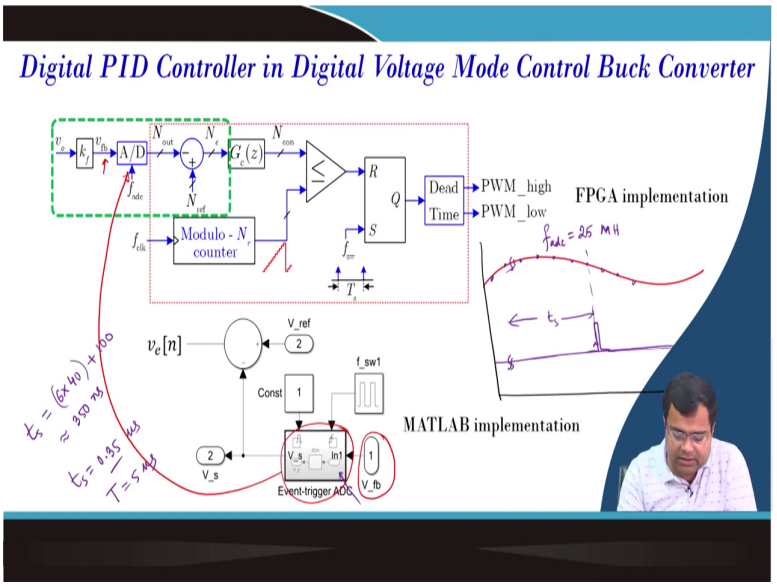
(Refer Slide Time: 05:32)




Now, this is the block that we want to implement inside the FPGA. This will be sitting there. So, how does this block with our Simulink model? So, if we remember our digital voltage mode control I think we have discussed it in lecture number I believe 26 or 20 sorry 25 or 24. We have multiple lectures in the 3rd week which consider digital voltage mode control.

So, if we recall digital voltage mode control. So, we are now we have earlier considered V0 directly, but now there is a step-down gain and this is k f is nothing but 0.27. So; that means, we are the first step we are incorporating the feedback gain. And accordingly, we have to select the reference voltage, because earlier when there was no feedback gain the reference voltage should be the one where exactly you would want the output voltage.

(Refer Slide Time: 06:30)




Now, I have to consider the scaling factor also next. So, the error voltage after the feedback is the feedback. So, here the feedback voltage is then we are using an event trigger ADC and this is what is similar to this. So; that means, we are taking the sample at the rate of the switching frequency; that means, we want to capture.

You remember if we take this output voltage profile; that means if you take the output voltage profile and if we consider the output voltage sample multiple points and we have discussed that if your switching clock comes here; that means if this is your switching clock come here like this.

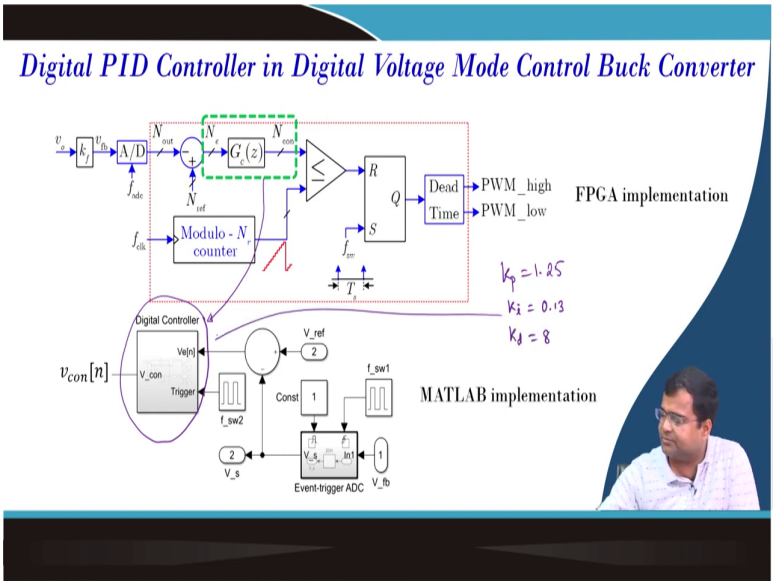
So, if you capture the output voltage data here. Actual data is 1, 2, 3, 4, 5, 6 maybe 6 cycles earlier ok. Maybe this is not the clock, because otherwise, it will be too slow. So, this is the point we are capturing ok. So, we can capture the data. Where are we capturing?

So, here we can introduce a delay we have discussed the sampling delay can be introduced to make it consistent and since we are using a pipeline ADC; that means, we are considering 6 cycle delay and we are using a 40 megahertz ADC clock sorry 25 megahertz ADC clock not 40.

So, that is my 8 ADC. So, for our total delay for convenience, we are taking 6 into 40 nanosecond plus there will be some additional driver delay and all. So, we are taking roughly 100 total we are talking about around 350 nanosecond we are taking. So, considering 350

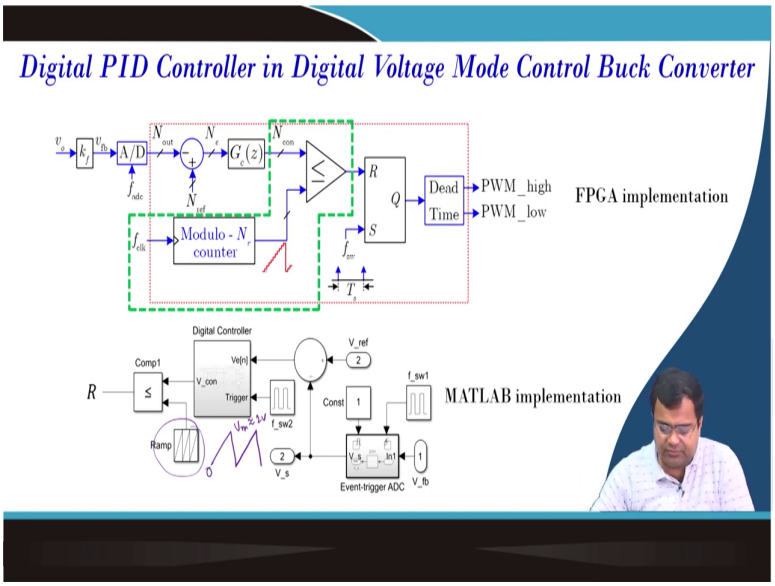
nanosecond is the delay. So, our ts is we are using 0.35 microsecond, where our switching period is 5 microsecond. So, this is also captured and the delay is considered here.

(Refer Slide Time: 08:50)



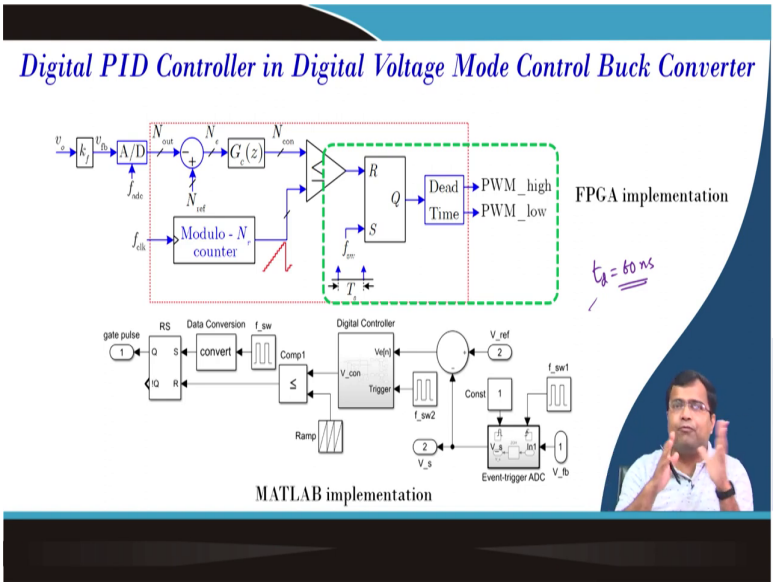

Next the controller, controller we know how to implement this controller using the custom model for k p ki k d that also we have discussed. So, I am not going to repeat it and we are setting the controller gain according to KP equal to 1.25 that we have discussed a discrete-time controller gain 1.3 and a discrete time derivative gain of 8. So, we will set those values inside here.

(Refer Slide Time: 09:21)



Then comparator we have considered this ramp, but we are not talking about the resolution effect we can add it, but we have just considered the sawtooth ramp. It is varying between 0 to Vm, Vm we have taken approximately 2 volt.

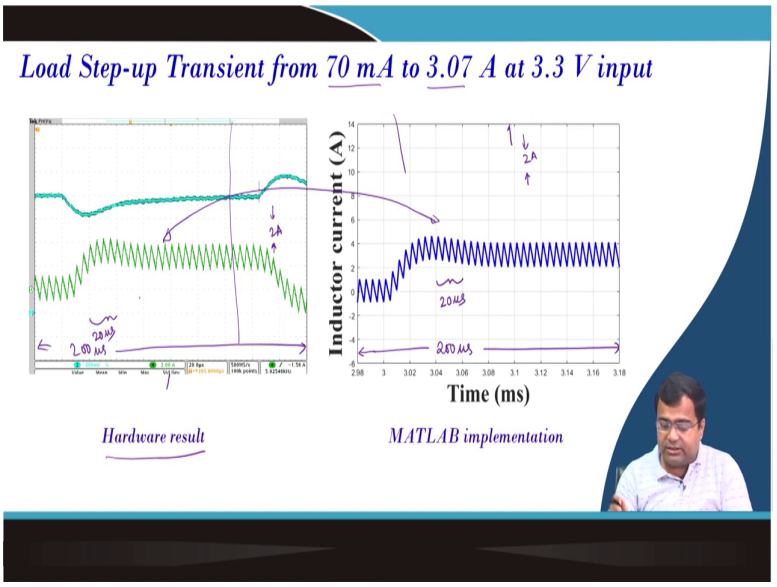
(Refer Slide Time: 09:40)




Then we have considered this saw tooth dead time although we are talking about ideal in the simulation we are talking about ideal synchronous buck no dead time is given in MATLAB, but practically there is a dead time, and that dead time we are giving dead time to be roughly around 60 nanosecond ok.

So, that is why it is expected there will be a slight deviation due to this dead time effect which is not captured. You can do it more realistic simulation, but this is just for understanding how far they are closed.

(Refer Slide Time: 10:08)

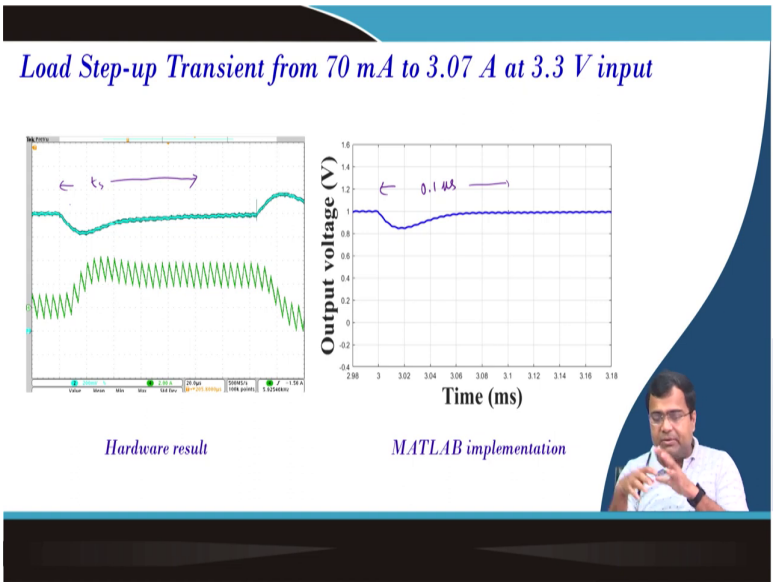



Now, we want we are making a load transient from 70 milli ampere to 3.07 ampere at 3.3 volt input. So, this is our experimental result and these are simulations of just the current waveform. You can see here the time division is 20 microsecond so consistently we have also considered 20 microsecond.

So, it should visually look like same. Here you can see the voltage resolution it is showing sorry here is the inductor current. So, 2 ampere here also if you see the current waveform here to here also 2 ampere so, we kept the same scaling the time. So, this tooth is like 200 microsecond which is also consistent with the hardware. You see the current waveform here we are making just step up this step up.

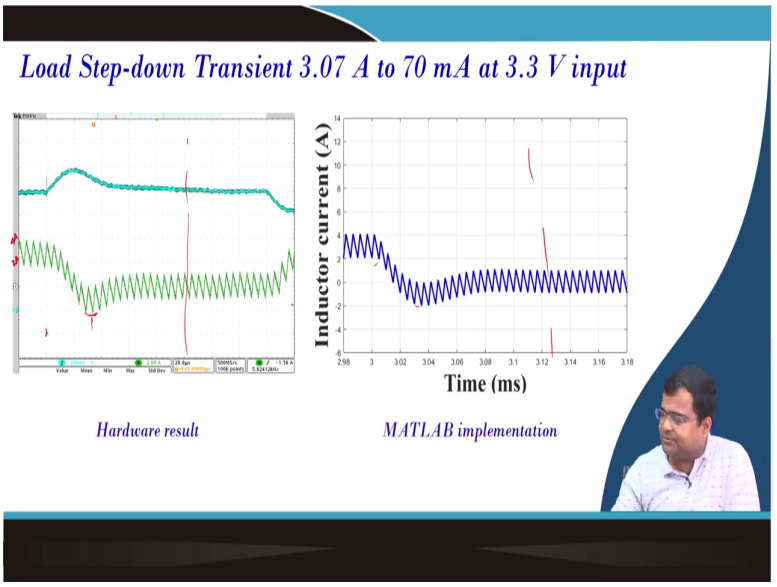
So, ignore this part, but if you match this to this they are quite representative; that means, this is the first step.

(Refer Slide Time: 11:27)




Now, in the same condition, I am showing separately the output voltage. So, you see the output voltage also matches quite nicely in terms of the recovery time. Like here it is taking like up to this; that means, it is taking like 0.1 you know micro second roughly. If you take here is 1, 2, 3, 4, 5. So, it is also coming to be 0.21 microsecond. So; that means, they are quite representative.

(Refer Slide Time: 11:59)

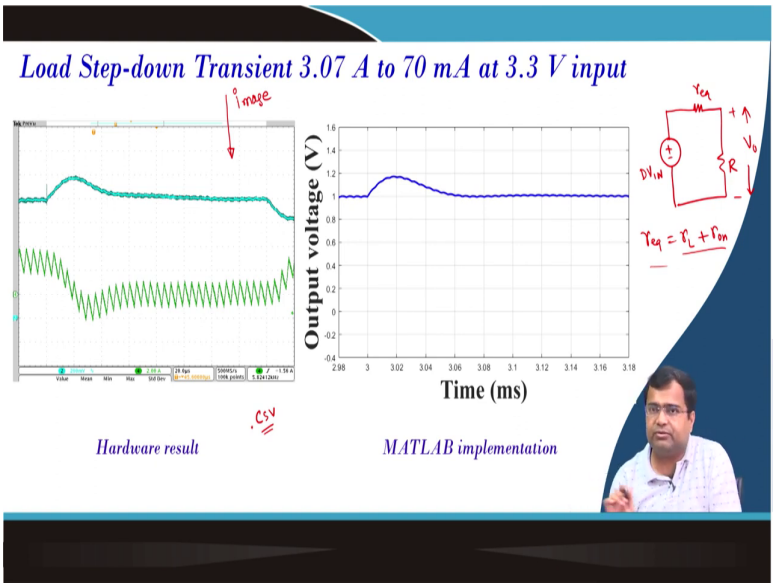



Now, we are going to see load step-down transient, where the current is now coming from 3.07 to 70 milli ampere, 3.07 ampere to 70 milli ampere same condition. So, we have

maintained the same time scale. Now, we are showing step down. You see when we apply step down it is taking kind of one-cycle delay it is happening and you can see this is coming around from here to here roughly how much? Around close to like 35.

So, it is also coming like this; which means, the profile of the inductor current if you consider up to this point looks quite representative and here you see this is 2 ampere, this is 4 ampere this is also 4 ampere 2 ampere. So, the ripple is also matching, and if you see the output voltage during the step-down transient. You can see that the current profile we have already matched, and the voltage profile is also quite matching.

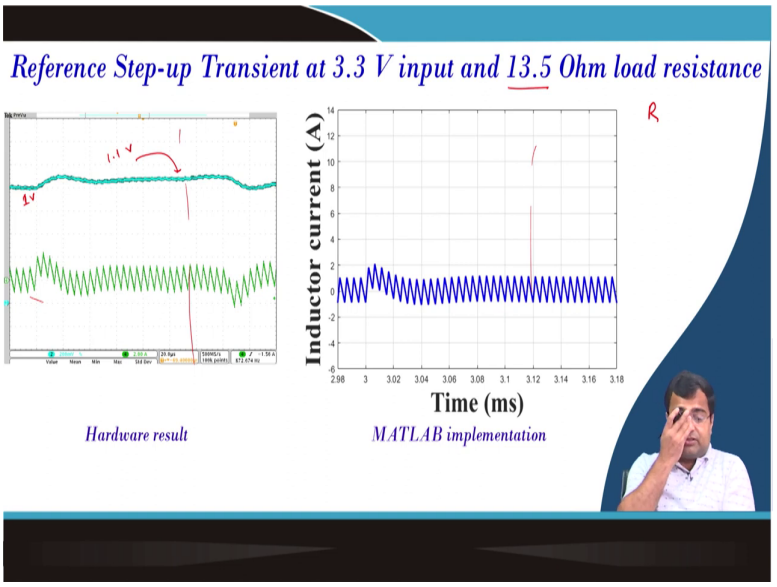
(Refer Slide Time: 12:53)




And in the subsequent lecture, we want to actually because here we have captured as an image right. We have taken the image of the result, but if we take the dot CSV file then we will get a data file then we can compare with the MATLAB data and the experimental data that we are going to consider in the subsequent lecture because before that we have to tell the step for taking CSV file and running and then you know capturing the signal then running in your; that means, post-processing those things we will discuss in the subsequent lecture.

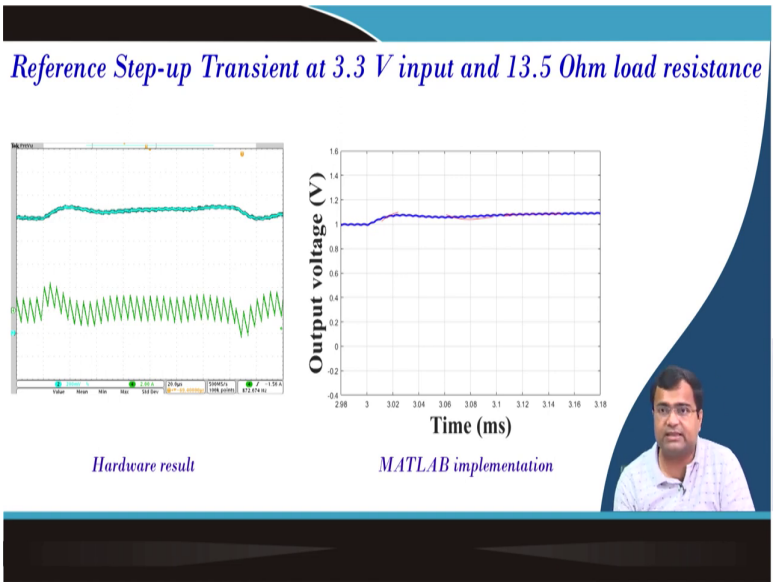
But here we are just keeping the image of this experimental result and the same output voltage.

(Refer Slide Time: 13:48)



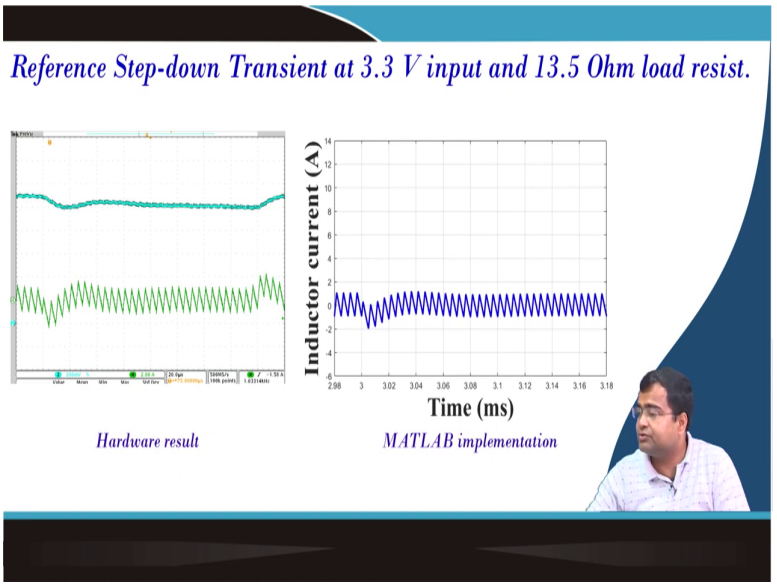

So, here is the reference transient and you see interestingly reference transient we are operating at 3, 13.5 ohm resistance which is my load resistance and it is undergoing a step-up transient from 1 volt to 1.1. So, this is 1 volt to 1.1 volt this is going here. If you see the current profile if you look from up to this point there, because we are only applying step-up transient they are quite you know similar quite representative.

(Refer Slide Time: 14:18)



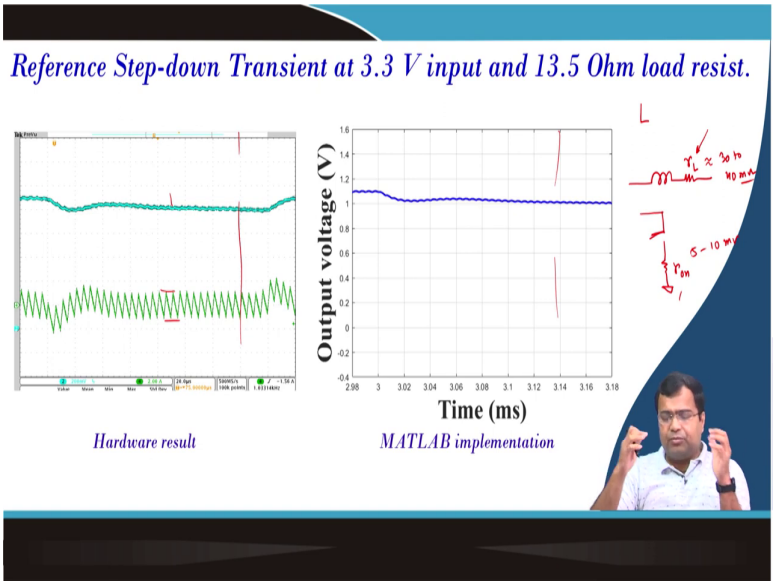

And if you see the output voltage profile. So, there is an initial kind of slight overshoot undershot and then it is coming. So, it is also the same then the same scale.

(Refer Slide Time: 14:30)




And if you look at the step-down reference transient, it also looks similar to that current profile looks quite similar and if you go to the output voltage profile that is also matching nicely.

(Refer Slide Time: 14:43)




So, it means; that means, I am talking about up to this portion because we are not applying any step up which means the experimental and the simulation results they are watching closely. So, which means we can capture the practical aspect but to get this model we have to

struggle because in the actual we know the inductor value that can be obtained from this current ripple.

We measured the capacitor value which was quite ok. That was 200 microfarad although there can be some degradation in the capacitor if we ignore that effect, the challenge was you know inductor will also have a dc resistance right which is RL then the switch we have considered the MOSFET right; that means, if we take a MOSFET we have to consider the r on. So, rds on still some information will be available in the datasheet which was ok.

But getting this RL was very difficult and we have to sort of run multiple case studies to come to a close conclusion that what will be the realistic value of RL, but one can try out the identification method; that means, we can do parameter estimation and all, but I am not going to present this parameter estimation method. Here it is more like an iterative way to validate how much the RL and r are on because r on we are getting around 5 to 10 I think milliohm.

But this we are getting close to 30 to almost 40 milli ohm for the r on RL for the inductor and the dc resistance of the inductor. So, this was a difficult task, because if you cannot match the damping ratio will be different, because if you go for the output impedance will be heavily or highly affected by the parasitic inductance and resistance, because we know that if you take the high frequency and the low-frequency behavior the inductor high frequency will be low-frequency inductor will be shorted, but it's parasitic will come ok.

Because, effective r equivalent circuit in the previous lecture in the previous course NPTEL course, because if we get the equivalent DC model right. So, the DC equivalent model we have discussed this DC equivalent model D into V in then we have to consider this r equivalent, and then it will be r ok. So, the output voltage will not be simply V0 it is a DC equivalent circuit because we need to consider this r equivalent and this r equivalent is nothing, but inductor DC here plus r on.

If we consider synchronous buck and if we consider the on-state resistance of the high state and low state MOSFET are the same, then we can represent. So, getting these values are very difficult, and we have used some procedure to do checking by running some DC equivalent case study and we got some reasonable value for this. And we have discussed the reference transient both step up and we can do step down.

(Refer Slide Time: 18:09)


The step-down transient also looks quite representative. If you take the voltage profile also that we have discussed. So, in summary, we have discussed some digital voltage mode control practical detail. We have discussed some realistic MATLAB models and we have shown some comparative simulations and experimental case studies. So, in the subsequent lecture these results we want to plot these in a single graph.

That means we want to take the CSV file of the experimental data and also want to capture the data in MATLAB and we want to plot in a single graph and show what the current profile looks like. And will give us if we get reasonable matching between the experimental and the simulation which we saw is quite close then it looks like our models are well enough.

Now, you go to the design case study and in the subsequent lecture we will go to week we will go to the design of voltage mode and current mode control. And then that will be used as a tool for what should be the parameter of the controller and then we can design various types of control and we can plug in those values in actual experimentation. So, this process will be very important to the design and we do not want to validate it in the actual experiment. That is it for today.

Thank you very much.