Digital Control in Switched Mode Power Converters and FPGA-based Prototyping Prof. Santanu Kapat Department of Electrical Engineering Indian Institute of Technology, Kharagpur

Module - 01 Introduction to Digital Control in SMPCs Lecture - 10 SMPC topologies and Power Stage Design for Hardware Demonstrations

Welcome back. So, in this lecture, we are going to talk about Switch Mode Power Converter topologies and some Power Stage Design aspects of you know the converters which for which we are going to consider Hardware Demonstration.

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Power stage ofBuck and boo	esign aspects of buck and boost converters ost converters under steady-state in CCM and DCM
 Full-bridge L 	LC converter – basic operations for varying frequency
 Conventional 	boost PFC and totem-pole PFC for AC/DC conversion

So, here, we will be talking about the power stage design aspect of buck and boost converter and we will be talking about their steady state operation under continuous conduction mode as well as discontinuous conduction mode. Then, we will talk about some basic operations of the full bridge LLC converter which will be considered as a demonstration experimental demonstration using an STM 32 microcontroller and we will be also talking about boost PFC and totem-pole PFC. So, one totem-pole PFC case study will be considered using the C2000 series microcontroller.



So, if you take a buck converter in continuous conduction mode, this waveform is known and if we take the ripple parameter, the inductor current ripple can be expressed in terms of input-output voltage and the on-time ok.

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Now, if we want to consider the ripple voltage up capacitor voltage, then using charge balance, we can get this expression can be obtained in terms of on-off time and this is discussed in lecture 7 in our earlier NPTEL course.

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Now, under pulse width modulation, when the on-time and off-time sum is fixed that is our switching period, and on time is D times the period and off-time is 1 minus D time, then we can write the ripple parameters in terms of this, where we are talking about a voltage regulator, where output voltage ripple will be fixed.

Now, this ripple will be maximum when the D is minimum; that means, this D is minimum and this D minimum means the input voltage is the maximum because we are regulating the output voltage. Similarly, the output voltage ripple will be maximum when D is minimum. So, both worst case conditions will be the highest input voltage, where the current and voltage ripple will be maximum and this we have discussed in lecture 7 in our earlier course.

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Now, if we talk about the RMS value how to compute for a piecewise linear waveform as we have discussed in lecture 7 in the earlier course that we can derive using integration. This is the expression, where these are the x 1, x 2, x 3 and it is a repeating periodic signal.

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Now, if we use this formula to find out the RMS current of the inductor current of the buck converter, it can be shown that it is the square of the load current that is the average inductor current plus delta L square by 12; where, delta L is the ripple current and here, for a given load current, that means if this is fixed, then it will be worst when the ripple is maximum

when the; that means, when the input voltage is maximum and higher the RMS current, more the conduction loss.

So, that is why if you go to any commercial you know the test cases of the efficiency curve, you will find the efficiency plot slowly you know gets reduced.

That means if you take the efficiency plot like this kind of efficiency plot if you take, for higher input voltage it will slowly come down and this loss is due to more conduction losses. And also there will be a switching loss increase for a higher input voltage. Now, for a given input voltage, the load current means the RMS current increases with the load current that is why in the efficiency plot on this side, the efficiency slightly decreases and slowly decreases because on that side your conduct, is dominated by the conduction loss.

And this side will be dominated by the switching loss under particular light load conditions. So, you will get to one point, where the losses will be minimized and the efficiency will be maximum. So, on either side your efficiency will fall; the right side will be dominated by conduction loss, and as you increase the load current this is the load current axis and this is the efficiency axis.

So, as we increase the load current, conduction also increases as well as as a result efficiency falls. So, the worst case RMS current will be the highest input voltage and highest load current when the efficiency of the converter should be lowest; that means, that is the worst case and that critical condition, we have to meet certain efficiency requirements and this is discussed in lecture 7 in our earlier NPTEL course.

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Now, in the design consideration, if we take a large inductor and a small inductor and this is under open loop condition, where we are made a load transient for a practical buck converter. It can be shown that a large inductor unit offers a smaller current ripple which may be good in terms of conduction loss point of view and also, output ripple will be reduced; but it penalizes in terms of undershoot because the slew rate of the inductor current is a small because of a higher inductor value.

Whereas, the smaller inductor, although it gives you a larger you know current RMS value sorry for the ripple; but it reduces the undershoot drastically because it happens in the lower higher slew rate. So, in the choice of power stage parameter, we need to be very careful about the choice of inductor and as well as capacitor.

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D	Design Consideration (Inductor) Large Inductor					
		Smaller ripple current $\Delta i_{e} = \frac{V_{o}(1-D)}{X} \times \frac{1}{2}$		vantages	Larger size (bulky inductor)	
	Iges	^L f _{sw} L Smaller RMS current			Slower transient response!!	
Advanta	dvanta	$\left(i_{\scriptscriptstyle L,\rm RMS}\right)^{\!\!2} = I_{\scriptscriptstyle O}^2 + \frac{\Delta i_{\scriptscriptstyle L}}{12}$	Disad	Higher voltage overshoot/ undershoot!!		
	A	Lower conduction loss				
		$\begin{array}{l} \textbf{Smaller voltage ripple} \\ \Delta v_o = \frac{V_o(1-D)}{8Cf_{sw}^2} \times \overbrace{\overline{L}}^{\widehat{1}} \end{array}$			Inductor should be carefully designed	

So, and this issue is discussed in lecture 7. If we take a large inductor the advantage will be current ripple will be smaller. So, the RMS current will be smaller and conduction loss may be reduced also voltage ripple is a function of you know this current ripple; that means, you know if you take the output voltage because the inductor is large. So, 1 by L., this will be smaller.

But the disadvantage is that bulky inductor the size will increase; slower transient response because if you go to you know subsequent, we have discussed in our earlier course that larger inductor will impose a limit if you take a voltage mode control the L c pole that will come even at a low frequency and it will be very difficult to compensate. Then, higher voltage undershoot and overshoot due to the larger inductor. So, you have to be very careful about the inductor choice.

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Smaller output voltage undershoot/ overshoot For details, refer to Lecture~7, NPTEL "Control and Tuning Methods" course (link)]	Design Consideration (Capacitor) Large Capacitor					
Image: State of the second	$\Delta v_{a} = \frac{V_{a}(1-D)}{2} \times \frac{1}{2}$	poor reliability				
Capacitor should be carefully selected	$\frac{^{o} 8Cf_{sw}^{2} L}{\text{Smaller output voltage undershoot/ overshoot}}$	Higher time and energy overhead during reference voltage transient				
[For details, refer to Lecture~7, NPTEL "Control and Tuning Methods" course (link)]		Capacitor should be carefully selected				

If you talk about the capacitor, if you take a large gap, it offers rs smaller output voltage ripple. It can alsreducees overshoot undershoot of the output voltage. But the size is bulky as well as the reliability will be poor also if you are talking about the devious, then this reference voltage changes because of the large gap; you have to change the large energy and that will cause higher current overshoot to undershoot. So, you have to be very careful about the selection of the capacitor and this we have discussed in lecture 7 in our earlier course.

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Now, the worst-case current ripple for the buck converter, if we consider it under pulse width modulation, will be worst at the highest input voltage that we have discussed. If you take constant on time, it will be highest; at the highest input voltage, the current ripple is the largest which is the worst-case current ripple. Under constant off time, it is independent of you know I would say input voltage. So, that means, it is insensitive and this we have discussed in lecture 23 in our earlier course.

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Now, the worst-case inductor current in a buck converter in continuous conduction mode is nothing but if you consider in CCM, worst-case RMS cRMSent. It is the same as your ripple current because for average RMS current is nothing but the average inductor current square plus RMS ripple current square by 12.

So, the analogy will be the same for this; the only difference since the load current is coming into the picture, the worst-case RMS is also a function of the load current. It will be highest at the highest load current and this is also, it is highest for the highest input voltage for both these cases. But it is insensitive to input voltage for constant off time and which we have discussed in lecture 23.

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Switching Frequency – Buck Converter in CCM					
Modulation Technique	Switching frequency (f_{sw})	Worst case scenario			
Pulse width modulation	$f_{\rm sw} = f_{\rm ext}$	Insensitive to system and operating conditions			
Constant on-time modulation	$f_{\rm sw} = \frac{1}{T_{\rm on}} \times \left(\frac{V_{\rm o}}{V_{\rm in}} \right)$	Highest switching frequency at lowest input voltage			
Constant off- time modulation	$f_{\rm sw} = \frac{1}{T_{\rm off}} \times \left(1 - \frac{V_o}{V_{\rm in}}\right)$	Highest switching frequency at highest input voltage			

Now, if you take the switching frequency for variable frequency, the fixed frequency that is fixed for the variable frequency you know has been we have discussed in lecture 23 in our earlier course; that means, the switching frequency will be maximum for the highest input at the lowest input voltage.

For a constant off time, the switching frequency is highest at the highest input voltage. So, you have to be very careful about the selection of this constant on-off time and that is why most of the products, sometimes use adaptive on-off time so, that the large variation in the switching frequencies may not be acceptable.

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So, if we talk about discontinuous conduction mode, we know about the waveform, and if we take the steady state because, in DCM, we generally do not operate in pulse width modulation when the load current decreases because you have a higher switching loss, maybe the ripple will be slightly reduced as the load current decreases, but if it is within the acceptable limits, no problem. So, we do not need this feature at all because we have to only maintain the output voltage ripple within a specified limit.

But if you take constant on time, the output voltage ripple will be more or less insensitive to load; but the switching frequency linearly reduces with the load current, if the input voltage is constant. Then, if the input voltage changes, then we have to use a current base constant on-time control, and that thing we discussed in lecture 24 in our earlier course.

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So, if you take a boost converter, the only difference here will be the ripple inductor current. Again, this will be a function of the state as well as the input voltage. So, the inductor current ripple will be maximum when the input voltage is also that means, it is in terms of input voltage. So, it is it cannot be straight I have calculated. If you use a constant on time, that is the maximum for V IN max.

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But what will happen for pulse width modulation? And this is discussed in lecture 7. For pulse width modulation, if we consider you know this is for constant in the generic term of on time and off time under PWM and if it on time is nothing but D into T and T off is 1 minus D into T. So, if you write this expression in for PWM, it can be found, it is it can be shown that it is D into 1 minus D. So, the inductor current ripple is maximum. If it is used for an output regulator, the voltage is fixed. Then, it is maximum at 50 percent duty ratio and this is what I discussed in lecture 7 in our earlier course.

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Ripple Output Voltage – Boost Converter			
$\Delta v_o \times C = I_o T_{on}$ $\Delta v_o = \frac{I_o}{C} \times T_{on}$ $\underline{\text{Under PWM}} \qquad T_{on} = DT_{sw}$ $\therefore \Delta v_o = \frac{I_o}{Cf_{sw}} \times D^{\checkmark}$	i _c <i>T</i>		
Worst-case voltage ripple at lowest input voltage and highest load co	• Duty ratio is maximum		
[For details, refer to Lecture~7, NPTEL "Cont	trol and Tuning Methods" course (<u>link</u>)]		

So, the ripple output voltage is a function of load current and it can be written for a for under PWM that ripple voltage is maximum, when the D is maximum as well as the load current is maximum. So, that means, the worst-case voltage ripple will be the lowest input voltage and the highest load current and we have to be very careful about the selection of the capacitor because we need to meet certain ripple constants for the entire range of load current and input voltage condition.

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And this issue we discussed in lecture 7. So, the worst-case current ripple for the boost converter under continuous conduction mode, if you use a pulse width modulation, it is the worst at half of the input voltage. That means, when the duty ratio is half; sorry, so that means, the input voltage is just double the output half the output voltage or basically output voltage is 2 times the input voltage.

And for constant on time, it is maximum when the input voltage is maximum and for constant off time, it is the maximum at the lowest input voltage and this is discussed in lecture 7. I think this would be lecture 23 in our earlier course.

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Then, the switching frequency of the boost converter is also in fixed frequency, it is fixed; for variable frequency, it depends on the high switching frequency will happen at the lowest input voltage for this case and will happen at the highest input voltage for constant off time and this we have discussed in lecture 23.

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Now, in this course, we will also have LLC converter full bridge. So, if we take a full bridge LLC converter, first of all, why it is used? So, it offers high efficiency and high power density because we are using a resonant circuit. So, that means, we can operate at a much higher switching frequency so, that the magnetic size can be reduced.

So, you can achieve high power density; the magnetic integration means this L m can be part of the transformer ok. And then, it offers low EMI because of the resonating operation it is not like unlike like a hard switching converter. So, yeah, here you can achieve low EMI because of the resonating behavior and we can operate at a higher switching frequency.



Now, in the case of a resonant converter this LLC converter, depending upon the power level your operating frequency changes. So, we know that the resonating frequency, depends on the resonating tank; but our primary objective, is can we achieve the switching frequency the same as the fundamental component of the switching frequency; can we achieve the same as the resonant frequency?

So, if the power level decreases, then our switching frequency will decrease with the power level and it will be below the resonating frequency this is the waveform and during the condition, when the resonant current; that means, the tank current is equal to the magnetizing current, then there will be no current in the primary path. So, this diode will not conduct. As a result, it will be disconnected and it will behave like an RC network on the output side, particularly during this duration.

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When you talk about a higher load condition, the switching frequency increases so, it will go above the resonating frequency and the waveform shape look like this. So, for both the below resonant and the above resonant, the waveform is not sinusoid; that means, it is a distorted waveform and if we extract the primary component of the sinusoid, it will also have harmonic content.

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But if we can match the switching frequency equal to the resonant frequency, then the resonant tank waveform will look almost like a pure sine wave, and there we can in fact,

reduce the harmonic content and you can achieve very high efficiency there. But this is somewhat difficult to achieve to maintain the resonant switching frequency and the in the resonant frequency and the switching frequency, it is difficult to equalize and that may be possible using an additional degree of freedom.

Sometimes this voltage is because generally the LLC converter is used a fan or on-board charger or off-board charger, where you have an input side power factor character circuit, where the ceiling voltage is the output of the PFC, and if you can slowly adjust this voltage so that you can achieve resonant frequency for a somewhat wider range of power level that may be possible.

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Now, in this course, we are also going to talk about power factor character. But before you go to the bidirectional totem-pole PFC, the general you know the full bridge; that means, diode bridge rectifier followed by the regular power factor boost power factor character that we know and this is like a this is a boost converter circuit and this boost converter, the objective is that the inductor current of the boost converter is forced to follow the rectified current of you know the rectifier circuit.

So, the input voltage, the AC input voltage, and the line current; which means, the input current, should be in phase so, that we can ensure a unity power factor. So, that is why the control objective for this PFC is to make the average inductor current follow the rectified

inductor current profile; that means, sorry the rectified output voltage profile; that means, is a scaled-down version.

That means, if you have a rectified voltage like this, rectified voltage like this, then if we scale according to the power level, if this is your current profile the rectified, the inductor current has to maintain this kind of average. So, the average inductor current should maintain.

The ripple content of this inductor current will be absorbed by this high-frequency capacitor; but then, the average current will be the line current. So, if you can force the rectified current to follow this path, then you can ensure that the input current and the input voltage will be in phase and you can achieve a unity power factor.

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So, in the typical mode of operation, you can operate this boost converter either in a continuous conduction mode, where the inductor current is always like above the zero level and you are tracking that current profile to achieve a unity power factor. You can also operate in the critical conduction mode, where it just touches the zero and then, increases, and then, you can have to make sure that the average inductor current follows these.

So, in this method, you can see it is a variable frequency operation. So, this is a variable switching frequency operation; frequency operation. So, we have to make sure that the core of the inductor and the magnetic core should support a variation of the inductor switching frequency as well as the ripple of the inductor current. So, we have to ensure that it should

not saturate the inductor. The other possibility when the power level decreases in the PFC, then the slow inductor current goes into the discontinuous conduction mode and in this mode, we can improve the efficiency.

But the challenge is here how to make sure the average inductor can still follow the current difference so that you can ensure unity power factor and also the shape of the waveform should not be distorted; particularly, it is more challenging in DCM that while we maintain the unity power factor, we also have to maintain that harmonic distortion is reduced. So, that is another objective.

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Now, if we go for the totem pole, we have we can replace this diode bridge because there will be a drop across the diode. So, that will be lossy. But now with the help of a wide band gap device, you can replace one of the hub bridge diodes with the MOSFET and this MOSFET boarded as it behaves like a diode in one of the hub bridges and this switch will operate in the line frequency, low frequency; whereas this FET is a wide band gap device, particularly it can be a GaN device or silicon carbide.

So, in this course, we are going to show GaN-based totem-pole PFC, where these devices will be operated at a much higher switching frequency. It is like a boost operation, where it can be hundreds of kilohertz; whereas this switch will operate at low frequency, it is like a line frequency like a 50 hertz or 60 hertz depending upon whether it is in you know India or you know the other country, where use 60 hertz. So, that means, we generally use high-frequency

GaN devices for these switches, this leg, and the other leg operator in low frequency where we can use simply silicon devices.

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So, now in this course, we will be talking about interleaved totem-pole PFC because if the power level of this converter increases, then one inductor cannot handle so much current and for better thermal distribution, you can split that into two in inductors like a multi-phase, it is called interleaved, where you need such two legs of GaN devices each dedicated for each inductor and you also can get an additional benefit because if you can make suppose you know one inductor is following like this for one phase.

But if you can ensure the other phase operate like a phase-shifting operation; that means, it is turning on like this. It is operating like this. So, the net current seen by this can be reduced and you can also reduce as a result, the filter capacitor requirement; that means, the output voltage ripple can also be reduced using the interleaving operation; the phase shifting operation.

So, it has double benefit; you can do phase shifting, you can reduce the size of the capacitor, and also, you can reduce the power loss or you can distribute the current among multiple phases so that you can have a better thermal distribution and so that you can have a nice you know heat sink; that means, thermal arrangement. So, this interleaved totem pole PFC one case study will be demonstrated using GaN devices and there will be using C2000 series

microcontroller and that will be demonstrated by an expert from (Refer Time: 21:06) students.

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So, in summary, we have discussed some power stage design aspects of buck and boost converters. We have talked about a buck and boost converter operation, and their steady state operation under CCM and DCM and we have discussed some aspects of the ripple under various modulation techniques we have also discussed the basic operation of full bridge LLC converter for varying frequency, for when the load power level varies and we have also discussed conventional boost PFC as well as the totem-pole PFC for AC DC power conversion.

And in this subsequent lecture, when we will be talking about the hardware demonstration, we will talk about a little bit of detail about this converter, and particularly for the buck and boost converter, we will be talking about you know their schematic as well as some layout aspect. That is it for today.

Thank you very much.