Control and Tuning Methods in Switched Mode Power Converters
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Module - 02
Modulation Techniques in SMPCs
Lecture - 08
Fixed Frequency Modulation Techniques

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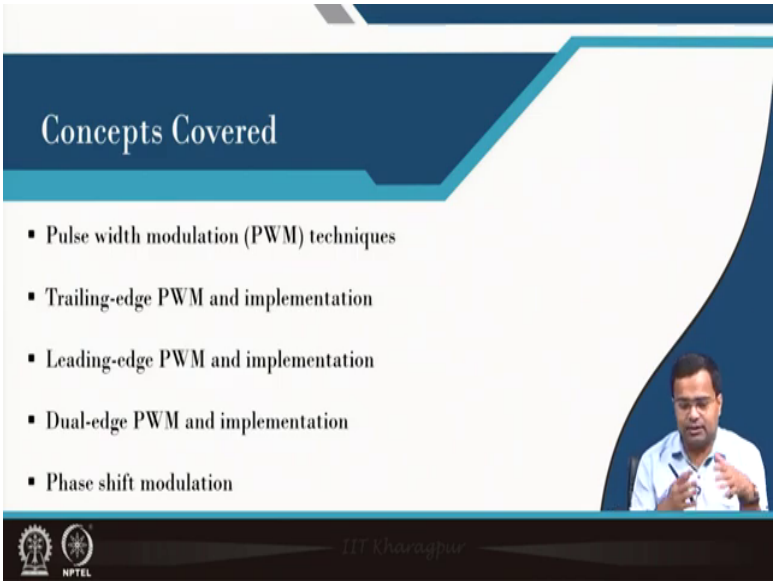

Today is the 8th lecture and today we are going to discuss Fixed Frequency Modulation Techniques. Under pulse width modulation, we will talk about trailing edge PWM, leading edge PWM, dual edge PWM, then phase shift modulation.

There are many other types of modulation techniques, but we will just try to give a glimpse; because you know as we move forward, we will use many of this technique a modulation technique as a part of the closed loop control.

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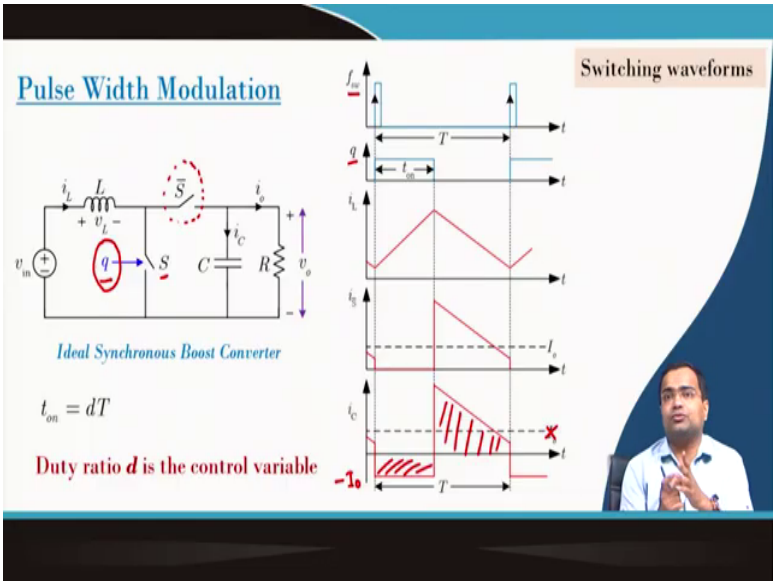

So, in pulse width modulation technique, as the name implies that, if we take an ideal synchronous boost converter and if we draw the waveform of this boost converter, where this f s w is the clock, external clock with fixed switching frequency. This clock is coming from externally, which can be generated inside the controller, and this clock can sometime come from externally, so that we can sync this clock with the other converter also, ok.

So, this frequency the clock is switching frequency clock, but we can program this frequency according to our requirement, provided that our, it should satisfy the design constraint of the converter. Because when you design a converter, we need to know what is the switching frequency. We need to set some switching frequency, accordingly we design inductor and capacitor.

So, in general, we discuss that switch q, which is the control switch, for here the control switch is S and the q is a gate signal. This is the gate signal of the control switch S and this low side MOSFET is the controllable switch. When this switch is on and this is indicated by the gate signal. The duration of the on time is t on and the total time is capital T, which is fixed.

When the switch is on, the inductor current will rise linearly; because we are assuming the output voltage is more or less constant. When the switch S is on, that L d i d t will be v in by

L, so it will rise linearly. When the switch is off, the inductor voltage across the inductor will be v in minus v 0; since it is a boost converter, where we want to achieve higher output voltage.

So, v 0 is greater than v in, as a result this slope is negative and it, so because the voltage across the inductor is negative. If we take the current through the switch S bar, which is the diode current in case of a conventional boost converter, this is replaced with a diode; but in synchronous boost converter, we can use a switch.

So, this current is discontinuous; because when the switch is on, this S bar is off, so current through S bar is 0. When the switch is on, then current through S bar becomes the inductor current and so on. Similarly, the current through the capacitor is also discontinuous, and this current is minus I 0 when the switch is on; the minus I 0 that is the base current, that means when the switch is on, the capacitor current is a negative load current.

So, this is not the one, because the average capacitor current should be 0. So, I think there is a typo here and this capacitor current when the switch is on, the charge across the capacitor is negative and when the switch is off, this charge is positive. So, in steady state, we need to achieve this charge balance, so that the voltage will get fixed at certain volt, like a is a fixed value, ok.

So, in this pulse width modulation, the control variable is the on-time where, since the time period is constant, where varying on time; that means we are effectively varying the duty ratio d. So, duty ratio is the control variable in case of pulse width modulation.

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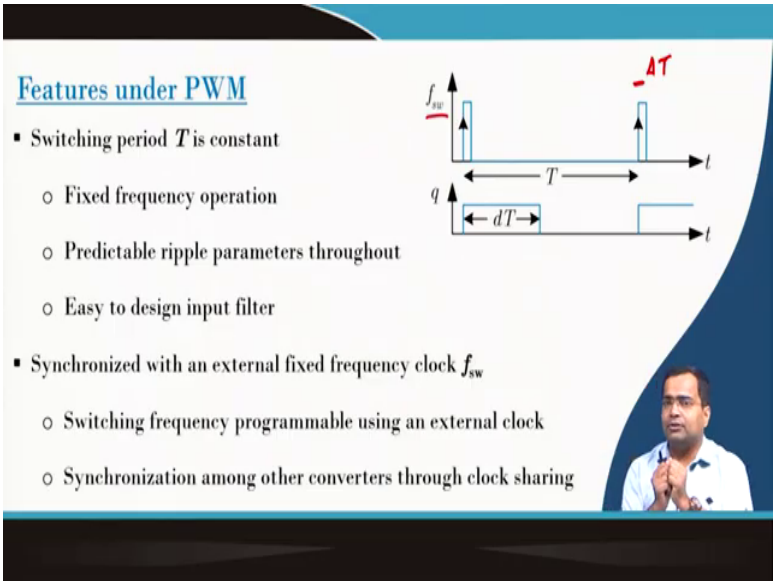

What are the feature that are available in pulse width modulation? Why the pulse width; because in a majority of the commercial products, actually commercial product apply this pulse width modulation technique. And what are the advantages? Some of the advantage is that the switching period is constant. If the switching period is constant, then the switching frequency is constant.

So, for the power converter, we can compute the harmonic distortion; that means what are the harmonic content corresponding to the switching frequency. If the switching frequency is fixed, the harmonic frequency will be fixed; that means second harmonic, third harmony they will be located at a fixed value.

And then we can design the input filter in order to attenuate the harmonic power content; because we want to achieve maximum power at the DC component, because this is a DC- DC converter. So, the fixed frequency it leads to a fixed frequency operation and the fixed frequency operation has an advantage.

Because you know if there is any jitter in the duty ratio, the time period is at least constant; so but there can be some clock jitter in the f s w also, that we are not considering. Sometimes, these clock jitters are intentionally introduced. It is known as randomized pulse width

modulation, which is used to spread the spectral component. Because we discuss you know we also want to meet EMI compliance.

So, one way to do that we can spread the spectrum by adding some you know variation in the switching pre period. If T is the time period, we can take a delta T, where delta T can be a random variable which can be positive or negative within a range with mean value 0 and it should satisfy certain distribution property.

And if we apply such a small jitter on the clock, then we can actually spread the spectrum, ok. So, fixed frequency operation if we do not consider the spread spectrum, it is a fixed frequency operation. The ripple parameters are predictable, because we have shown last slide that the inductor current ripple is predictable throughout. If we can ensure that under closed loop control, the stable periodic behavior is achieved.

If the stable periodic behavior is lost; that means it may lead to sub harmonic oscillation, then the spectral composition can adversely vary. So, first we ensure that the closed loop operation is stable; we can guarantee periodic behavior and under fixed frequency operation, we can predict the ripple parameter.

So, if you can predict the ripple parameter. If you fix the switching frequency, it will be easy to design an input filter, ok. Then, as I said, the f s w if we generate using an external clock or if we take directly from an external clock; because you know whenever we connect, let us say if we talk about DC micro grid application, where multiple converters are connected.

Sometimes we can sync them, synchronize them using an external clock; we can use a common clock to synchronize many converters. In such cases, the switching frequency can be directly the external clock, the synchronization clock, or it can be derived from the external clock. So, that we want some kind of synchronization between multiple converter. So, that is possible.

Also, switching frequency is programmable. We want to vary a little bit. This is particularly important when we want to do it intentionally. Suppose if we see that load has going, down load current is going down; we can decrease the switching frequency to save losses, the switching losses. So, these are also possible.

And sometime this frequency variation can be achieved inherently by using some kind of pulse skipping modulation and other techniques. So, by using this common clock or synchronization clock, we can synchronize among multiple converter, while considering a DC grid architecture and this DC grid architecture is common in many applications, like even we have mobile phone.

We have a common DC bus like a battery voltage and where multiple POLs are connected. So, this is a low voltage DC grid we can think of, where the converter can be synchronized using a common clock.

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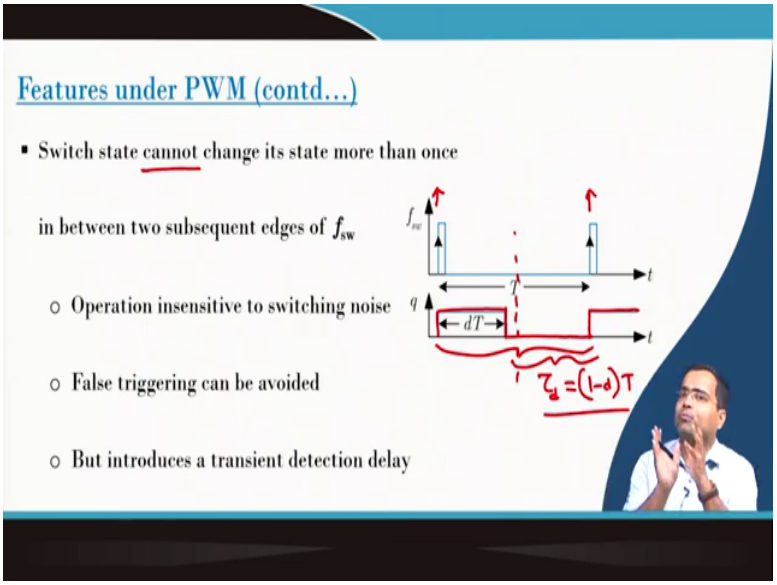

What are the other feature? In PWM operation, we want because from looking at this waveform, if you see the waveform, we do not want once the q is turned off, that means it is going on and off, we do not; we want the switch to remain off for the rest of the duration.

That means we do not want false triggering multiple switching; so that means switch state should not change state, instead of cannot, I should say it should not, we should not allow the switch state to change its states more than once in a periodic interval, ok. That means, in between these subsequent edges, this edge and this edge, it should change only once; that means it turns on and turns off. After turns off, it should not turn on before the next clock edge.

And if we can make sure this will not change state, will not change states; then we can make this operation insensitive to switching noise. I will show you in the subsequent slide. We can avoid false triggering that means you know if you have multiple chattering kind of behavior that we do not want. And, we are we are trying to turn it off. Once it turns off, we are not turning it on throughout the rest of the interval. For this, we have to pay a penalty for that.

What is the penalty? If any transient comes, that means after the switch turns off; if the state of transient comes, that means we need to increase the current, but it cannot, it will not respond, because the switch will not turn on till the next clock arrives. So, this will also introduce some delay and that delay can be as large as this tau d delay, this can be as large as 1 minus d into T.

This is this kind of technique is called trailing edge modulation, where the switch turns on at the rising at the clock and switch turns off when certain logical operation is made, logical you know condition is made.

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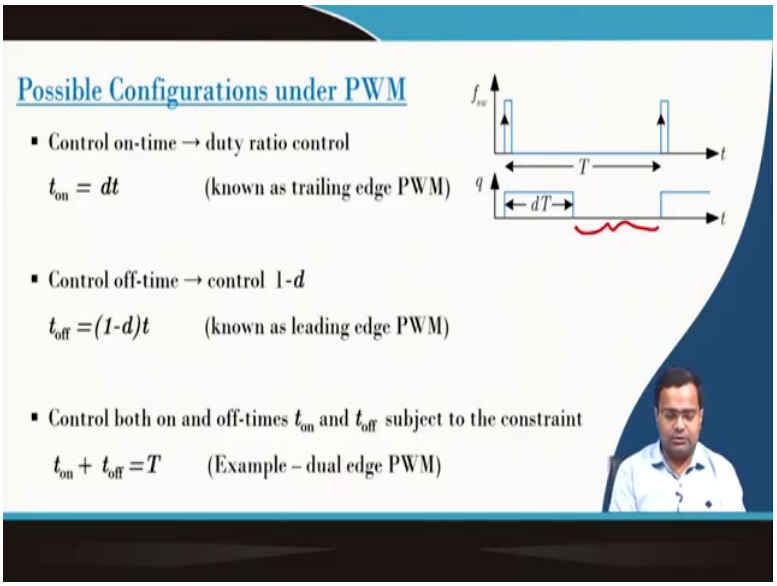

So, possible configuration under pulse width modulation control on time, which is called duty ratio control, and that we known as trailing edge modulation, where we directly control the on time. It is possible also possible, we can directly control the off time; this is also possible to control the off time, but total time period is constant.

So, in this case it is called leading edge modulation, where we want to control the off time directly and the on time will be the remaining duration t minus off time, it is known as leading edge PWM. And we can also control both on and off time; but subject to the constant, the total time period is constant. Such techniques is called dual edge modulation, the total time period is constant.

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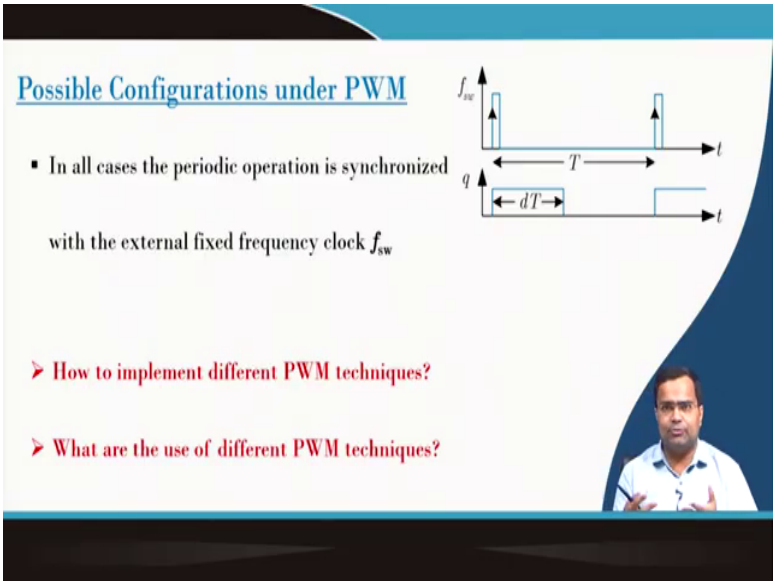

So, possible configuration, in all cases our periodic operation, is synchronized with an external switching frequency clock with a time period capital T which is fixed. Now, how to implement different PWM techniques? First, second, what are the use of different PWM technique; in which application should we use you know leading edge modulation, trailing edge modulation, leading edge modulation and so on, ok?

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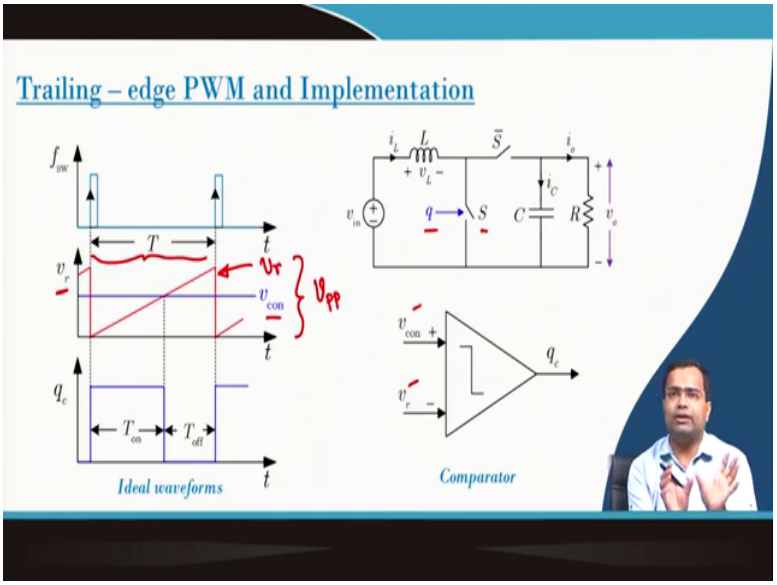

Trailing edge modulation, if I talk if we take a buck-boost converter, where we need to generate the gate signal for the controllable switch S and this we want to generate using a trailing edge PWM technique.

First of all in order to generate this, because it is a, we have to generate a discrete signal; that means on and off and on time we will have a certain duration. Then we see the discontinuous signal, which only can take the value between 1 and 0 and it will stay for some time in its individual states. How can you generate that?

So, if we compare two voltages, one is control voltage, which for the time being assumed it is a constant voltage and v r which are ramp sawtooth voltage. So, it is shown as a red color. So, this voltage. So, this sawtooth voltage, this is my sawtooth voltage, which is my v r; this sawtooth voltage has a fixed slope, and it is going up and once it reaches you know when the time period total T is met, then it resets, that means it is set to 0.

This v r will actually have something like an upper voltage or you can say peak-to-peak voltage limit and this peak-to-peak voltage limit if we change it, without changing the slope, then the time period will also change. So, with this sawtooth waveform, if you compare a control voltage, then we can generate q c which is the comparator output.

And this comparator output from here you can show that, as long as the control voltage v con is higher than the ramp signal red colour waveform, then the switch in the comparator output will be high and when it goes below, it will be low. So, by that way we can generate T on and T off. Is it so simple, ok?

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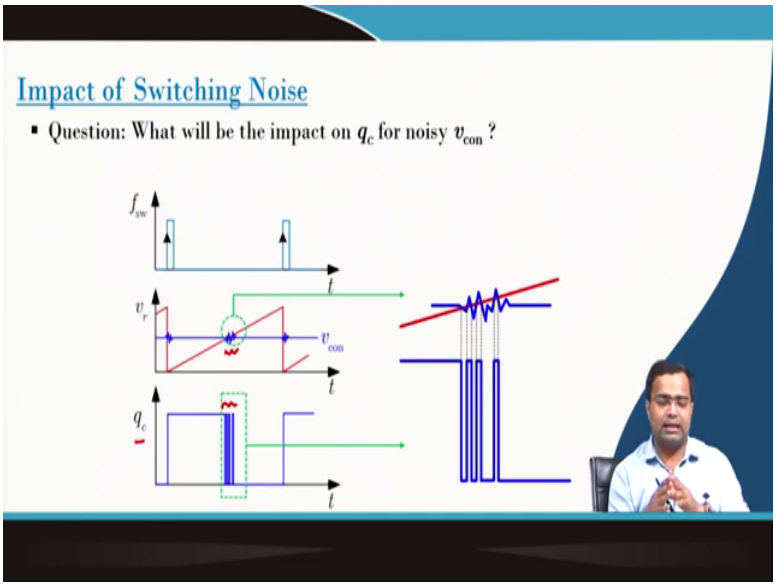

What will happen if suppose we inject some noise into the control voltage? You can ask me how; because this control voltage is not actually a constant voltage. When you do closed loop feedback control, this control voltage is coming as an output of the controller and in the controller's output, there can be switching noise, because it is a switching converter.

So, such switching noise if you inject with this control voltage, then you can say there can be multiple chattering because of this control voltage and this may lead to quick turn on and off of this switch output of the comparator. And such a signal, the comparator output should not be used as the gate signal of the MOSFET. Because MOSFET if you try to turn on and off at a such high-speed faster rate.

First it may not respond, because each MOSFET also has a slew rate limit; because it has a finite rise time and fall time, it cannot be turned on like immediately. Similarly, if you try to heat the limit in the rise and fall time, you know it can get heated and if you continuously do that, even it can damage the MOSFET, ok.

So, such chattering is not recommended and you should not allow to pass it to the gate signal. Then how to avoid chattering? So, this chattering can happen multiple leads to multiple switching; because there can be multiple intersection between the ramp signal and the control voltage.

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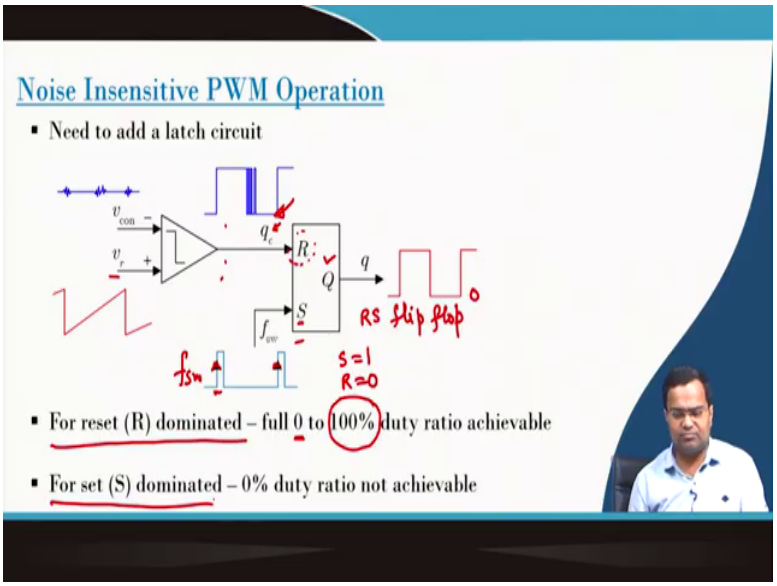

How to avoid? In order to avoid, we need to add a latch circuit; that means we have a ramp signal control voltage. This was the earlier block. Now, we are adding a latch signal, where this is my external switching clock. And how does it work? Whenever the external clock rising is come, the set button is it is set, provided that our reset is 0. So, when set is 1 and reset is 0 the Q will be 1. So, switch turns on.

And we need to keep this as a very low width, but here what I am showing is a latch circuit; but typically we should use flip-flop circuit, that means you should use edge detection circuits rather than level, edge sensitive circuits rather than level sensitive circuits, because level sensitive circuits are not recommended. Because level can actually it can be, it is susceptible to get distorted by the noise.

So, you can use a D flip-flop also rather various possibilities are there. So, here we are just using RS flip-flops. In the RS flip-flop when the first edge; that means where it works on the edge, in the first edge come, this is RS flip-flop, we are using RS flip-flop, not RS latch.

Whenever this edge comes, then the Q is set to 1 and then that edge is gone, then it looks at the edge of the q c.

When the control voltage goes beyond ramp or basically ramp goes above controlled voltage, then q c is high and it detects the first edge and that edge actually turns on the reset switch. If the reset switch is turned on, then q is set to 0. So, this logic 0. And when it is set to logic 0, then you cannot set it to 1; even though there can be multiple, you know high low pulses are coming in the R edge input.

But it will not respond; because even if you set R equal to 1 it is already 0. When you set R equal to 0, since S equal to 0, it will hold the previous value. So, it will remain at 0. Again, when the next switching edge will come, the switch will set. So, this is called trailing edge.

But now there might be a problem, when if a rising edge of the switching clock comes, at the same time if you get another rising edge of the q c; that means both R and S inputs can see rising edge, then what to do? So, we need to avoid such situation. So, we need to make one of them like a master dominant. So, if we make reset dominant; that means if we find that at the edge rising is of the switching clock.

If you find that control voltage is lower than the referent voltage; that means the switch should be turned off, then we should use the reset button to be reset signal to be dominant over set, then it will consider prioritize the edge of the reset rather than set. So, it will turn off and if it is turned off and after sometime the edge of the external clock will also go, then it will remain turn off for the throughout of the cycle.

So, you can achieve 0 percent duty ratio. But for reset dominant, we can achieve 0 percent duty ratio. But 100 percent duty ratio how it is achievable? Then we have to make, 100 percent duty ratio is achievable when you make set dominant because, ok. So, in this case, you can get 0 to 100 percent you know duty ratio.

For if you make set dominant, that means whenever you know; that means you want to make sure that if the rising S of the set signal comes and the rising S of the q c on comes, I want to turn on the switch. And after sometime, when this another edge comes, it will turn on. So, it

will turn on for very short time; that means you may not get, you will not get 0 percent duty ratio.

So, that means reset dominant logic dominated logic is used if you want 0 to 100 percent. But if you want to limit the duty ratio to a minimum value; that means you do not want to go to 0 percent, then you can use set dominant logic, ok.

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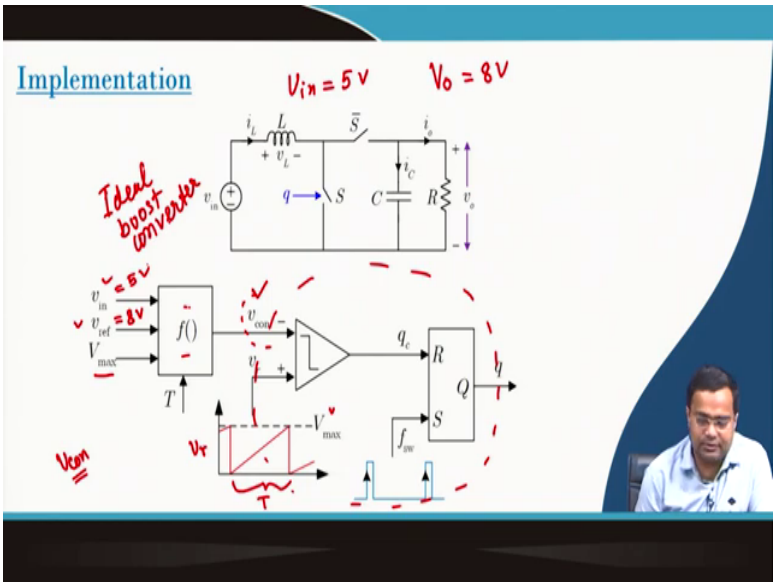

So, implementation you can do this implementation using MATLAB that will be presenting in subsequent lectures, where we want to generate this control voltage and sawtooth voltage. also it is there in the know you can use a MATLAB symboling block..

And this function we already we have already discussed, now we need to generate the control voltage. Initially, we are not doing any feedback control, because that we will discuss later.

Now, our first target, if we take an ideal boost converter; suppose you take an ideal boost converter, ideal boost converter, I will ask a question. If you give me an input voltage; that means if the input voltage is given to you, I want to achieve, let us say my V in is for example, my V in is 5 volt and I want to achieve my V 0 which is let us say 8 volt.

If I want to achieve V in 5 volt and V 0 8 volt; then how what should be my control voltage, if my maximum value of this sawtooth v r is given and time period is also given to you, ok.

So, then what should be my v con voltage? So, this can be derived from the desired voltage that we want to set; here v ref we want to set to 8 volt an output should achieve that, v max is given to you, v in is given like a 5 volt. So, this is given as 5 volt. Then what to do?

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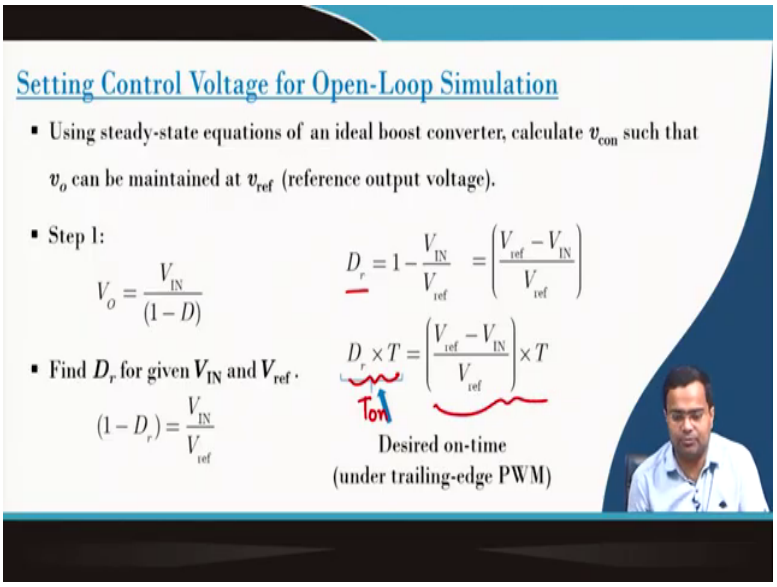

We need to set up you know this case for simulation. Using steady state equation of an ideal boost converter, we can calculate this control voltage such that v 0 can be maintained at v ref. Step 1 we know v 0 for a PWM boost converter is v in by 1 minus D, where D is the duty ratio, steady state duty ratio.

Now, we want to get the desired duty ratio for which our output voltage will be equal to the reference voltage, which you want to achieve. So, I can calculate desired voltage as 1 minus v in by v ref.

But remember, all these we are doing for an ideal boost converter. This will not work for practical boost, because there will be parasitic drop and you will get lost because of in the computation, because that drop is also not fixed, it depends on the current passing through the resistance, I mean it also depends on load condition and different condition.

So, you can get this D r simply by v ref minus v in by v ref. Now, if we multiply this D r into v T; that means on time, this is the on time, this is my T on time, this is nothing but again this quantity, desired on time under trailing edge PWM.

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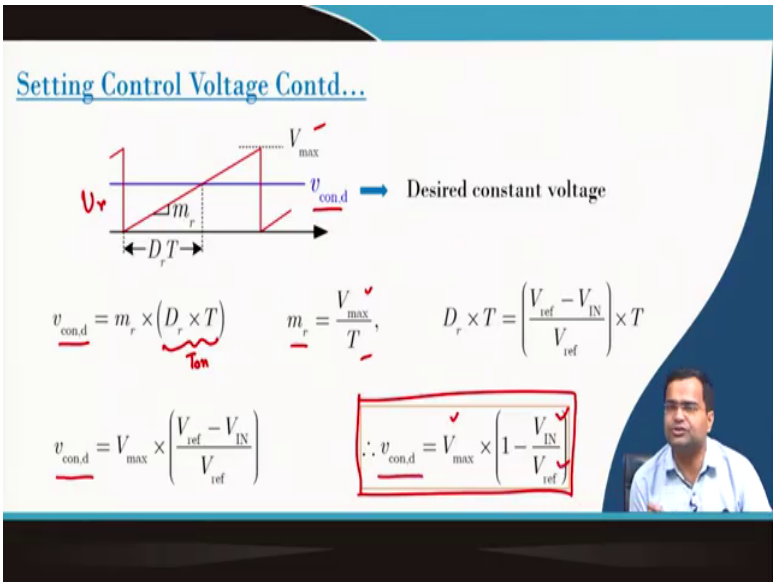

Now, setting the control voltage, we need to now set this control voltage. What is my desired control voltage? V_con_d which is a constant. So, v con d if we know the slope m r, that is a ramp slope, this is my ramp signal; then I can multiply this ramp slope into this on time. This is my desired on time and I can find out. And what is my slope? For a given maximum value, this value and given T, I can find out ramp slope.

And I can get from this equation that D r into T all this I know. So, I can get v converter d is equal to this voltage. So, you can get it from this equation; that means it depends on the maximum voltage of the ramp signal; it depends on the input voltage that we want and the reference voltage. So, for the time being this v converter control d, it is independent of T, because T T get canceled.

If you plug in, if you keep the maximum voltage constant and input and reference voltage constant, then even if you change the time period, that means if you change the slope, I mean if you if you change the slope and you change the time period, this value will remains same, that means a duty ratio same duty ratio can be achieved.

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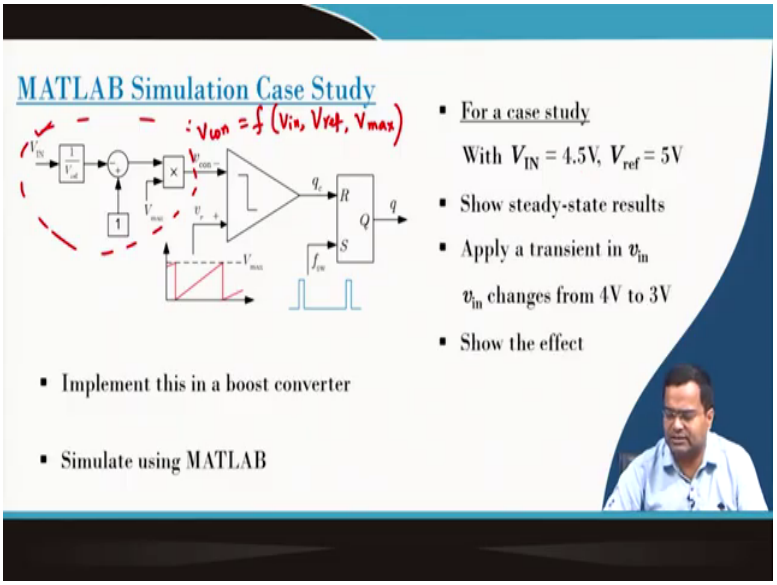

Now, you can do a MATLAB case study, where this is my v in and 1 by v ref whatever equation you saw. So, this is a function block to generate v con, v con is generated as a function of v in, V ref yeah these two are the function. And of course, there is another component, which I actually I should show as well. So, there is another component. What is that? That is my V max.

With this we can plug in this and you can implement in a boost converter; because we have already demonstrated the boost converter case study. So, here you can take a synchronous ideal boost converter, you can simulate using MATLAB and you can take as a case study at 4.5 Volt input 5 Volt output and you can see the steady state effect.

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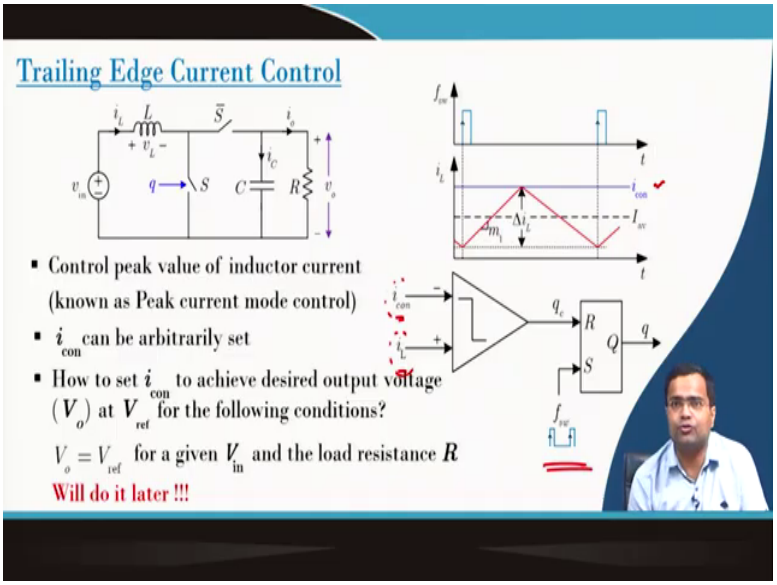

So, under trailing edge modulation, you can simulate I know; now if you do current control technique, instead of a ramp, now you can use the inductor current. You can set a control current here, peak current and then you can compare the control current with the inductor current.

So, here the ramp signal is replaced by inductor current and voltage is replaced by equivalent current and this logic remains same; then you can actually achieve you know the current ah, that means it is directly current control. So, it is a trailing edge pulse width modulation.

And we will discuss detail about the current mode control in later, like a dedicatedly current mode control technique.

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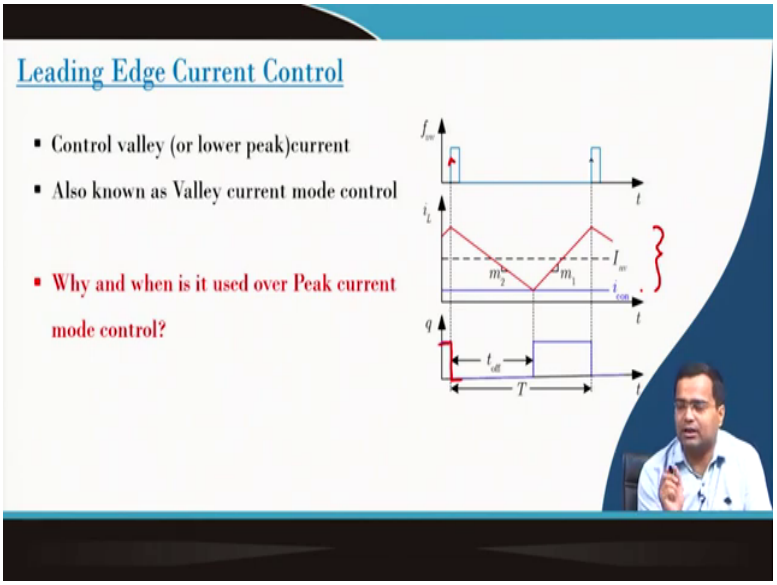

If you do leading edge technique, that means when the clock edge comes, first we will turn off the switch; you see the switch is turned off and inductor current actually starts decreasing. When the inductor current reaches the bottom value; that means control current, then it turns on the switch and here again we can use a latch circuit.

So, I would suggest that you should realize this circuit using a latch and comparator. How does it look like? And though we are going to implement these in the future slide, like a future lecture; but I am just giving you an insight that how to realize this leading edge modulation.

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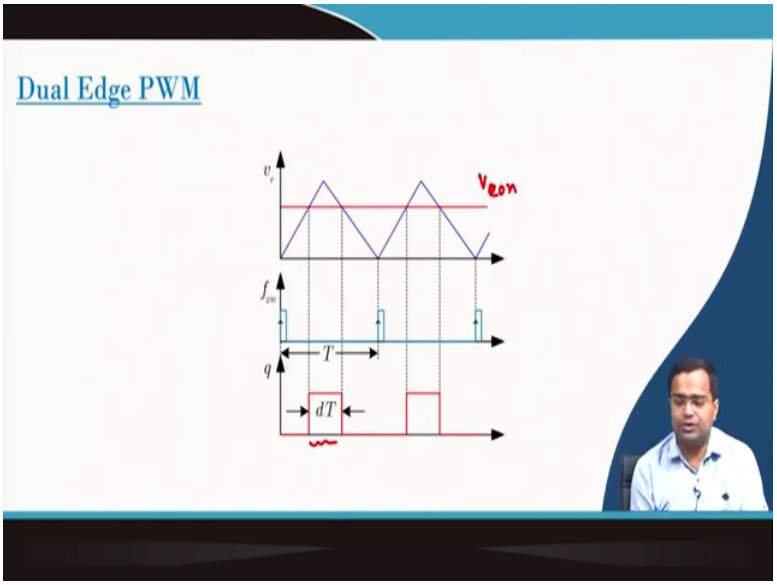

The third one – we left is a dual edge, where you can use a ramp signal like a triangular voltage. This is my control signal, this is my control signal, this is my control and whenever it the control signal is below this sawtooth; then it will generate a duty ratio that a high pulse, otherwise it will generate low pulse. So, using this method, we can generate duty ratio and that is called dual edge modulation.

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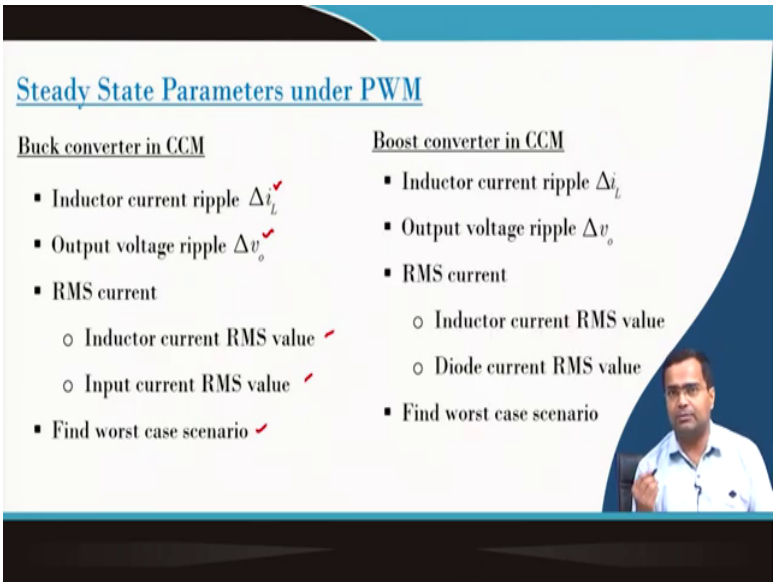

And using this pulse width modulation for a buck converter, we can now if we want to set some inductor ripple current; we can also find what is the output voltage ripple. We can find out RMS current, inductor value, input current and we have already computed this RMS ripple current in the previous lectures. So, you can design the worst-case scenario for pulse width modulation. We can do the same exercise for boost converter; we can find out ripple current, ripple voltage, RMS current and so on.

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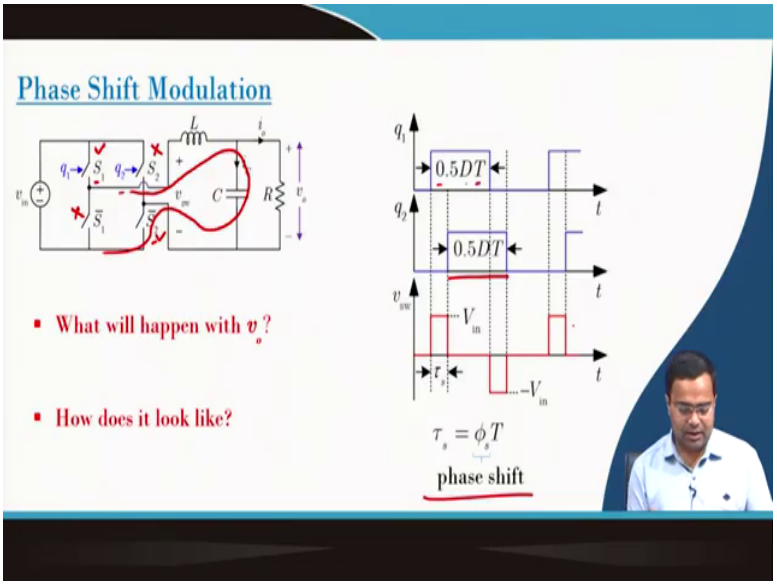

The other one which is left is the phase shift modulation, where it is also fixed frequency modulation, where this S 1 and S 2 bar they are operated using the q 1 pulse or you can you know and S 1 bar and S 2 they are operated using q 2 pulse, ok.

So, this switch and this switch are identically operated and this switch and this switch are identically operated. So, if you use a 50 percent duty ratio clock for this S 1 and S 2 bar and if we use S 1 bar and S 2 50 percent duty ratio like this pulse. Then if you create a phase shift between them, whenever let us say this S 1 and S 2 bar switches are on, that means you know this switch S 1 and S 2 bar are on.

And S 1 in that case if q 2 is off; that means, then what is the input voltage? That means, this path will be created between this, it will go like this and it will go like this. So, you can see

that v s w, the switch node voltage will be input voltage. If both q 1 and q 2 are on, then what will happen, both q 1 and q 2 are on?

I am sorry here I should mention that S1 and S2 bar are not the same switch. S1 is operated by a switch signal q1 and S2 is operated by a q2 signal. S2 and S2 bar will operate complimentary fashion. S1 and S1 bar will operate complementary fashion, I am sorry. So, that means when S 1 is on and S 2 is off; that means S 2 bar is on, we can see v in voltage.

When S 1, S 2 both are on, you will see 0 voltage across the switch node point; if you again take S 1 off S 2 on, it will get negative voltage and when S 1 bar and S 2 bar are on, you will switch 0 voltage. So, with this you can shift the phase, you can we can, you can vary the phase shift and then accordingly we can change the width of the pulses.

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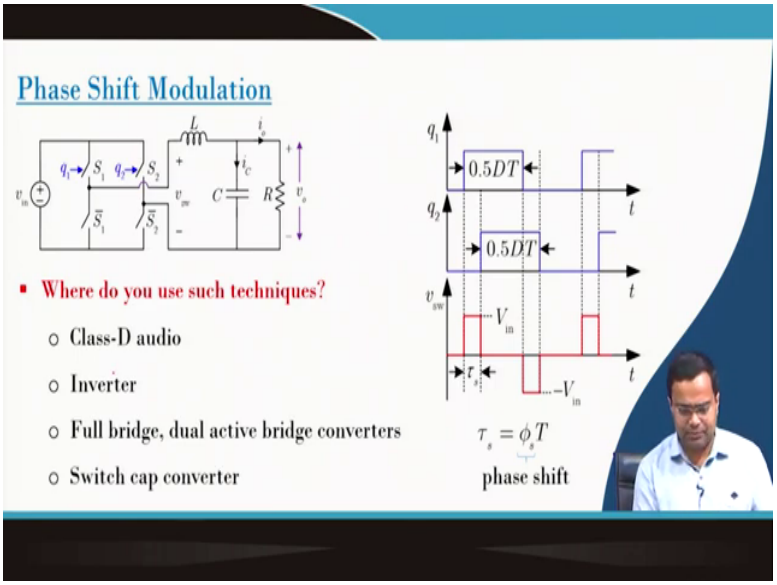

So, this is typically use, where do you use such technique? Like, we use a class D audio amplifier, inverter circuit, full bridge and dual active bridge converter. In fact, if you if you generate a positive phase shift, then the power will flow from left to right; for dual active bridge if you generate a negative phase shift, it will power will flow from right side to left side.

And that is used for bidirectional power conversion. In fact, this phase shift control is also modulation is used also for switch capacitor converter that we discussed at the very beginning

lecture 2. So, such modulation technique, this modulation techniques are also used for such switch mode power converter.

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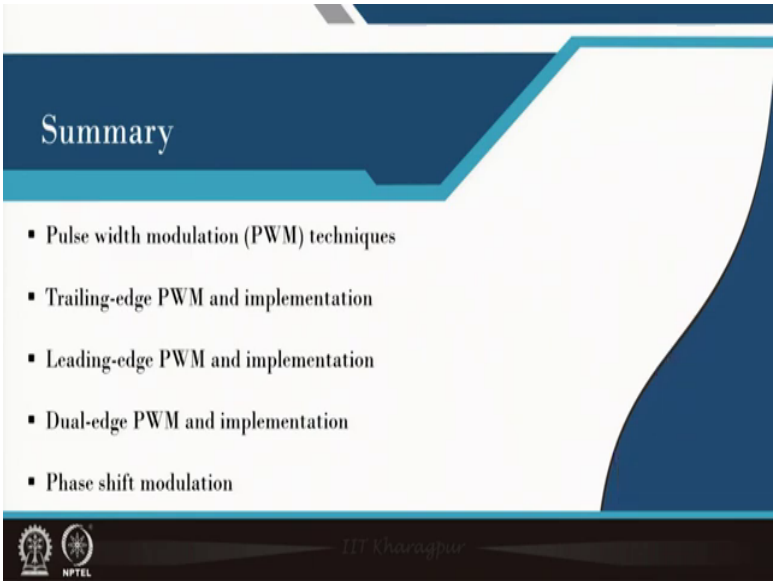

In summary, we discussed pulse width modulation technique, trailing edge PWM. We have implemented that block, leading edge PWM, current based control, dual edge PWM and you also discussed phase shift modulation that is it for today.

Thank you very much.