Control and Tuning Methods in Switched Mode Power Converters

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Module - 12
Performance Comparison and Simulation
Lecture - 58
Overview of Fixed and Variable Frequency Digital Control Architectures

Welcome. This is lecture number 58. In this lecture, we are going to talk about Overview of Fixed and Variable Frequency Digital Control Architecture.

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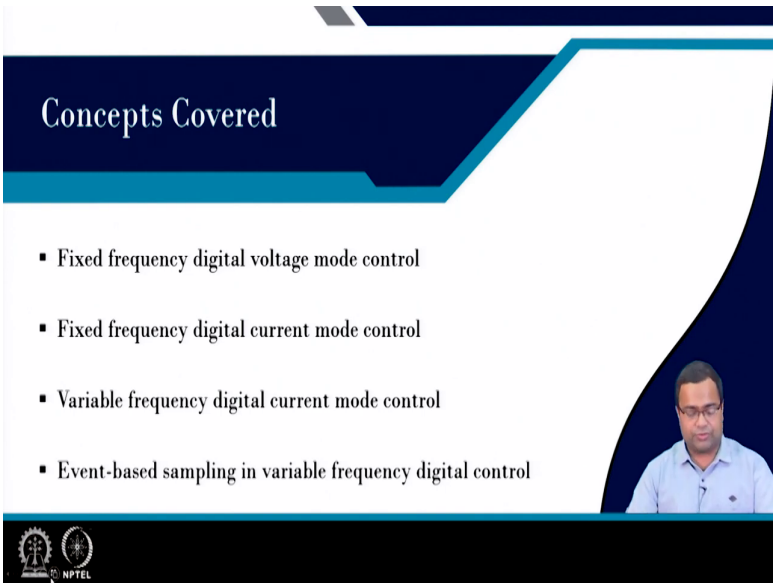

So, in this lecture, in fact, in this course, the digital control it just a just an introductory part, but you know it could be a separate course altogether. But just to give some idea whatever we have learned, how can we; how can we go for digital control? So, that we can you know apply tuning and other stuff.

So, in this lecture, first I will talk about digital voltage mode fixed frequency voltage mode control. Then, I will talk about fixed frequency digital current mode control different techniques, then variable frequency digital current mode control and some event-based sampling technique in variable frequency digital current mode control.

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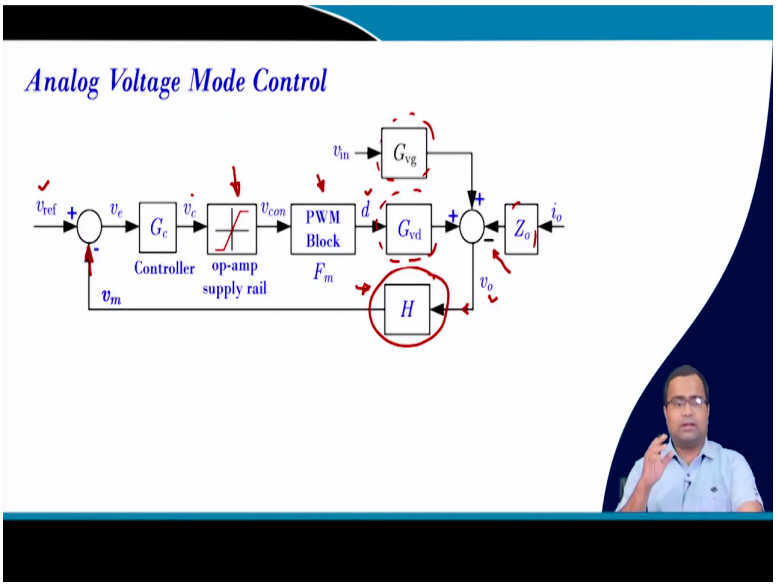

So, in this we will start with analog voltage mode control. We have already discussed in analog voltage mode control. We have a reference voltage and we are trying to design a voltage regulator. This is my actual output voltage, and this is the sensor. Typically, this could be a resistive divider. And then this sense voltage goes to our this is the sense voltage here.

And then error voltage and then this is the output of the controller and if we generally consider operational amplifier op-amp for you know implementing this controller, but op-amp also has a supply rail. So, we will come up. There will be a saturation limit here and then, we have discussed, there is a pulse width modulator block. In fact, we can do for variable frequency control.

Then we will have either constant on time constant off time modulator or it can be hysteresis control. And then, it goes to in fixed frequency we have duty ratio and that duty ratio goes to G vd control to output transfer function that we have already derived. And then this control to output transfer function output; that means, it reflects the change in duty ratio sorry change in output voltage due to the change in duty ratio.

This one is the audio susceptibility, which reflects the change in output voltage due to the change in input voltage. The output impedance reflects the change in output voltage for the change in load current and we need to take into account the sign, because if we are talking about a sinking current, then a negative sign will come into the picture. So, adding all together we are getting this is the output voltage variation.

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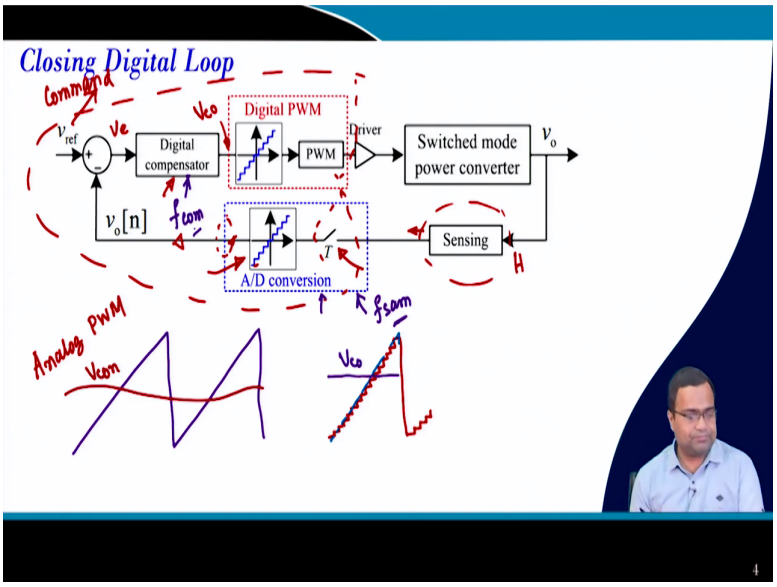

Now, if we want to go for digital control; the first part that you know in our feedback loop we need to incorporate A to D converter. In fact, this sensor circuit, whatever we have consider H transfer function it is still there We still need to consider a resistive divider and unity gain buffer. Some signal conditioning circuit, which should you know kind of try to match the impedance of this signal of you know impedance of the output of this sensing circuit with the input impedance of the A to D converter.

So, there have to be some matching criteria. And then, this signal so that the ADC should not be loaded. Then, A to D converter is used to convert the analog signal into digital signal and this goes by three things. One thing is there is a sampler block like a mathematically we can represent. Then, there should be a quantizer block, because the sampling block will sample the voltage or any signal that we pass at different discrete level right; that means, we have to take the sample voltage at T equal to 0 T equal to some capital T S, then twice TS and so on.

If we talk about uniform, sampling after every fixed interval of time, we will take a sample, but there can be non-uniform sampling also that will go that we are going to discuss when the time period can also vary. Now, once we sample then, this sample signal has to go through like a in the ADC, there is a finite number of bit; that means, whether we are talking about 8-bit ADC, 9-bit ADC, 6-bit ADC and we know about the resolution of the ADC.

So, ADC will discretize in amplitude also, because quantize I will say, because it has a finite resolution. And depending upon the number of bits, I mean we can define what is my

quantization voltage level, but after this quantized voltage. Then, generally there has to be one codifier or coder, which converts what type of code you are getting, because it will be a stream of binary number and that can be represented either in 2 s complement or offset binary or straight binary.

So, depending upon different architecture, but in general ADC we consider 2 s compliment. So, this kind of coding also needs to be considered, because accordingly the output number binary number, which is coming out of the ADC, will be treated. So, whether it is a 2 s or offset, because if you do not take into account this coder, then you may completely miss interpret the data with the real or analog signal.

So, in this particular you know digital control, we are talking about there is a sampler and there is a quantization block. And we will see what is the impact of the sampling and quantization effect in this digitally control converter. Once we get the quantized voltage level that actually compares with the reference signal; that means, you can think of this whole block is like digital block.

So, starting from this process; this whole block is digital. So, this is the number. This is the command. I will say it is a command. It is a reference command, which is a number and your output voltage will be compared and the error voltage which is again the quantized discrete voltage or number that we pass through the compensator and generally, it is a digital controller which can be PI, PID controller there are a variety of compensator that we can consider.

You can talk about type two different types of compensator like you know lag-lead compensator and so on, but the compensator voltage if we talk about; this we call about control voltage. And in analog control, it is typically you know compared to the sawtooth waveform. For example, if we talk about analog; if we talk about analog you know PWM Analog PWM.

So, in Analog PWM, we have a sawtooth waveform like this, like this and then we have like a control voltage like this. So, this is my control voltage in case of analog ok; let us say just to be specific control voltage for analog. What will happen; the same thing for digital. If you want to draw something similar or equivalent, it will be like a staircase waveform. You may think the easiest one is the counter base approach, where there will be a kind of staircase waveform and again it will reset. It will go like this.

So, in the average sense, you can think of this slope is something similar to analog control. Interestingly, we will see that this control voltage what is coming from digital; this will change updates according to the sampling and the computation rate, because it will only update when you get a new sampling data; that means, the sampling data get updated, and that updated data will be added and the control will also be updated.

So, we need to remember that the clock use if you say the clock; that means your computational clock and if we talk about the sampling clock. So, these two should be matched, they should be synchronised. But sometime what happen in some cases, we may sample at a higher rate, but we may compute at a lower rate, because the ADC can be used sometime for you know kind of transient detection circuit where we need to sample at a faster rate to identify when the transient happened or in some cases.

You know we are just looking at the error voltage, whether it goes beyond or not. But in general in most of the cases, the sampling rate of the A/D converter is same as the controller computation, because they will be sink the same rate. So, it is a uniform sampling rate. So, we are not talking about any multi rate sampling here.

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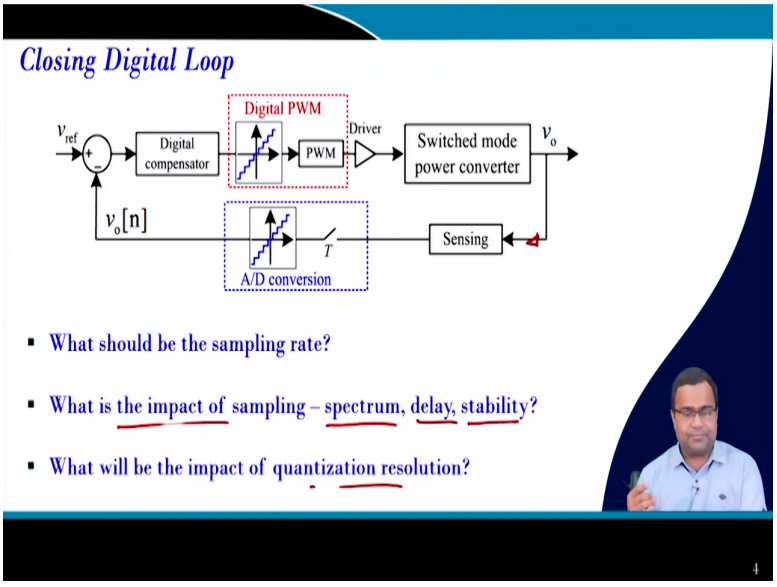

So; that means, now the next question you may ask I mean you know that will come to our mind what should be the sampling rate, I mean what should be our sampling rate? Should it be higher than switching frequency, lower than same what? If it is higher, in what factor it should be higher?

Then, we will also see what is the impact of sampling like in terms of power spectrum, delay, stability; that also we want to see and then what will be the impact of quantization resolution. So, in the next lecture, these two thing like a delay and the quantization effect we will see, but in this lecture we are going to see architecture where we want to see at least the power spectrum, because we need to take a decision what should be my sampling rate ok.

And if we take a different sampling rate, then, if I take the power spectrum of actual analog output voltage and if you take the power spectrum of the discretize or basically digitized voltage, how is it how are they going to be? Whether they are going to be same or they are going to be different.

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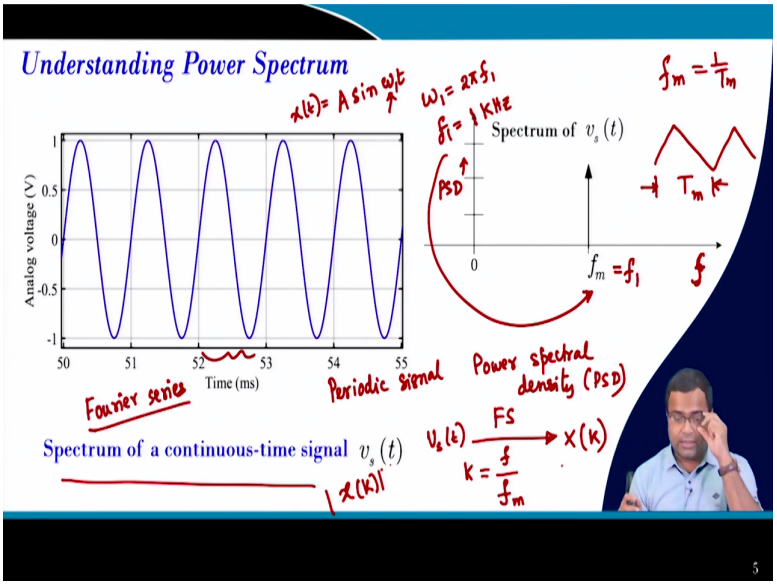

So, we need to first understand the power spectrum. What is the power spectrum? Suppose we take a pure sine wave. If we consider a sinusoid, it can be sine or cosine or a combination; let us say we are talking about a continuous time signal an equal to sorry x t equal to A sin omega t, where you know omega here.

Here, let us say we have taken 1 millisecond; that means, we have chosen here some omega 1 is equal to 2 pi f 1, where f 1 here we have considered 1 kilohertz ok. So, we have to consider 1 kilohertz is my frequency. Now, if we took power spectrum; that means, you know this is the periodic signal right. So, this is the periodic signal periodic signal and if we want to extract the frequency component of a periodic signal, then what we should do we go for Fourier series right Fourier series.

So, I am not going too much mathematics for that, because these are well established, and it is a different course. But I want to say if we apply Fourier series, then we want to get the power spectrum of this continuous signal and it will be simply a single frequency component. And here, I can say f m equal to f 1 because this is my injected frequency and sometime it is called modulating frequency.

So, in the frequency spectrum, what is y axis y axis is the power spectrum power spectral density PSD. It is called power spectral density; in short form we write PSD. How does it look like? So, power spectral density if we write the Fourier; that means, if x in this case it is v s of t if we pass through ok.

So, suppose v s of t if we pass through like a sampler a sampler block. sorry here we are talking about power spectrum. So, we are not talking about any sampling suppose for this signal. If we apply Fourier series, then what will get. We will get something like a X of K. What is X of K? X of K is a Fourier series of the v s of t where K implies. It is basically the modulating you know here the instantaneous frequency; that means, if I take this is my frequency axis.

So, K corresponds to. So, K f divided by your modulating frequency or basically the periodic frequency the time; that means, your it is like it has switching frequency is fixed. So, sorry your periodic frequency is fixed so, periodic frequency right. And here you will get you will get f by f m; that means, 1, because it has only one frequency component that is the fundamental.

Now, if we talk about, let us say other than sine wave. Suppose we talk about a triangular wave like any arbitrary shape, then we will have time period T time period T. This is my frequency modulating period and my f m will be 1 by T m, but in this case if we apply Fourier series, because it is a periodic signal; you will get harmonic content other than that means, K will be 1 2 3 and so on you will get power spectrum.

And since it does not satisfy any symmetric property. We will get even all types of harmonics. And for this x of K, if we take x of K that its power basically, you will find the Fourier coefficient; that means, you know. So, we want to see what is the power content, because we can apply Parseval's theorem and find out what is the power contained here in this signal; that means, in the Fourier domain, then we will find the power spectral density.

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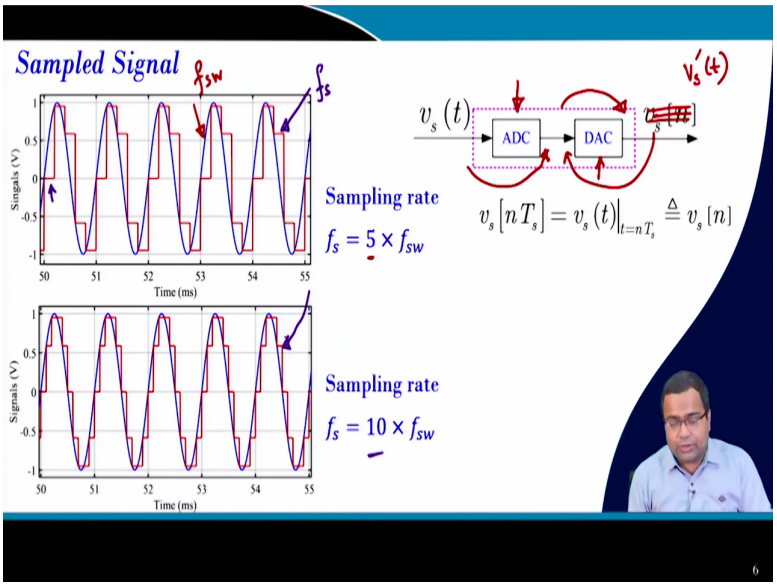

Now, we have talked about a periodic signal. Suppose this periodic signal is pass through an A/D converter, followed by a D/A converter; that means, first we are discretizing the signal; that means, we are converting from analog-to-digital. And then, we are converting from digital-to-analog.

If the sampling rate is very, very high and as we know from our common sense, then the output signal this is like your you can say v s dash t, because this n should be here, because it is a time domain it should be time domain, because it is again analog signal continuous time signal.

So, v s dash t which is the output of the ADC followed by DAC this will be almost equal to v s t; if the sampling time is very very small. It is very small and the quantization resolution is very high; that means, you have a very higher order, you know a number of bit, then they are almost like a same signal will be represented.

But in reality, neither we have very excessively large number of you will get a number of bit, nor you will can find out or you cannot you can apply a very high sampling rate. So, there should be some limit. So, here we are talking about the sampling of this signal 5 times of the periodicity; that means, we can think of the blue signal it has f sw is the time period sorry frequency that is the frequency of the analog signal.

And we have sample the signal, which is shown here by the red one this one is my sample signal after sampling and what is sampling rate here 5 time. So, we will see there will be 0 order hold effect right. So, the sample signal will not look like exactly like a sine wave.

So, there should be distortion in the waveform. And if we take a higher sampling rate, then you will get somewhat close approximation of the actual digital signal right, but here, we have not considered any quantizer. If we apply quantizer, you may even get somewhat more distorted waveform.

But for the time being we are only talking about sampling rate. So, if we increase to 10 times, then we will get closer behaviour of the analog signal, but still, they are not exactly same. So, now, the question is what should be the sampling rate should we go to 100 times should we go to 200 times. So, it is simply impractical, because we are going to apply such sampling in our switching converter, in which the switching converter itself is running at a higher switching frequency.

So, we have little flexibility to increase the sampling rate like we cannot impractically increase it right very high sampling rate we cannot say. A practical signal even if you want to sense a periodic signal; our sensor can even if you there is no you know even if you take negligible variation in the time period, it can so happen the sensor can have some uncertainty. The distortion in the sensor can also add up this kind of variation ok.

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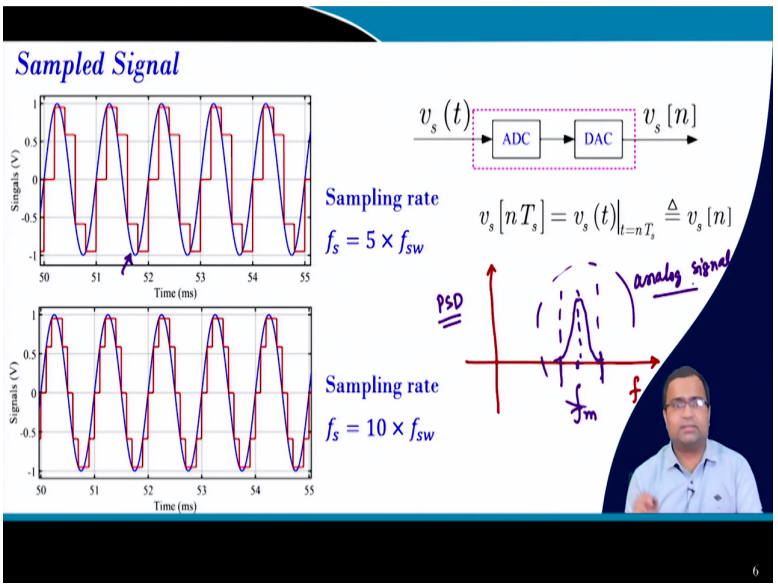

So, as a result, after sensing the signal, we will get something like band limited signal. So, if it is my frequency spectrum and if I take, this is my nominal frequency, my modulating frequency. So, in perfect case you should have got like this only a single frequency component, but in reality, you will get something like this, something like this; that means, this is band limited. So, we will take certain band we are not probably going to take too much of band.

So, it is a band limited signal and we are talking about the power spectral density. Since, we are talking about a real system taking into account all types of uncertainty. So, we will talk about a band limited signal ok so, certain band. Even if we have a very high frequency component in the actual signal, our sensor will have a bandwidth. So, we will get some sort of band limited signal.

And if such band limited signal if we take this sine wave pure sine wave to be a band limited signal. So, we will get the power spectral density of the analog signal looks like this something like this.

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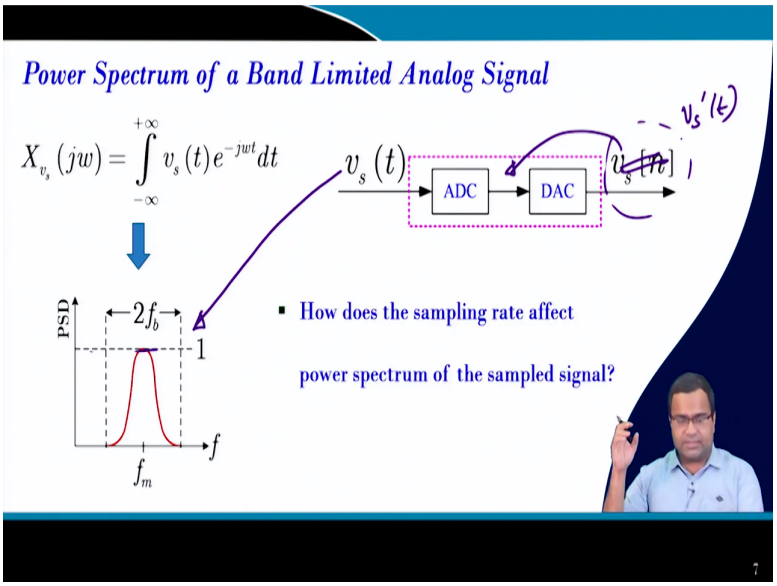

Now so, this is the power spectrum of the band limited signal. I told you about the a switching converter. Switching converter; what we consider generally we have a sensor feedback a sensor and the feedback signal will also have some band ok. So, this band limited signal; if we take the power spectral density, this looks like this. Assuming in normalization, the power spectral density is 1 the peak value is 1 ok. Now, we want to see what will happen

in the power spectral density of the sample, followed by like ADC is followed by DAC; that means, again, it is a continuous signal. It should be v s dash t, because this will come actually here, because it is a discretize. And then, after that, it will again become a continuous time signal. Now, how does the sampling rate effect the power spectrum of the sample signal?

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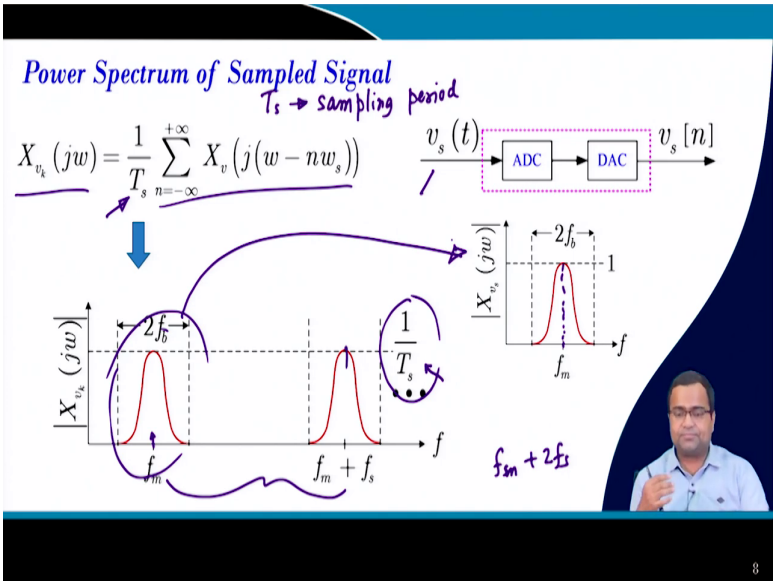

So, this can be proved mathematically if you take the power spectral density of the sample signal. I am talking about v s dash; that means, it is passing through ADC followed by DAC. It can be shown that it is 1 by T s and which is the sampling time period.

So, here T s is the sampling period, it is the sampling period. It can be shown 1 by T s sum of this; that means you will get a train off kind of spectrum right, so that means, in the power spectral density, you will get a sum of multiple thing how does it look like? So, it will look like the band limited signal that we have considered which is in the continuous time signal of the analog signal sorry analog signal that is scaled by 1 by T s, because we took earlier it was 1 that was for the actual band limited signal it was 1.

But is scale by 1 by T s and it will create multiple loop that means, 1 at the frequency of excitation, because this is the modulation frequency that is the periodic frequency of the or the nominal frequency of the analog signal. And then, on top of that, you will get f m plus f s then you will get another f m plus f m plus twice f s f m plus 3 f s and so on. And similarly, left side we will get f a minus f s and so on. So, we will get side loop.

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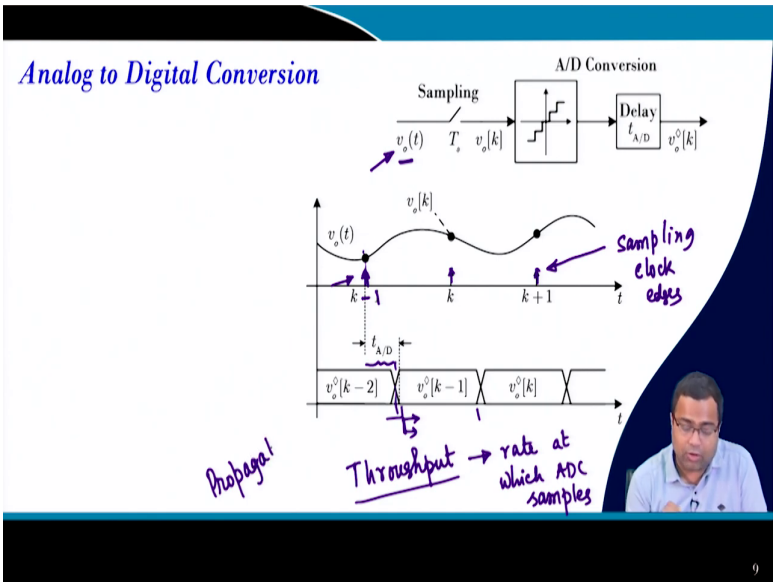

And all this component will have equal amplitude like 1 by T s and depending upon. Now, if we decrease this T s; that means, if the sampling rate is increased, this spectrum; that means the distance between these two spectrum will keep on increasing. So, as if it is another band, actually it will repeat after very very you know long time ok and then it can be shown that at T s tends to 0, this signal will asymptotically look like this signal; that means, as if they will again become like an analog signal.

If T s tends to 0 and this comes, you know this, because this theorem was Nyquist theorem right, the Shannon sampling theorem; from where we can get the spectrum of this sample signal ok. So, now, why we are studying this? Because in our switching converter, we need to decide the sampling rate.

Now, going back to the analog to digital converter. In our DC DC converter, we have output voltage. In fact, this is our sense voltage where we can consider the gain of the sensor, but let us for the simplicity, let us assume it is the output voltage and we need to sense the output voltage.

This is my sampling command. So, these are my sampling command, sampling edges clock. I will say sampling clock edges; that means, whenever these edges come, it you know it gives the instruction to the ADC that you now sampling.

So, this is the moment when the ADC will sample. But the moment your you are instructing the ADC to sample the actual data which will be available; that means, a digital data that will take time, because you have some finite delay of the ADC the conversion time, but we still have not considered the delay due to the other parts of the loop delay. Here, we are only talking about the delay due to the A/D converter.

So; that means, even if we are sending the commend signal here and it is k minus 1, the actual data will be ready after some delay; that means, it is ready here. So, from this point onward, your data will be ready this point onward; that means, we need to take into account this delay. And this delay can vary depending upon what type of ADC you are talking about, what is the sampling rate of the ADC.

And there are various types of ADC; like you know we can have you know successive approximation type ADC, you can have pipeline ADC, you can have flash ADC. The flash ADC may be seem you know have a least delay, but it is generally not preferred, because it requires impractically large number of you know comparator ok.

So, there are like or you can have you know serial ADC parallel ADC. So, there are different type of ADC architecture. I am not going to discuss, but the conversion time can vary from ADC to ADC. And there are a different way of getting the digital signal, but we are concerned about the delay even though ADC can sample, because there are two terms that come into picture ADC; one is called throughput.

This is the rate at which rate at which rate at which ADC samples right; that means, whether you want to sample 50 mega sample per cycle, 10 mega sample per cycle. So, this rate will be decided by the throughput. This is important, but more important for this power converter is the propagation delay propagation delay or sometime in ADC terminology, it is called latency.

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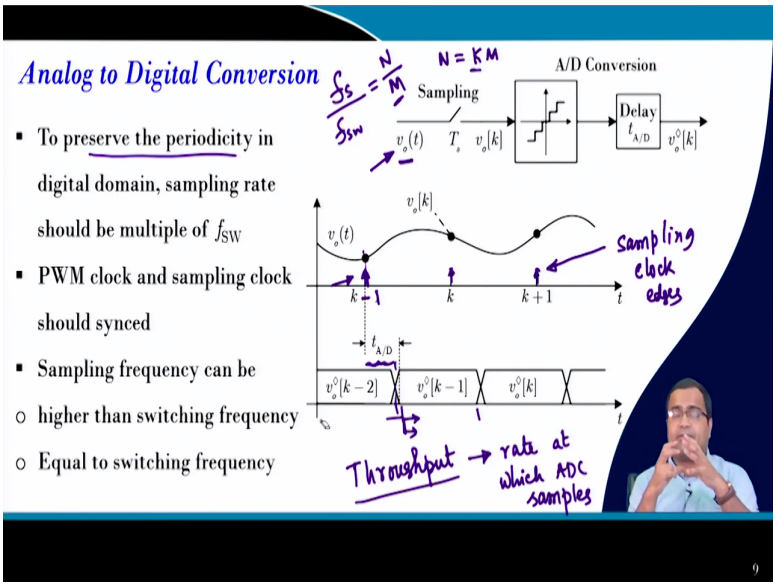

So, we call it as a latency. So, for us this is the one of the most important. This latency will decide what is my delay? So, if we take pipeline ADC. The pipeline ADC is the delay is generally decided by the number of stages pipeline stages. So, if there are 6 numbers of pipeline stages. So, your delay will be 6 times of the sampling clock.

So, if you want to reduce this delay, you have to sample at a very high rate and we have to check whether such sampling can be supported by this thing or not ok. So, the latency is the one which is very important for us which decide the delay.

So, now, one things few things have to keep in mind, in order to preserve periodicity, because we should not abruptly sample even though we sample once per cycle or 10 per cycle, but there should be some uniformity, some synchronism. Because in order to preserve periodicity, generally the sampling rate is to be an integral multiple of switching frequency.

If they are fraction; that means, the sampling rate if you take. Let us say the sampling rate divided by the switching frequency ok. So, let us consider a scenario. If you take something like sampling frequency by switching frequency, it is something like a N by M; that means, this is a ratio of two integer numbers. I it is a rational number which is the ratio of two integer numbers.

Now, we generally take N is K times M; if K is integer is fine, but suppose we take K fraction, then what will happen. This will introduce some non-linear behaviour and which can

lead to you know quasi-periodic behaviour, sometime you know mode locking behaviour. So, unnecessarily, it may generate some sort of non-linear behaviour, which sometime you call like a limit cycle or it can be chaotic behaviour. So, we generally avoid such kind of fractional sampling rate or basically, it should be integer multiple.

And PWM clock and some sampling clock, they are generally synchronized sync. And third; the sampling frequency either can be integral multiple of the switching frequency, it is can be higher or it should be lower, but we should not take generally the lesser number of sampling rate. In fact, that may be possible if the converter is running perfectly under steady state.

Then, in order to save power or avoid computation, you can keep your processor idle and you can just continue with the value which is already stored fixed number. Because ultimately the digital control under steady state, you know it will look like an open loop; that means your error voltage in digitally become 0 and then there will be no update in the digital controller. So, it will look like a constant number ok.

So, in that case, we can even reduce the sampling rate ok. So, there are many architectures or many intellectual properties as well as research papers are available. But, I am not going to discuss generally we are talking about for sake of analysis. It should be equal to this.

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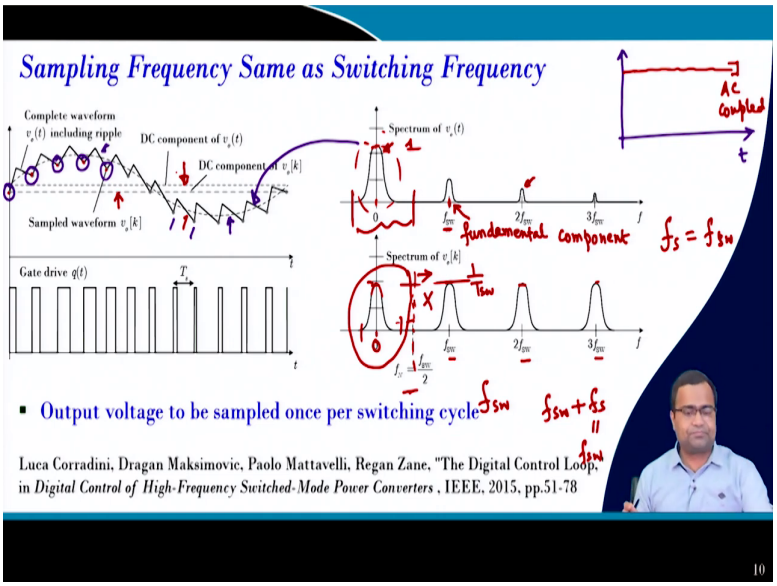

Now, the sampling frequency same as switching frequency is a scenario. Suppose this is my complete waveform if this is my output voltage ripple and you can see the output voltage

ripple looks like somewhat dominated by the ESR ripple, as if it is capturing like a similar nature of the inductor current. So, we have this is my average output voltage and the actual output voltage will also have a ripple.

Now, if you take one sample here, all this sampling point. So, here we are sampling here; as if we are sampling at this every edge. These are the sample waveform. Then, what will happen actual power spectrum of the analog signal; that means, if we take the power spectrum of this analog like means analog voltage, then we know the output voltage in a DC DC converter should be ADC right; that means, ideally or if this is my time domain waveform.

So, our output voltage, if we take in a division like a 1 volt or 2 volt in oscilloscope, we will simply see it is like a flat output voltage. But if you take AC couple; that means, if you take zoom this part AC couple mode if we go to AC couple mode, then you will find these kinds of ripples are there.

And generally, these ripples are of around 2 percent of the steady state value. So, you can imagine that the power contained in the AC couple signals is much less compared to what is there in the DC couple, which primarily dominated by the average voltage or the DC voltage ok.

So, we will get a high peak at 0 component then f s which is our switching frequency; that means, this you can say the fundamental component. This is my fundamental component corresponding to switching frequency component, then we will get harmony. And as we move higher and higher harmonics, the power content will get reduced, because the maximum power will stay in the DC component.

Now, if we take one sample per cycle, then what we can expect we saw. So, we saw that one sample that means your sampling frequency is same as switching frequency. And we know that here, at 0 frequency, it will also have a side lobe, which is here; that means, we will get f sw, then we saw f sw plus sampling frequency. And in this case, sampling frequency is same as switching frequency.

So, we will get 0 f sw, 2 f sw, 3 f sw and all will have equal amplitude, because this is the band limited signal. And we saw that if a periodic signal if we take only this part of component is passed through the sampling block; only this part will be repeated multiple

times and they are they will be scaled right. So, it will be 1 by T sw there will be scale if this quantity is 1 right that we have seen.

But now, since our sampling rate is same as switching frequency for the digital controller, we can always see up to Nyquist sampling rate, which is half of the sampling rate; that means in the digital controller, nothing will come beyond this; only component will come left side of this.

So, as a result you will see only this part will come into the picture. So, there means, but suppose if you take a higher sampling rate. Then it may so happen in the Nyquist sampling rate, you will get additional component. This can cause aliasing effect and you know. So, to avoid this aliasing effect, one sample per cycle is considered.

And you can get more detail in this book and there are multiple papers of that. But the only thing we can miss is that due to this reduction in the spectral peak, you may lose, because you can imagine you are only taking the bottom value of the sample. And if you take the average out, they are somewhat smaller than the actual average voltage. So, as a result, your sample voltage is here and actual average voltage of the DC converter here. So, you will lose some regulation point and that we have to anticipate by suitably give providing an offset to the reference voltage, so that can be taken care.

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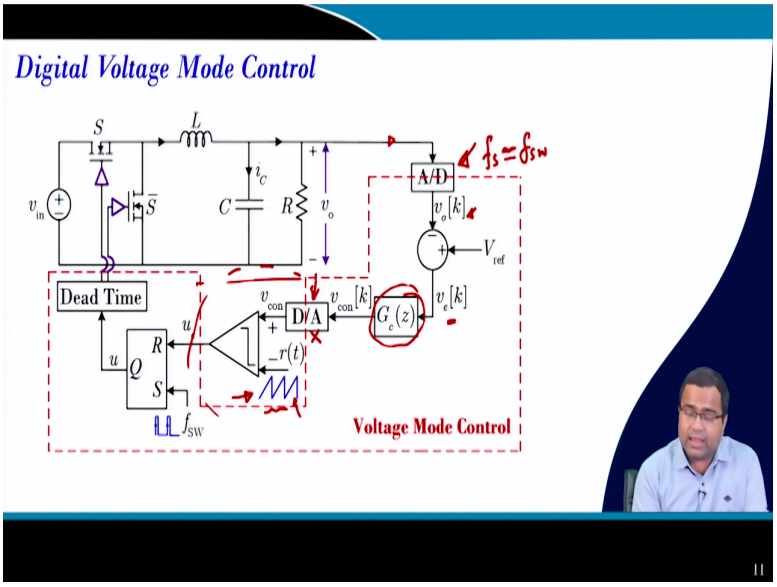

Now, if you go to digital controller. So, we discuss one A to D converter and we discuss this sampling rate to be roughly we are taking same as the switching frequency right. And then, after this sense voltage comes inside, it is the digitized one; that means, it is both sample as well as quantize.

And then, it is compared with the reference voltage and we get an error voltage and then it goes to the compensator. And then, this compensator output if we talk about, you know, sawtooth waveform in analog or we can all we can also consider the whole thing in digital. So, then, in fact, this can be current also; that means, here this provision is kept to show current. But in voltage mode control, this whole thing can be digital and you may not need any DAC, if you generate this sawtooth in the digital waveform.

But in some cases, you know people prefer to use you know this saw-tooth waveform outside, because there are certain restriction due to the sawtooth which will create impose a constant duty ratio, because this will be responsible for the resolution of the duty ratio. So, in order to improve the resolution, sometime you know some designer also consider D to A, but again you have to pay a price for the D to A converter.

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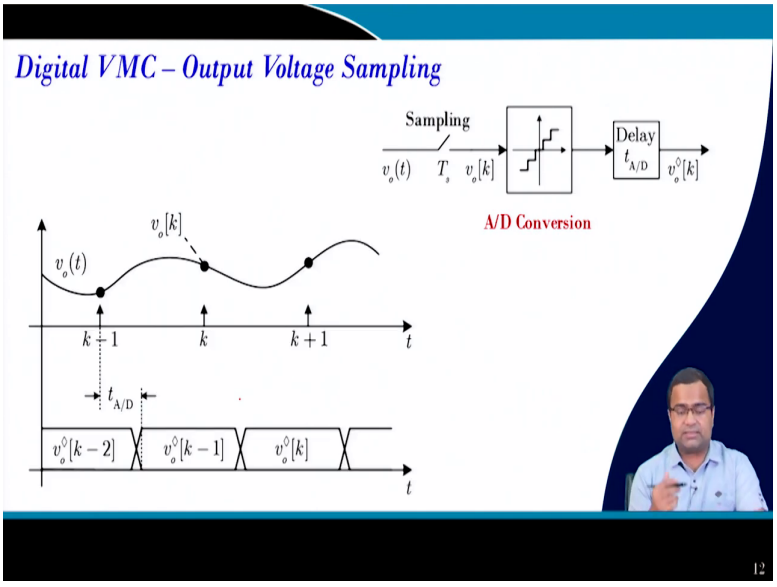

So, in general, most of the digital controller will be discussing; that means we are taking everything in the digital loop. Once it goes into the digital, controller nothing is analog after this. But once we go to current mode control, we will see this D to A converter can be also

used when you when you want to keep the fast-changing current loop in the analog domain. So, now, output voltage sampling we have discussed this aspect.

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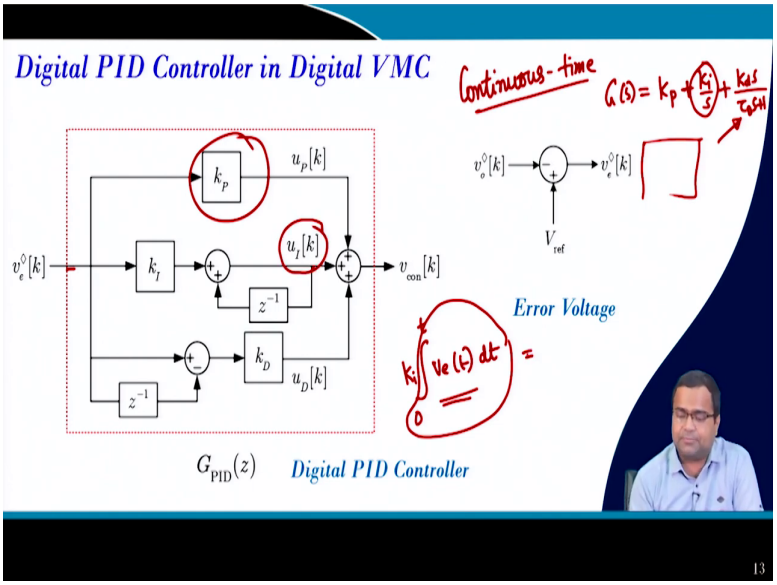

Now, suppose we want to implement a PID controller that we discuss. So, if we want to implement a PID controller, we know in continuous time; in continuous time, we know that a PID controller that means, G of s is generally k P plus k i by s plus k d s by tau d s plus 1 and this is my digital derivative filter. Now, in case of digital, this is like a proportional control. The error voltage is coming, because as if there is an error voltage and after the error voltage, we put a PID controller in case of analog, simply keeping.

Now, in case of integrator; that means, if I take the time domain; that means, it is simply k i is outside integrator error voltage times that integrating over you know you can start from 0 time and you move on right. Assuming that at 0 time there was no initial condition or even if there is initial condition that can be taken care.

So, this quantity in digital control this some block can be realized using something called velocity algorithm or incremental thing, because otherwise, if you simply. So, this block can be approximated like a summing block, because the integration will become a summation when you move from continuous time to discrete time and this can be realized by means of an incremental algorithm. For example, here you see here it is u k. Suppose, let us say we have represented.

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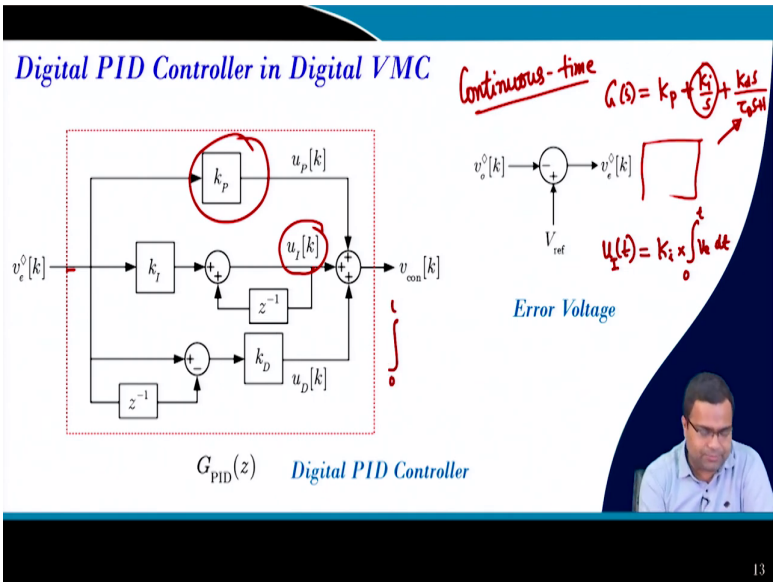

For example, let us consider we are talking about. Suppose you want to get the u of let us say u of i integral action is nothing but our analog gain v e into d t ok 0 to t let us say ok. Now, if we take this 0 to t that means.

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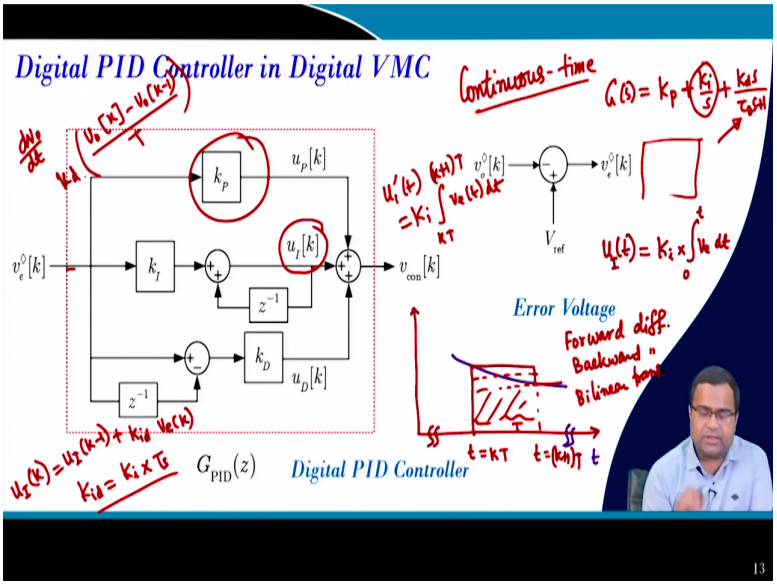

If we draw the error voltage, we have certain this kind of error voltage profile. This is the profile of the error voltage. Now, we are talking about different sample like we are sampling here; we are something here. So, only we have these available samples are there. We do not have full access here. So, these are the ok.

So, let us say we have here, we have here. So, when you say integration; that means, it is basically suppose we are talking about this particular time. We choose some, let us say, to make it much simpler. I want to highlight some part that means let us say this is the part I am highlighting. I am highlighting some particular part again you can. So, in this part, I am taking this is the sample again. It is going like this.

So, this is my t equal to let us say KT, and this is my t equal to K plus 1 T. So, here if we take the integration; that means, let us say u i of some dash where we are trying to integrate k i between KT 2 k plus 1 T v error t dt. Since this period is T this period is T. So, this area under the curve can be computed in different way. So, if you take this one, then this will be the area. If you take this one, this will be the area. So, based on that there are or you can take their average where this will be the area ok.

So, this thing can lead to call forward difference formula backward difference formula and another is called bilinear transformation or Tustin method. So, I am not going into this, but this can be realized. This integral u of k, if we take the backward difference formula u of k can be realized by u of k minus 1 plus; this is the discrete time integral gain into error voltage, where u of k minus 1 where k id is simply continuous time integral gain into the sampling time ok.

So, this can be represented by this. So, this is the velocity algorithm by which and the derivative you know if we take dv 0 dt. So, here it is taken as you know v 0 k minus v 0 k minus 1 divided by T. So, this is what it is taken and this whole thing into k d is my this ok.

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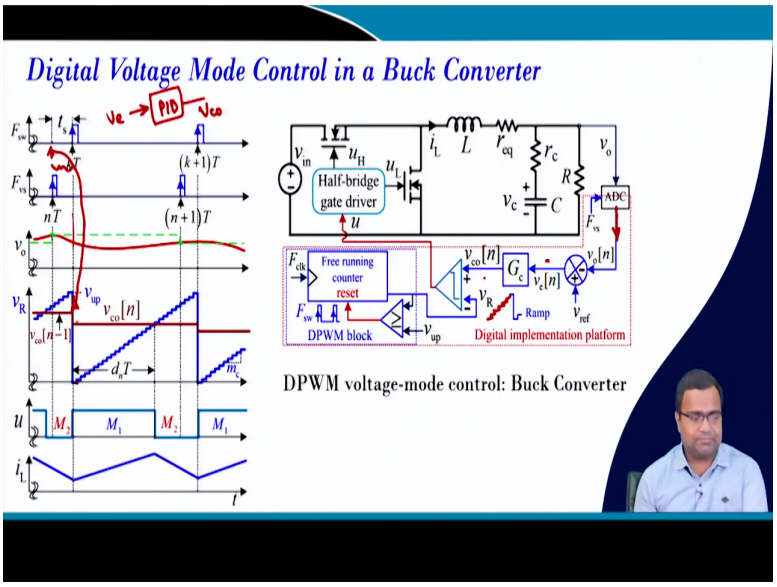

Now, coming back to our digital controller as I said this is A to D converter your sample voltage, this is error voltage, then control voltage and now, this sawtooth waveform is generated inside the digital control. So, there is nothing outside ok. And we have this if we want to draw the waveform and we have to discuss, generally we need to send the sampling command much earlier, because it will take some time to convert the continuous time signal like it a.

It will include the ADC conversion time and controller computation time, and this time can be pretty large. In fact, it can be comparable with the switching period or even in some cases it can be higher also, because we need at high frequency, we need to reduce the burden of the computational burden ok.

And now, we are going to have this sawtooth waveform and this is our sampling clock, and this is the actual switching. So, here, as if once you get the sampling data, this data will be computed and will be ready at this point, because as if this error signal will go through our PID controller and output of the PID controller will be ready here. So, it will take care of the ADC conversion time plus the PID controller computation time.

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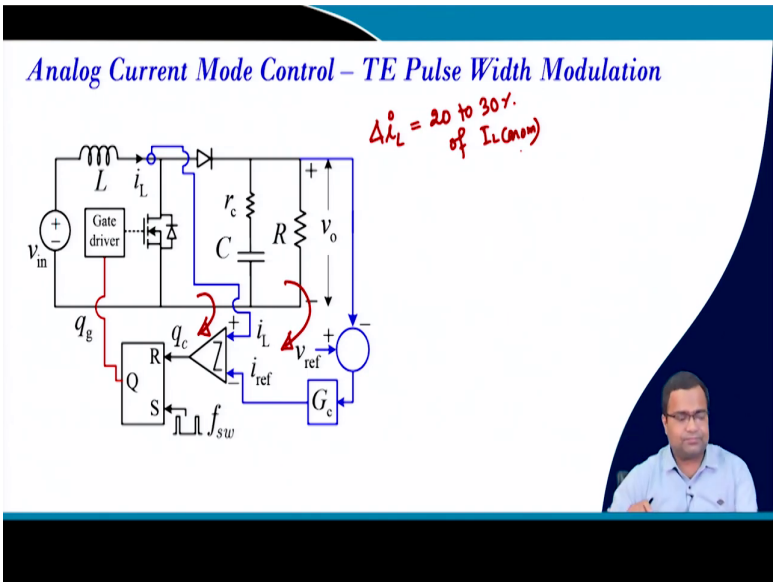

Then, we can do regular PWM operation. If you go to analog current mode control; current mode control, we have 2 loop control. One is the current loop, and the other is the voltage loop right. And we know the current loop voltage loop can be sampled once per cycle, but the current loop cannot be like that, because the current ripples are quite large.

And current ripples are generally, we have discussed in the beginning like you know lecture number 7 that it is taken to be around 20 to 30 percent of I L average nominal value ok. And that is why it is pretty large whereas, for output voltage ripple it is 2 percent of the nominal voltage. So, where we can take one sample per cycle for voltage, it can retain more or less the information, but in current we cannot do that.

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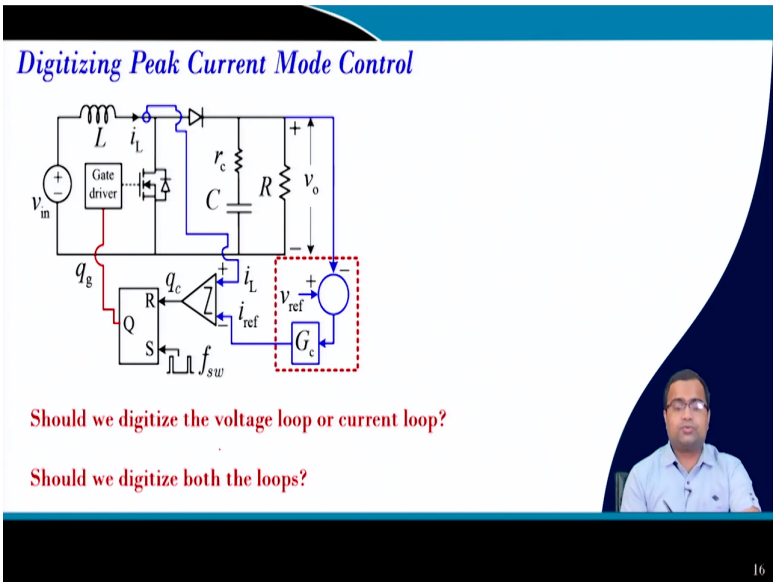

So, the next question how do you digitize the peak current mode control. Should we digitize the voltage loop, should we digitize the current loop, or should we digitize both the loop?

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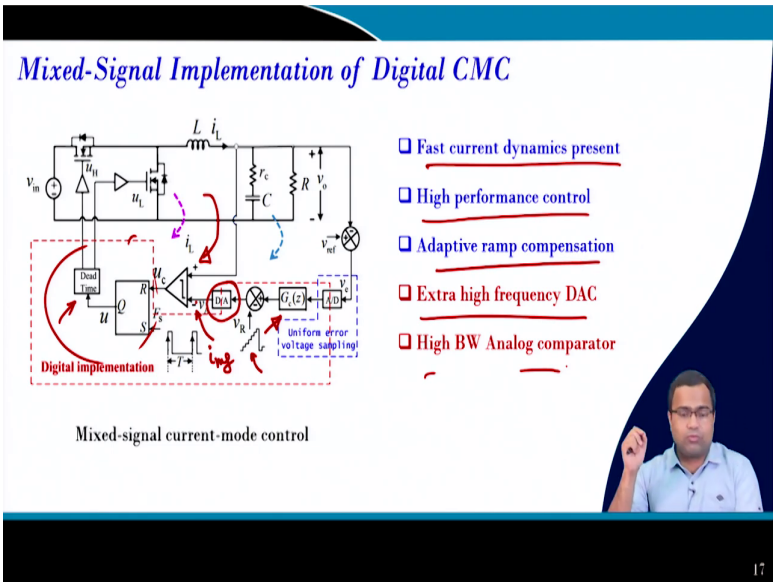

So, one of the solution if you go for mix signal; that means, since our current loop requires faster. It is the fast dynamics and we need to retain the ripple information we should not now digitize the current loop. So, current loop let it be in the analog domain, but the voltage loop is digital domain; what is the advantage, because since you have a compensator in the voltage loop. So, we can play with the tuning that we have learned right.

Because we have already talked about gain scheduling, different type of control algorithm; why they need to adjust the controller gain based on the operating point requirement. We have also learned the large signal tuning where we need to update the gain based on the operating condition. So, that can be easily done in the digital controller and then the reference current will go it pass through a D to A converter and then the reference current.

So, here you can think of it is my reference current peak current, and that is compared with the inductor current in the analog domain and; that means, we have an analog comparator and then, the comparator output is digital. So, then we can put a latch circuit the whole dead time and this whole dead time everything in digital. So, we can adjust the dead time based on our load information and other information right.

So, here the first current dynamics is present. It is in analog domain; high performance control can be implemented. And I will show you some case study in the future lecture. Adaptive ramp compensation is very easily possible. So, the ramp is in the digital domain, but you need an extra A to D, D to A converter here and high bandwidth analog comparator is still required, because that consume lot of power and. So, our next target is how to replace.

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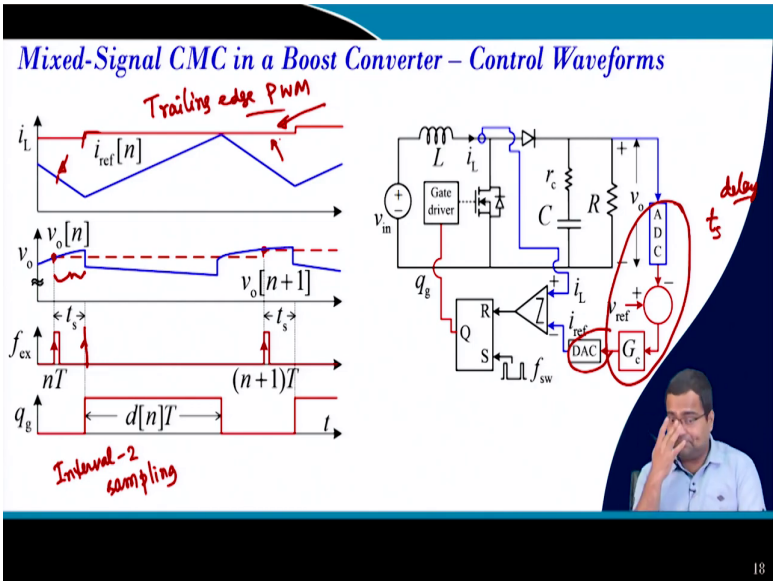

If we take the mix signal current waveform in the boost converter; as I said, we take the output voltage sample here and we provide this delay time so that our computation of the controller that means, this whole process can be completed this delay; that means, here it is the t s delay.

This whole process of sampling as well as computation can be completed including the DAC it include the DAC. So, that your analog reference current is ready. Once it is ready, then your actual switching clock start. So, this is your switching clock start then switch turns on now it is the regular trailing edge modulation; that means, it is the regular trailing edge PWM, but with some sampling delay.

And we are taking the sample during the off time; that means, when the switch is off. So, this is sometime called interval 2 sampling; interval 2 sampling ok. So, once you that means, we can realize this mix signal current mode control implementation. So, you can see everything looks like our analog control: what we learn; there is nothing new. Only thing due to the sampling your this has there has to be some delay.

Another interesting point in analog current mode control, the peak current is coming from the analog loop where the peak current actually varies within the switching period, because it is a continuous function, but in digital control; since your sampling once per cycle, this peak currents remain constant for the whole cycle. So, it looks like a constant current reference for the whole cycle and it will get updated in every cycle.

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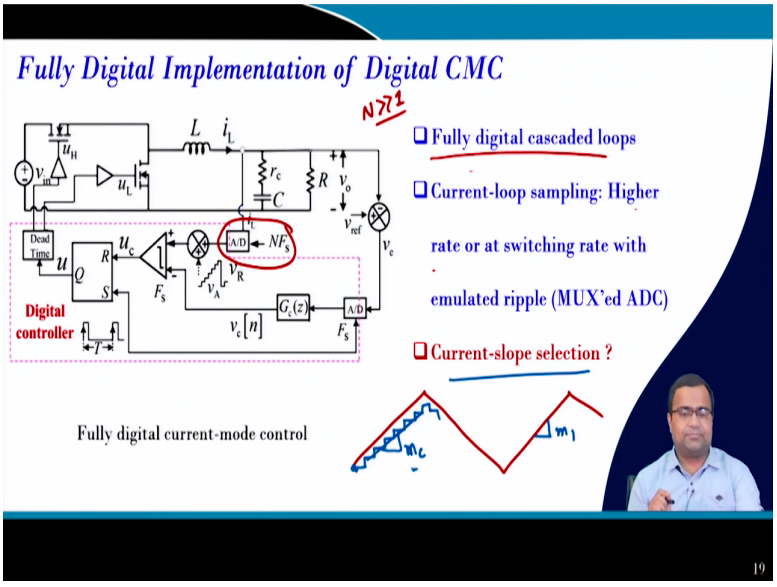

In case of fully digital, we know that the now the current loop is in digital domain, but we need to sample either at a high sampling rate or we can sample. That means a cascaded loop. Either you can use the higher sampling rate; that means, this N; N can be very, very high, but

that is that is called multi sample, but generally that will consume a lot of power, because ADC sampling requirement is very high.

Or you can sample the same rate of the ADC of the voltage and then you can add a ram. For example, if I draw a current like this is my inductor current right. Now, I want to take this sample. Now, in the digital controller, I can add a sawtooth waveform inside. It is like a STR case like I can emulate. And but the question is that what should be the slope of this, like a compensating ram sort of inside the digital control, but this is the actual current slope.

So, how can we get the slope equal to this current slope it is not? In fact, required ok and there are many architectures. You know many techniques are available, where either you can find alternative way and there are many such things so, but we are not going to discuss here. Only thing we need to get the right slope; it need not to be the exactly equal to m s m 1, but it also comes has some stability requirement and that not I am not going to discuss here. But the bottom line is this we can emulate this current.

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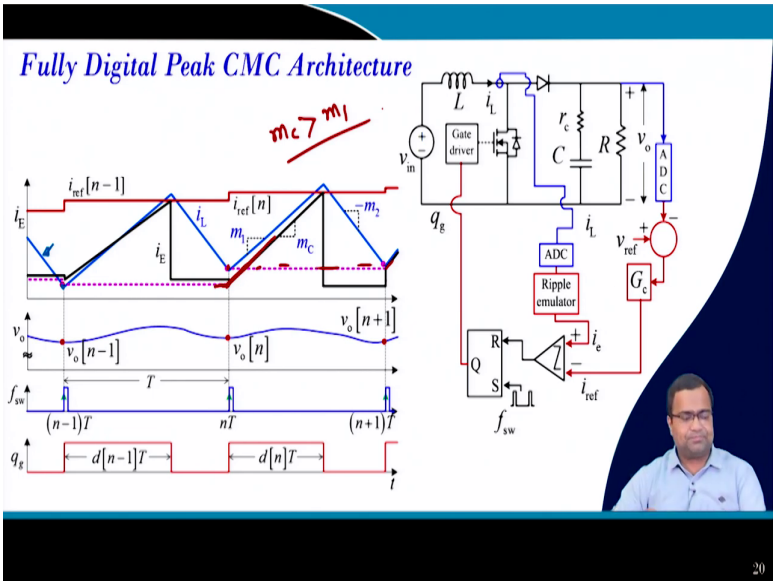

How does the waveform look like? So, if we take the sample of the current, because since we are taking the valley current sample and you need to emulate this, but as I said when you send the sample commend, nearly it takes time to get the actual sample available, because there will be A to D conversion delay. So, generally we cannot take the same sample and emulate in the same cycle.

So, what is the common thumb rule? You take the sample of the current of this inductor current in this cycle, but you emulate in the next cycle; that means, this valley current as it is extended here. Now, we are adding this ramp and this the black colour is the ramp that we are adding; that means, if I use a red colour. So, this is the ramp we are adding here. So, this similarly, this current is extended here in a reading ramp here.

So, by that way, we can implement fully digital current mode control and there are many literatures. And you know in future we may come up with something like this.. But for the time being there are different type of architectures are available and they have various stability property requirements and there those are fundamentally different from analog current mode control.

The current loop stability can be requirement is much more stringent or basically mores ramp slope; that means, you need m c to be higher than m 1. How much higher? And there are many architectures, where you can also manage m c equal to m 1, but we are not going to discuss here, but I think it is possible.

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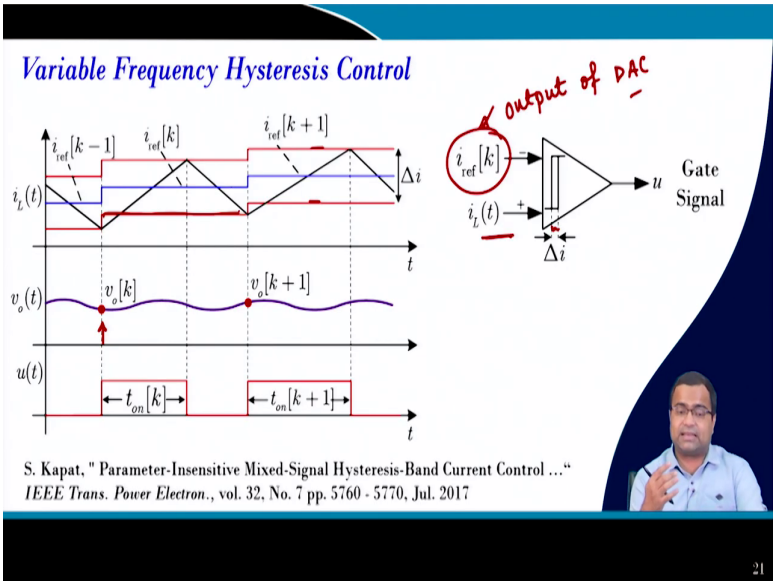

But if you go to variable frequency control, we have talked about hysteresis control right. And we talk that if we use a hysteresis current band, then we can keep the current ripple within the band right. So, here again, the current inductor current is analog domain and the reference current is coming, which is the two-reference current is coming from the digital loop right.

So, this hysteresis band either you can implement a hysteresis comparator or you can use you know there are architecture that we will discuss shortly that you can use the single comparator. And a single D to A converter. So, you need a D to A converter here. So, this will come output of D to A converter. And this D to A converter input is nothing but the controller output.

And here, if we sample once power switching cycle and it is reported in this paper the one sample per cycle, then you can perfectly stabilize this whole hysteresis control using one sample per cycle, but since the hysteresis control is a variable frequency control. So, we should not use a uniform clock.

And that is well reported here. Because if we use the uniform sampling clock, it will lead to multi limit cycle oscillation and what we have to do. We have to use the event-based sampling; that means, the event is here whenever switch tries to turn on, then you take the sample ok and then you provide some delay where the switch will turn off after a certain delay and then you continue ok.

So, by that way, you can ensure that the peak reference current will not vary throughout the whole cycle and that will make the whole system; that means, in analog hysteresis control, we saw the actual current ripple is smaller than the hysteresis band, because of sensitivity due to the gain controller gain you know.

I think it was in the fourth week or third week, where we have discussed in detail about hysteresis control. I think it is in the fourth week, where in analog hysteresis control the hysteresis band is higher than the inductor current ripple. Here by means of one sample per cycle you can make them equal ok and you can make a stable.

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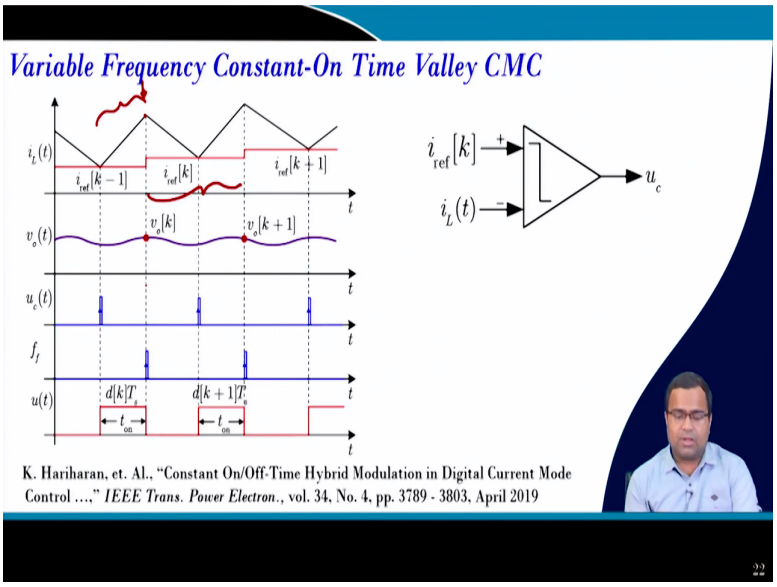

And if you go to variable frequency constant on time control in fact, in the next lecture, we will show the waveform the experimental result that it remains same and if we go to constant on time control, it is also a variable frequency control we have learned. Again, we can use this event-based algorithm.

For constant on-time, we generally take the sample before switch turns on off because that means this on-time actually comes from our mono shot timer. So, once the timer almost finishes the timing, then you can send a sampling command. And then after short time, you actually turn off the switch, then that sample actually takes the valley current generation and then you can do the regular valley current operation.

So, it in the sense that the valley current remains fixed for the whole duration. Again it is an event-based sampling one sample per cycle. You can stabilize and you can get wide operating range. This is also reported in this paper, where you can stabilize and we have shown that you know by means of a one sample per cycle, we can get a stable periodic behaviour for a wide range of operation.

And since in variable frequency control we saw, the current loop never becomes unstable for the entire duty ratio range. So, you can take the benefit of that current loop inherent stability as well as the digital controller tuning where you can adjust the. This time period can be adjusted by setting a suitable on time; that means we can set the suitable on time in such a

way so that we can regulate the switching frequency. This was constant; I think it should be constant on time.

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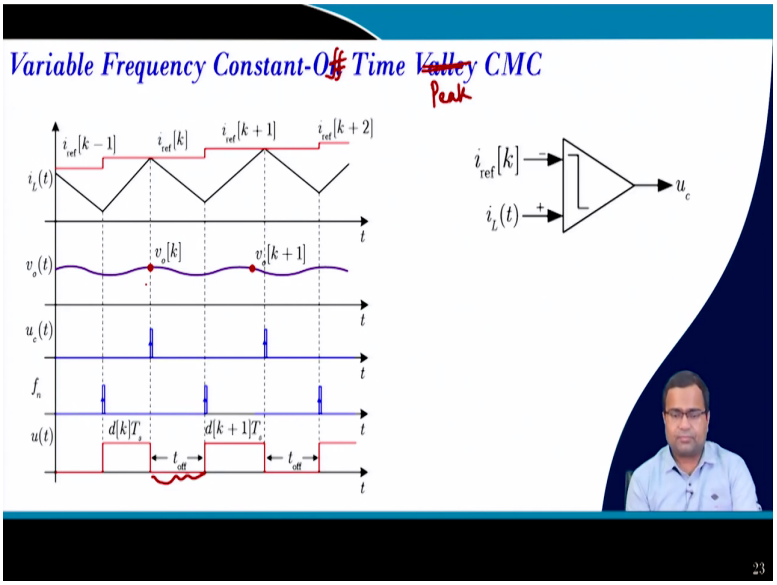

And this should be constant off time. So, it should be constant off time and it should be peak current mode control sorry peak current mode control. Here, it is similar to peak current mode control where the off time is fixed, you can see the off time is fix. And we are taking the sample whenever the switch hit the upper limit; that means, that means in the mono shot timer when sorry it should be taken here.

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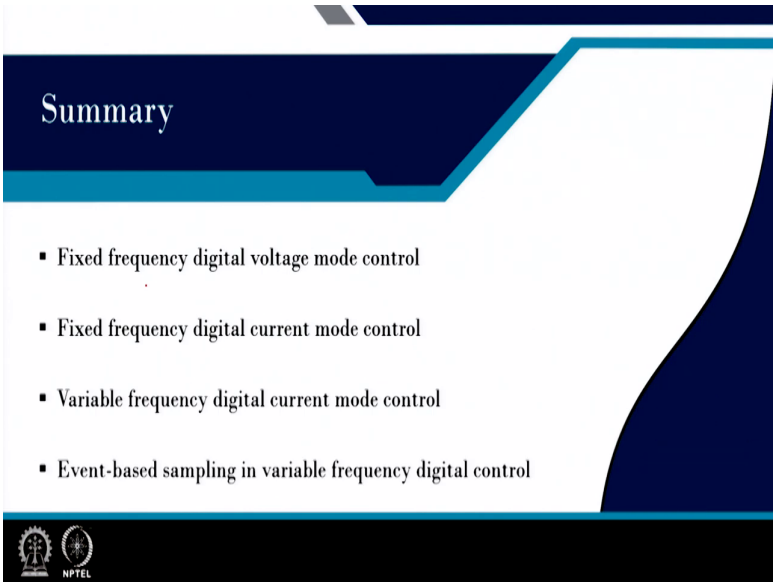

So, we can also implement the peak current mode control for constant off time and that we can discuss in the next lecture, where we can actually implement the peak current mode control variable frequency modulation. So, in summary, we have discussed fixed frequency digital current mode voltage mode control, fixed frequency digital current mode control.

Then, variable frequency digital current mode control and event-based sampling in variable frequency control for hysteresis as well as constant on time modulation and it can achieve. We will show in the next lecture wide like a stability range for a wide range of operation. So, with this I want to finish it here.

Thank you very much.