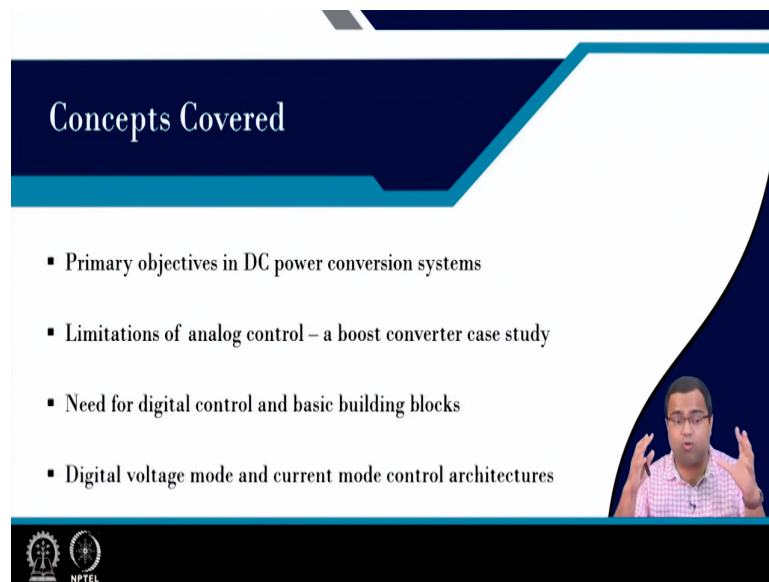


Control and Tuning Methods in Switched Mode Power Converters
Prof. Santanu Kapat
Department of Electrical Engineering
Indian Institute of Technology, Kharagpur

Module - 12
Performance Comparison and Simulation
Lecture - 57
Digital Control in High Frequency SMPCs - Introduction and Motivations

Welcome. This is lecture number 57. In this lecture we are going to talk about Digital Control in High Frequency Switch Mode Power Converter; Introduction and some Motivations.

(Refer Slide Time: 00:36)



Concepts Covered

- Primary objectives in DC power conversion systems
- Limitations of analog control – a boost converter case study
- Need for digital control and basic building blocks
- Digital voltage mode and current mode control architectures

The slide features a dark blue header with the title 'Concepts Covered' in white. Below the header is a white area containing a bulleted list of four topics. In the bottom right corner of the slide, there is a small video inset showing a man in a pink shirt and glasses speaking. At the bottom left of the slide, there are two logos: the Indian Institute of Technology (IIT) logo and the NPTEL logo.

So, here we are first going to talk about primary objective in DC power conversion system, then what are the limitation in analog control and I want to show using a boost converter case study. Then, we need to need for digital control and some basic building blocks and some introduction of digital voltage mode and current mode control architecture.

Since it is not a digital control course. So, I want to give some brief introduction in this lecture and the next lecture. So, that you know we get some motivation why to go for digital control and maybe in future we can think of digital control in another course.

(Refer Slide Time: 01:09)

DC Power Conversion – Primary Objectives

Source voltage variations

- Tight voltage or current regulation
- High efficiency over a wide range
- Very fast transient performance
- High power density – smaller size
- Stable behavior – predictable ripple

Load current variations

So, here we are talking about a DC power conversion system and we have discussed this in lecture number 1; in the first lecture, the primary objectives; that means, we have a DC source and then we have DC load and the source voltage can vary load current can vary and we have also discussed dynamic voltage scaling.

So, we need to achieve tight voltage regulation. In some cases, we need to regulate the current. Then we need to achieve high efficiency over a wide range and very fast transient response with high power density and small size. We have to ensure stability.

(Refer Slide Time: 01:44)

Challenging Control Requirements

Dynamic	Static
<ul style="list-style-type: none">• <u>Fast transient response</u>• <u>Small overshoot/undershoot</u>• <u>Fast-scale, small- & large-signal stability</u>• <u>Low audio-susceptibility, output impedance</u>	<ul style="list-style-type: none">• <u>Higher efficiency – lower thermal overhead</u>• <u>Conducted & radiated EMI</u>• <u>High switching frequency (F_s) – compact size, high power density</u>• <u>Good line/load regulation</u>

Now, the question is what are the control requirement and what are the challenges. So, it can be categorized into two parts; one is the dynamic requirement, another is the static requirement. In the dynamic requirement, we will talk about very fast transient response; that means, the fast transient response is something which is obvious.

And we have spent a lot of time to achieve this. Initially we started with small-signal model. We have developed design and tuning method to get whatever the achievable performance within the model limit. We also discussed non-linear control. Then also we have discussed non-linear tuning, and we got the fastest response.

And we also discuss something, some another reconfigurable circuit which can even improve the performance. Then we need to reduce, thus you know we need to achieve small undershoot overshoot for both current and voltage and we need to ensure the fast scale stability; that means sub harmonic stability should not come.

There should not any large-signal or small-signal stability because we also talk about large-signal stability like you know Lyapunov stability and small-signal like we have to ensure that it has sufficient stability margin like phase margin, gain margin, bandwidth and so on.

And we also need to achieve low audio susceptibility and low output impedance. In the static requirement we also discuss high efficiency because we need to achieve high efficiency so that the thermal overhead can be reduced. The size of the converter can be reduced.

Conducted radiated EMI is another important because though we are not discussing here, there can be active EMI control by means of spectral spread. We can spread the spectral spectrum by means of periodic modulation by means of randomized modulation and so on. And we can operate at a high switching frequency that is one another objective and that we can use a wide band gap devices and we can reduce the size for high power density, and we also need to achieve very good line and load regulation.

(Refer Slide Time: 03:55)

Challenging Control Requirements

Additional requirements

- Reconfigurable controller – performance/efficiency trade-off
- Real-time energy optimization – customizable dead-time & Fs
- Coordinated control – improved overall performance & longevity
- Safety & reliability - monitoring, communication, action

Handwritten notes on slide:
Digital Control
PMBus

Video inset: A man in a pink shirt speaking.

So, this requirement along with this we need some additional requirement for current tense of power supply as well as for the future power supply. Some of these we need to have a reconfigurable controller because we have discussed we need to tune the controller parameter to get fast transient.

Because we should come out from the traditional analog control where we you know if we use the off chip component where we have no flexibility or little flexibility in tuning the controller parameter. As a result, our design was based on the worst case and that is not going to meet the future requirement.

So, we need to have a reconfigurable controller, whether we go by small-signal based design whether we go for large-signal based tuning or non-linear control, so our controller parameter has to be reconfigurable. That means whether we can use a one controller throughout, but update the parameter or in as per requirement, we can also change the controller configuration.

Suppose if we develop an IC which can be used either in voltage mode configuration or current mode configuration, or we can change the different modulator architecture at least for voltage and current mode, we may need a different compensator. Or we also discuss that you know load transient response type three may not be good enough. We may go for even lag-lead compensator.

So, this kind of structure can be incorporated in reconfigurable controller and that can be easily implemented in digital control so that we can take the controller that we want. And we can also update the parameter to get a fast response. And we can also do a trade off with efficiency because we saw if we achieve the time optimal response since we are reducing that you know in the previous lecture we saw the time optimal response over the classical response can improve the dynamic efficiency.

Because the number of switching event during a large recovery is reduced so that your driver loss can be reduced so, but then conventional way not only we are losing performance we may need, we may lose the transient efficiency or basically energy efficiency.

Similarly, we want to go for real time energy optimization because if we want to if we use the fixed dead time for synchronous converter then we will really lose efficiency, because the dead time will be decided by your load step size as well as your you know; that means load current and the input voltage condition right.

So, if you are operating at a higher load; that means, your switch when it turns off you it will swing from that load current to the zero current, but if the load current is low, then the current magnitude is reduced so why do you unnecessarily use a larger dead time so, you can reduce the dead time so, you can optimize.

We can use the coordinated control; that means, we can coordinate between multiple controller because we discuss that in a smart phone there are multiple POL we need to coordinate. So, that you know we can use the information. But you have a battery, and if all the converters undergo transients, then the battery has to supply huge current, and the battery can collapse.

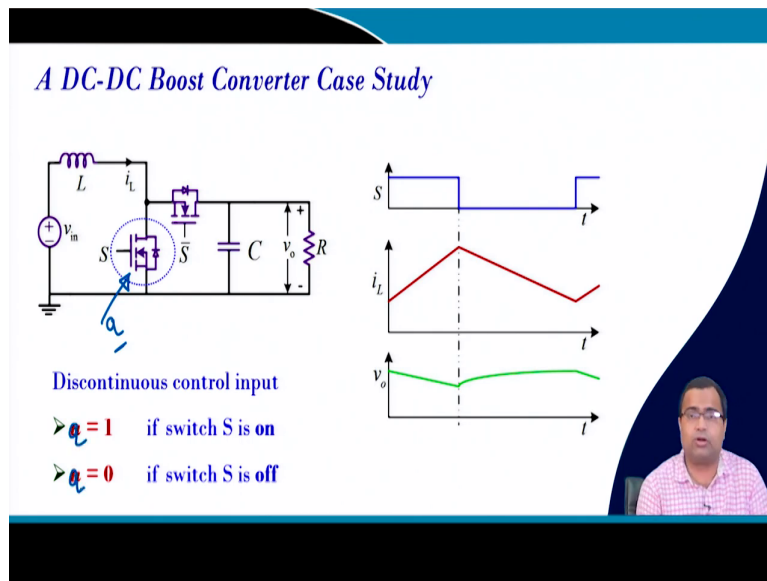
So, this coordinated control can help to reduce we have to only respond to the transient, which is critical and then slowly we will respond to the other transient. Similarly, we can coordinate between the controller because if there are multiple converters there can be interaction and that can lead to a stability problem. And this part is also important for microgrid application and other application where this coordinated control can really help to overall improve the performance stability and efficiency.

And this can be done by means of communication because we are talking about PM bus communication PM bus and now the products are also available. So, it is a trademark product

technology where this is a protocol where you can share it share the data and the clock between multiple converter by this communication.

So, this communication also we can go for more reliable power supply design. We can make the power supply safe and also we talked about hot swapping multiple controller. So, by this information exchange, we can achieve the hot swapping technique as well. So, this motivates to go for something like a digital control already. So, something like we go for digital control.

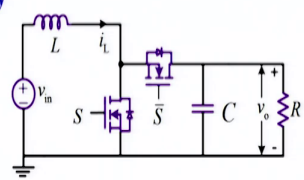
(Refer Slide Time: 08:34)



Another thing if we take a boost converter that we have discussed multiple time and if we go for this boost converter, the gate signal we have considered earlier u here I have taken u so we have taken earlier the gate signal. So, you can use this as a q . This is our q q equal to 1 or 0 discontinuous.

(Refer Slide Time: 08:53)

A DC-DC Boost Converter Case Study



State space modeling

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -(1-u) \\ \frac{(1-u)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} Bv_{in}$$

$$v_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix}$$

Discontinuous control input

- $u = 1$ if switch S is on
- $u = 0$ if switch S is off

(Refer Slide Time: 09:00)

Linear Small-Signal Modeling under PWM

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = G_{21}(s) = \frac{(1-D)V_o}{LC} \left\{ 1 - \frac{sL}{(1-D)^2 R} \right\};$$

← RHP zero

$$\Delta(s) = s^2 + \frac{s}{RC} + \frac{(1-D)^2}{LC};$$

Duty ratio d is the continuous control input

$$s_{poles} = \frac{-1}{2RC} \pm \sqrt{\left(\frac{1}{2RC}\right)^2 - \frac{(1-D)^2}{LC}}$$

So, we generally obtain a state space model which is a discontinuous control and this thing we have already discussed in the past. Now, suppose if we obtain the large-signal model linear sorry linear small-signal model, then we know how to obtain this transfer function and this boost converter. Then the duty ratio we are going to control it is a right half plane zero.

(Refer Slide Time: 09:14)

RHP Zero Effect on Transient Response

①

②

$$y_z(s) = G_z(s) \times \frac{A}{s} = \left[G(s) \times \frac{A}{s} \right] - \frac{1}{s_z} \times \left[sG(s) \times \frac{A}{s} \right] = y(s) - \frac{1}{s_z} \times sy(s)$$

$$y_z(t) = y(t) - \frac{1}{s_z} \times \frac{dy(t)}{dt}$$

And if there is a right half plane zero, we have discussed in the earlier lecture the right half plane zero introduces a undershoot behaviour right. Because if the converter has no zero; that means, if the transfer function has no zero, only 2 pole and if it is under-damped so this is the one which is number 1.

But suppose if you multiply with a right half plane zero number 2 transfer function. So, this will be there will be undershoots. So, if the right half plane zero comes close to the imaginary axis, you will have more and more undershoot behaviour like this. So, it will be more there will be more severe bandwidth problem.

(Refer Slide Time: 09:52)

Dynamics of a PWM Boost Converter

Open-loop control-to-output transfer function contains

- **One right-half-plane (RHP) zero** $s_{zero} = [(1-D)^2 R] / L$
- ❖ Higher load & voltage gain - RHP zero closer to imaginary axis
- ❖ Limited gain margin - leads to smaller closed-loop bandwidth

So, if we take the open loop transfer function of the boost converter we have a one right half plane zero in the control to output transfer function and that right half plane zero comes close to the imaginary axis at high load and high voltage gain so, that makes the bandwidth very slow. Similarly, the limited gain margin leads to smaller closed-loop bandwidth.

(Refer Slide Time: 10:12)

Dynamics of a PWM Boost Converter

Open-loop control-to-output transfer function contains

- **Two stable poles - complex conjugate if** $R > \frac{Z_c}{2(1-D)}$
- ❖ Light load & lower voltage gain - Damping ratio decreases
- ❖ Thus larger overshoot/undershoot & longer settling time !!


Now, that transfer function also consist of two poles which has complex conjugate zero and that; that means, under high load light load condition you can have a poor damping and that may reduce your phase margin and lead to more overshoot undershoot.

(Refer Slide Time: 10:28)

Dynamics of a PWM Boost Converter under VMC

- ❑ **Loop transfer function** $L(s) = \frac{k_f(1-D)V_o}{F_m LC} \left(1 - \frac{s}{s_{rhp}}\right) \times \frac{G_c(s)}{\Delta(s)}$
- Locations of RHP zero & open-loop poles – **unchanged**
- High load - RHP zero effect; Light load (i_o) – **complex poles**
- Pole/zero compensation difficult for varying i_o and V_{in}
- **Type-III compensation or PID voltage controller needed**
- Fixed-gain controller – Design based on **worst-case scenario**
- Control BW up to $f_{rhpz}/5$ – **Limited achievable closed-loop BW**

Voltage-mode PWM not preferred !!

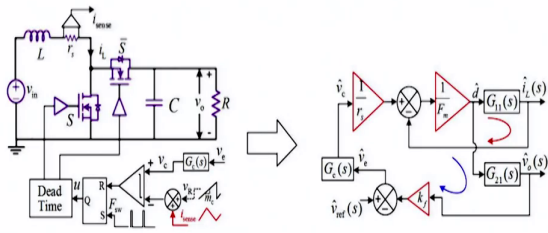


So; that means, if you take the dynamics of a boost converter the RHP zero limit, you know your high load and high voltage condition bandwidth limit light load condition. You have complex conjugate poles. So, the pole zero compensation become very difficult and we have already discussed this case study using a type three compensator and then fixed gain controller may not be sufficient based on the worst case design.


And generally our f control bandwidth is limited to one fifth of the RHP zero. So, that is why voltage mode control is not preferred for a wide duty ratio operation in analog control.

(Refer Slide Time: 11:06)

Dynamics of a PWM Boost Converter under CMC



- ❑ **Cascade control, control-to-output TF** $\frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{1}{r_s} \times \frac{G_{21}(s)}{F_m + G_{11}(s)}$




(Refer Slide Time: 11:12)

Dynamics of a PWM Boost Converter under CMC

□ **Cascade control, control-to-output TF** $\frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{1}{r_s} \times \frac{G_{21}(s)}{E_m + G_{11}(s)}$

- Location of RHP zero – **unchanged**
- Poles $s_{poles} \approx \frac{-V_o}{E_m L} \frac{-1}{2RC}$ - approximately **single-pole system**
- **Type-II compensation or PI voltage controller enough**
- Control BW limited to $f_{rhpz}/3$
- **Fixed-gain controller design for worst-case: $BW \approx f_{sw}/20$**




If we go to current mode control our right half plane zero, you know we can convert into a first order pole, but the right half plane zero still exist and it remain unchanged there it does not change the right half plane zero when you move from voltage mode to current mode.

But it gives a single pole approximation of the pole and we can simply use the type two or type three compensators. Here we discuss that we can achieve bandwidth up to one third of the RHP zero. But if we go for a fixed gain controller, we end up the worst case bandwidth to be one twentieth of the switching frequency and which may not be acceptable.

(Refer Slide Time: 11:43)

Limitations of Analog PWM Control

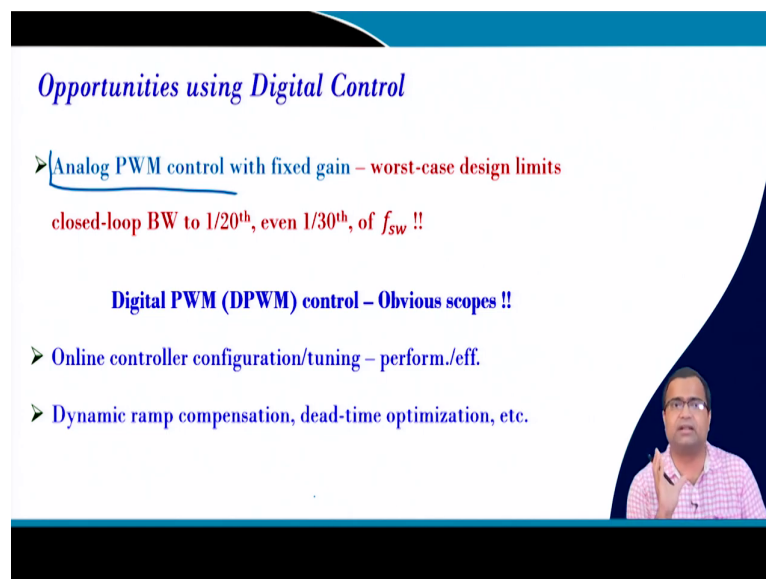
- **VMC: Single-loop control, but very difficult to compensate under varying load current & input voltage**
- **CMC: Single-pole compensation, but sub-harmonic oscillations for $D > 0.5$: Need a compensating ramp, but excess ramp slope makes poles complex conjugate**
- **Analog PWM control with fixed gain – worst-case design limits closed-loop BW to $1/20^{\text{th}}$, even $1/30^{\text{th}}$, of f_{sw} !!**



So, then the limitation of analog control if you go for voltage mode control it is very difficult to compensate under varying load current and input voltage condition. We saw under current mode control sub harmonic oscillation may come when the duty ratio exceeds 0.5 we need to compensate ramp.

But if the ramp compensation is excess, then the poles become complex conjugate and then again the problem may come what will happen we saw in the voltage mode control. And analog control using fixed gain, the worst case design of a boost converter can be even 1/30th of the switching frequency and which is not acceptable.

(Refer Slide Time: 12:21)



Opportunities using Digital Control

- Analog PWM control with fixed gain – worst-case design limits
closed-loop BW to 1/20th, even 1/30th, of f_{sw} !!

Digital PWM (DPWM) control – Obvious scopes !!

- Online controller configuration/tuning – perform./eff.
- Dynamic ramp compensation, dead-time optimization, etc.

The slide features a blue header and footer, a white central area with blue and red text, and a small video inset in the bottom right corner showing a man in a pink shirt speaking.

Then what to do? What are the opportunity using digital control? So, we can overcome this thing by means of controller tuning and that we have discussed in the previous lectures. The tuning even the last in week 11, but those tuning can be implemented in digital right dynamic ramp compensation dead time optimization is possible. So, these are some of the reason that it motivate to go for digital control.

(Refer Slide Time: 12:48)

Feedback Control – Closing Digital Loop

Voltage-mode digital PWM control

Spectrum of $v_o[n]$ with $f_s = f_{sw}$

No aliasing effects – no LPF

- Voltage loop - one sample per cycle enough
- Reduced sampling & computational requirement
- High freq. DPWM – practically feasible

Spectrum of $v_o[n]$ with $f_s = 3f_{sw}$

Discrete-time LPF needed to avoid aliasing effects in digital feedback voltage loop

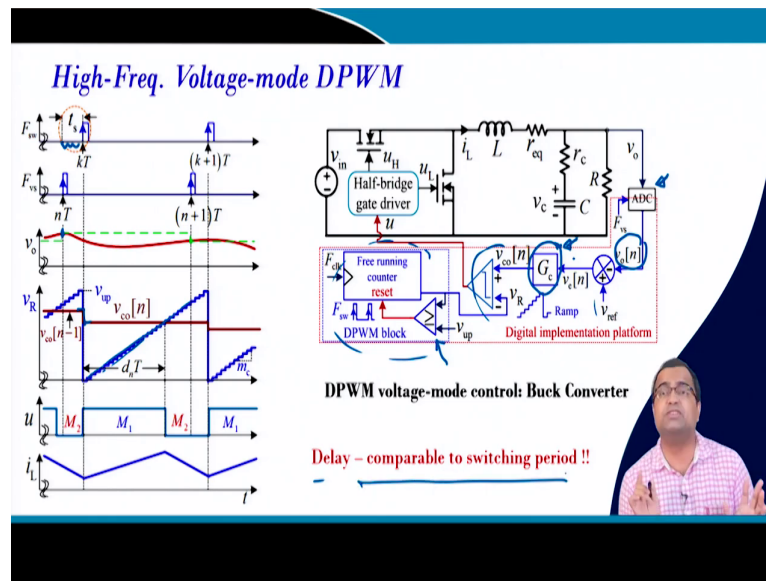
If you go to digital control, then you know in our PWM block we introduce the digital pulse width modulator DPWM. And in your A to D block, we have a A to D conversion where we have a sampler circuit and also a quantizer block. Now, the question is how to sample the output voltage in what rate we should sample?

So, if we sample higher than switching frequency, then and since the digital control, the nyquist frequency is half of the sampling frequency. So, that you will find that aliasing effect will come. So, then we need to put a low-pass filter to attenuate that effect, but if we take one sample per cycle, then in the nyquist frequency range there is no aliasing effect, so we do not need any low-pass filter.

So, one sample per cycle is the common thumb rule for DC DC converter in digital control. The voltage loop is sample once per cycle; that means, it reduces both sampling as well as computation because even if you sample at a faster rate the compensator has to compute at the same rate. So, that require a lot of processing capability so, if we reduce the computation requirement then you can also reduce the power.

And high frequency DPWM is very much possible; that means, if you go for very high frequency, it is possible because your sampling reduce sampling rate is almost same at switching frequency.

(Refer Slide Time: 14:17)



Now, if we take a voltage mode control architecture. So, we have an A/D converter here so, output voltage is compared with the reference voltage and the error voltage it is the controller and then we have a digital comparator and then that actually we have a DPWM block.

And there are many architectures of DPWM block and that we are not going to discuss in this course. Because in this course, I just want to give a brief introduction in digital control and some motivation. And if you draw the waveform of the digital control, we are sampling the output voltage here, but you know that every ADC takes some time to convert; that means, the ADC conversion time. So, we need to provide some delay where the ADC conversion as well as this controller computation both can be computed.

So, your actual data, which is sample here, will be ready after computation is a control voltage and that is compared with the saw-tooth waveform and since it is a digital, it has a stair case kind of waveform. So, this will give us this kind of closed loop operation.

But the delay can be comparable to switching period because even if we are taking you know the delay we do not want a very high speed ADC because that also increases cost because we want to reduce cost, we also do not want a very high speed you know digital computation so we need to provide time.

And in fact, this delay sometime we intentionally increase in order to keep some regulatory purpose in mind and if you go to different digital control architecture, this delay has to be like one sample delay. So, the delay can be close to switching period.

(Refer Slide Time: 16:01)

High-Freq. Voltage-mode DPWM

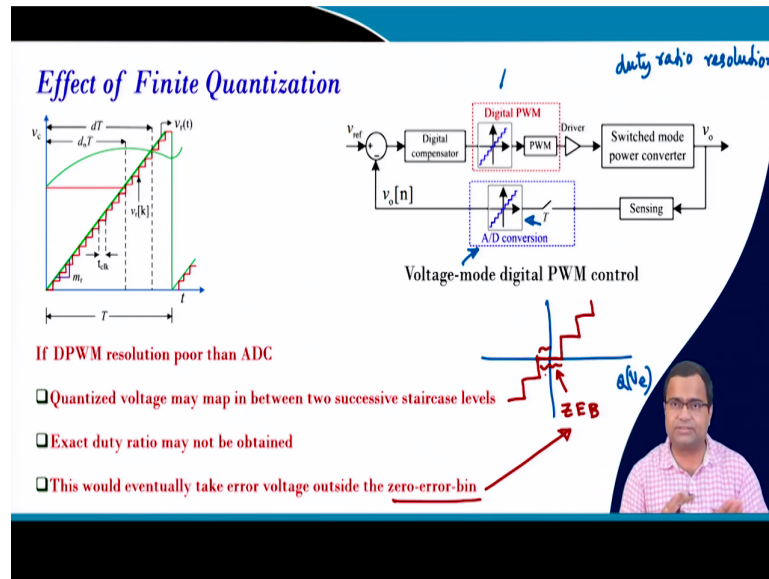
- ❑ Reconfigurable controller G_c
- ❑ Real-time energy optimization
- ❑ CMOS IC: power, size, portability
- ❑ Fast prototyping, validation
- ❑ PMBus interface - interactive

DPWM voltage-mode control: Buck Converter

Now, with this digital control, we can reconfigure this controller. We can do real time optimization by means of dead-time you can optimize in this driver circuit. So, the whole thing up to this MOSFET, including this MOSFET and from this ADC, the whole thing can be using a single CMOS circuit; that means, CMOS.

So, you can reduce the size and everything and you can do very fast photo typing for validation in like you can use an APGA based photo typing to validate idea and you design the code and you can use your HDL code hardware descriptive language. And whatever HDL code you synthesize, that HDL code can be used to synthesize your actual digitalizing. And then PM bus interface can you know it will make your power supply reliable, you can communicate and achieve higher performance.

(Refer Slide Time: 16:56)



But it comes with various price first of all you need ADC, first of all you need here there is no DSC requirement, but there is a resolution in the ADC as well as the resolution in the DPWM. And that will put a limit on your duty ratio resolution duty ratio resolution ok.

If the DPWM resolution is poor than ADC, the quantized voltage level may not be able to map properly and it will back-and-forth map between the successive level. So, exact duty ratio may not be achievable. So, it cannot lock the error into the zero error bin ok. So, what is zero error bin? That means, if you take qualitatively, this is the quantize error voltage ok. And there is a zero limit here right and then it goes like this.

So, within this voltage range their quantize voltage is 0. So, your actual digital controller will see like an error voltage zero error voltage, but actually it is not zero because within this voltage range you may have a variation in the error, but as long as within this is called zero error bin zero error bin. So, this is zero error bin ok. So, you need to lock this error into zero error bin and keep it there so that you can achieve the stable periodic behaviour.

(Refer Slide Time: 18:34)

Effect of Finite Quantization

Voltage-mode digital PWM control

DPWM resolution poor than ADC

Necessary conditions – DPWM resolution finer than ADC & DT integral gain < 1

But if you do not do that if your resolution is poor, then you will end up with this kind of behaviour which may be called as a limit cycle or it can be more complex non-linear phenomena. In general, the phenomena can be substantially different like an ordinary limit cycle and it may end up with your duty ratio saturation ok.

So, there are various necessary sufficient conditions are available and we will discuss a little bit in the next lecture. You know there are very high sighted reference that we will discuss in the next lecture that will lead to this limit cycle oscillation.

(Refer Slide Time: 19:09)

High-Freq. Fixed Frequency Digital Current Mode Control

Mixed-signal current-mode control

Fully digital current-mode control

So, but if you go to these are voltage mode control if you go to current mode control. So, the current mode control it is a two loop control. And we have a very fast current loop, but a slower voltage loop. So, this voltage loop can be kept in the digital domain by putting an ADC here, but after the controller computation then your peak current reference is coming and that you can use a D to A converter to generate the analog current reference here.

So, this is my analog current reference here, and that is directly compared to the sense inductor current and then the rest of the process is same. And this architecture is called mixed signal where the current loop is in analog and the voltage loop is in digital because we want to retain the first dynamics of the inductor current.

We can sample the voltage 1 per cycle because it is a very slow dynamic. The ripple is small, but we cannot do for the current because the current ripple is 20 to 30 percent of the nominal value. So, we must take either in analog, we must take into account the ripple information.

So, one way you keep the analog voltage current in the analog loop. Another way we can keep another put another ADC to sample the inductor current, but this ADC has to be sampled at a much faster rate. So, if this is your actual inductor current and if we take a multi-sample ADC like you know it is like this. So, inductor current can be sampled multiple time it will look somewhat closer to the inductor current.

But this multi sample ADC also has a stability issue right because in the next lecture last lecture we want to highlight some of the aspect here. So, lot of stability issue and if I use a high sampling rate, then you also need to have a very fast ADC and power will increase the cost of the ADC will increase, but this architecture where we keep both voltage and current in digital is called fully digital current mode control.

(Refer Slide Time: 21:05)

High-Freq. (Fixed Frequency) Digital Current Mode Control

Mixed-signal current-mode control Fully digital current-mode control

Voltage-sampling & controller computation – same rate of F_s

- Fast current dynamics present
- High performance control
- Adaptive ramp compensation
- Extra high frequency DAC
- High BW Analog comparator

- Fully digital cascaded loops
- Current-loop sampling: Higher rate or at switching rate with emulated ripple (MUX'ed ADC)
- Current-slope selection ?

Now, in high frequency application, the control is fixed frequency digital current mode control mixed signal and fully digital. In both cases, voltage is in the digital domain and they are sampled at the same rate of the sampling frequency.

But in the mixed signal, we keep the analog current loop so we can achieve. We can retain the fast current dynamics we can achieve very fast transient response. In fact, whatever tuning we have discussed, we have implemented with using analog current loop mixed signal current mode.

An adaptive ramp compensation is possible to make the system stable; that means, you can achieve use this current mode control for a wide duty ratio operation. And if you look at this, the ramp compensation can be added here from digitally. So, you can add any ramp that you want from the digital platform digital controller, but it comes with a price. We need ADC, DAC because if you see it require a D to A converter here so that increases price.

Also high bandwidth current analog comparator because these comparators in analog domain so the bandwidth of the comparator has to be very high depending upon what is the switching frequency, but in this case the comparator is in digital ok. So, if we look at this fully digital cascaded loop high sampling, higher rate and current loop slope selection.

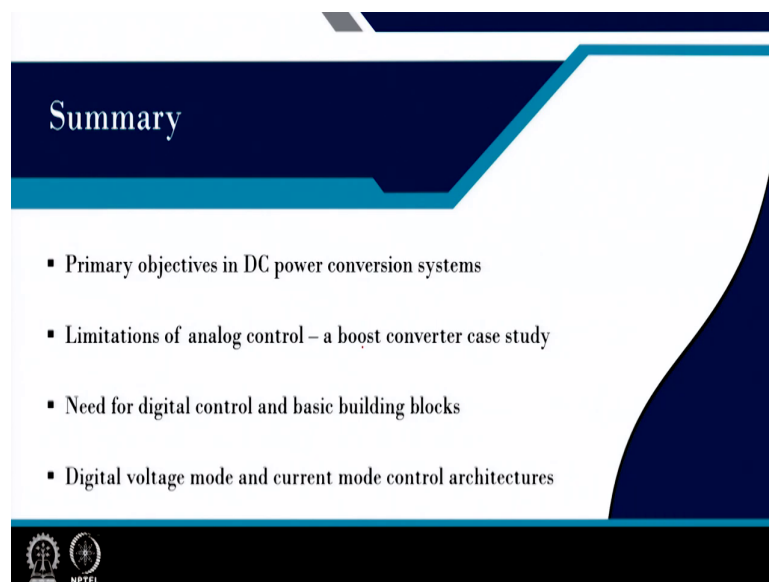
So, as I said, one way you can either sample multiple time that is one possibility or you can sample the current once and that is my sample current, but you can emulate inside the digital

loop. And this slope, whatever you are using it is my slope of the ramp not the slope and this is the slope of the current.

So, m_c need not to be always m_1 in fact, it may not be ok and actually there are multiple works that even if we set m_c because the initial objective was to get m_c equal to m_1 , but that may not ensure a different type of stability and that we will discuss in the next lecture.

So, big signal current mode control architecture I told. But in fully digital we can use one sample per cycle and then we can you know add ramp to emulate the current ripple, but the question remains: what should be the right current slope. If you choose higher, lower or equal, whatever is required that remains also another concern.

(Refer Slide Time: 24:01)



So, in summary today we have just discussed the primary objective in DC power supply conversion system. We discuss limitation of analog control and we have taken one boost converter case study. We discuss need for digital control and some basic building blocks, but this is just an introductory talk maybe in next lecture I will give an overview, but again this course is not designed for digital control so we are not going too much about digital control.

Then we have also discussed some digital voltage mode and current mode control architectures. So, with this I want to finish it here.

Thank you very much.