Control and Tuning Methods in Switched Mode Power Converters

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Module - 11
Large Signal Controller Tuning
Lecture - 53
Critical Performance Limits in Dynamic Voltage Scaling and Possible Solutions

This is lecture number 53. In this lecture, we are going to talk about Critical Performance Limit in Dynamic Voltage Scaling application and Possible Solutions.

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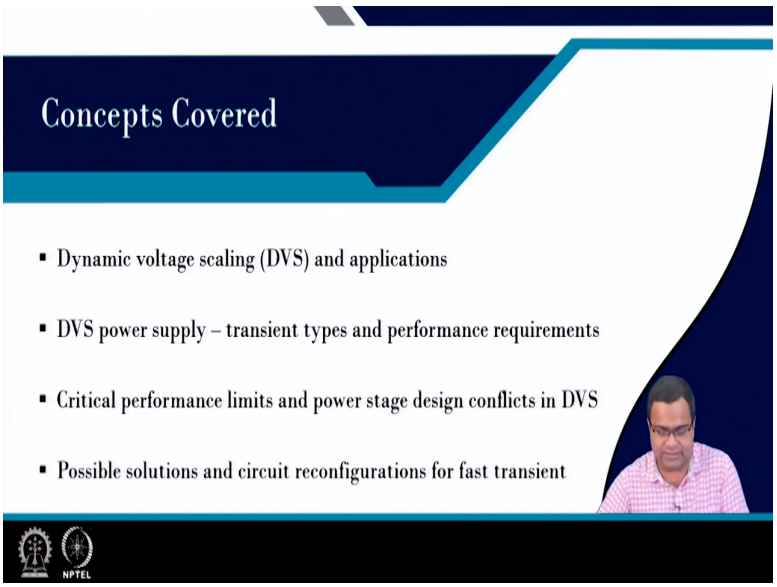

So, in this lecture we will first talk about dynamic voltage scaling and applications then DVS power supply what are the transient type as well as the performance requirements transient types and performance requirements then what are the critical performance limits and then power stage design conflict in case of dynamic voltage scaling application and then what are the possible solution.

I will discuss a few solutions which we have worked on, but there are multiple solutions are also available and which will help to improve the transient response by means of circuit configurations.

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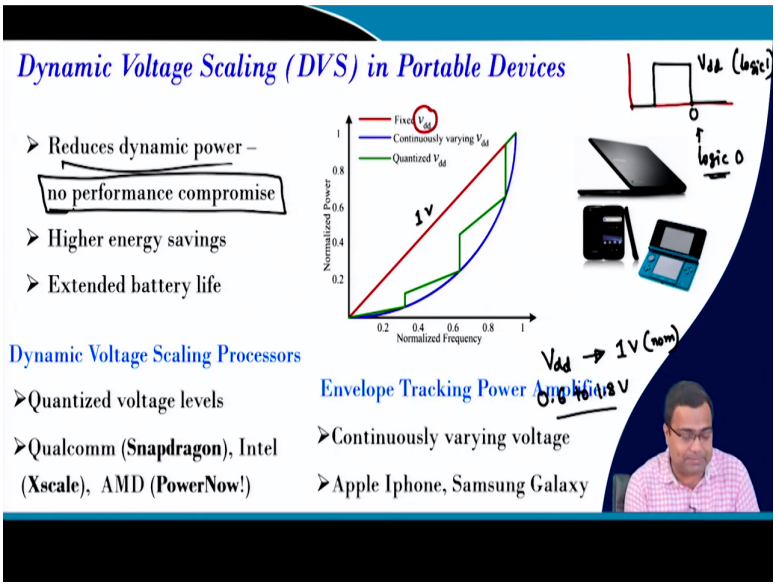

So, if we talk about dynamic voltage scaling in portable device, now the portable device is like common right. It is like a mobile phone laptop, then there are many electronic gadgets and particularly in post COVID scenario these devices. It is a common practice. Because we use more and more mobile phone, you know or you know other devices for video conferencing and so on.

So, all these devices they operate in battery like you know though in laptop we use you know adapter, but you know it is often expected because these devices are made for like it to operate in battery. So, when you operate in battery then there are many aspects in terms of because each device has various computational requirements and there are various functionalities. So, based on that, current voltage will differ with their based on their processing capability, their power supply requirement will also will be different.

But if we use such device since they are many digital devices for processor other application, where we need to provide a power supply V dd; that means, for digital processor or power supply, this is V dd. This V dd that means that is the supply for the digital processor weather should we use because we know in digital supply we talk about any digital logic if you consider.

You know we either talk about 0 or 1 logic 0 and logic 1 right. So, this corresponds to V dd and this is 0. So, this is our we call it as a logic 1 right and 0 we call logic 0. So, because of the voltage scaling because the voltage is scaling down and down, so, this V dd is also going

down because you know earlier days, it is used to be close to 5 volt. Now we are talking about 1.8 or even below even around 1 volt.

But this V dd also has some flexibility. Even though we choose, let us say V dd its nominal value. Let us say we are talking about 1.2 volt or you know one point. Let us say 1 voltage is the nominal. So, let us say we are talking about 1 volt is a nominal is a nominal.

But this V dd will also have we have some flexibility using a noise margin; that means, they can vary between 0.6 up to you know 1.8 volt why we. So, why we do? So, because and within this range, your logic will be still will be decided like or treated as a logic 1. So, this variation in the voltage is provided to do something and that we are going to discuss.

So, if we use a fixed voltage, let us say 1 volt throughout ok so; that means it is a normalize frequency. then for a fixed voltage, the power actually increases with the frequency. And we will discuss short in a very shortly the dynamic power is linearly proportional to frequency of operation because a digital circuit we need to do frequently changes the clock right, at the clock edge they have to do certain computation.

So, the power normalizes power linearly varies with the normalize frequency whereas, the power will vary in square of the V dd. So, if we reduce the voltage then with respect to normalize frequency then we can actually reduce the power, but reduction of the frequency also you need to check what will be the impact if we change the V dd.

So, first of all the dynamic power which I talk and which we are going to discuss, we want to reduce the dynamic power. So, that our battery life can be extended energy saving will be more battery life can be extended. Because we have a battery and we want the battery to last for a longer duration.

But at the same time we do not want to compromise any performance because these are all real time system we cannot expect that suppose if you are doing some computation in real time it has to do otherwise the whole system will hang right. So that means it should not be compromised in the processor performance requirement at the same time we want to reduce the power.

So, such dynamic voltage scaling processors are very much available at the quantized voltage level, like Qualcomm processor, Intel, AMD. And there is another aspect which is like you

know if you go for envelope tracking powers amplifier. Because now even if we want to talk about 5G communication or even if you have for the communication device or even if we want to you know do conversation like you know communication, so, where the we have an antenna in our mobile phone and the antenna is to communicate with the nearby tower right.

So, this kind of communication while talking we need to adjust the supply of the power amplifier. In such a way that because if you use a fixed supply then our battery will discharge very fast and the and phone will get heated and it can burn also, but because of the losses.

But if you want to reduce losses, then we need to change the supply of the power amplifier which is actually supplied to the antenna and in that process the DC-DC converter has to generate their variable supply voltage and that require a very high bandwidth power supply. And all these phones use this envelope tracking power supply like apple iPhone, Samsung Galaxy and there are many more.

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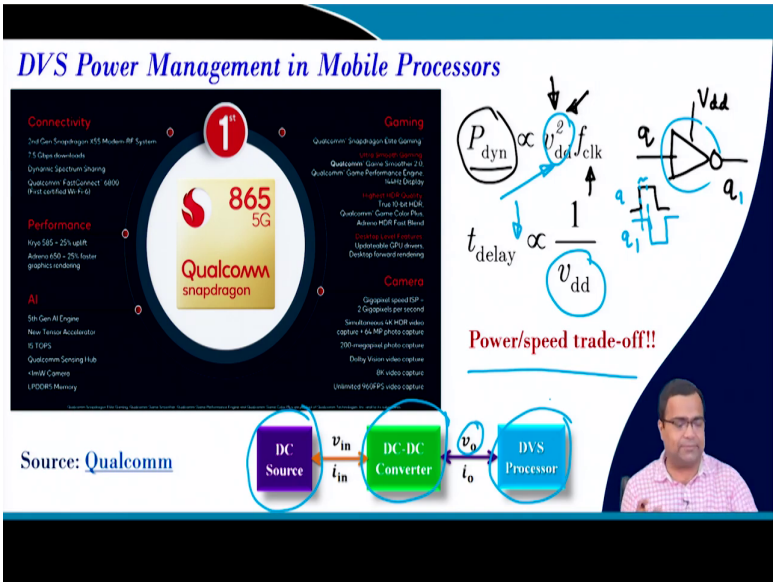

Now, this DVS power management in mobile processor if you consider this Qualcomm smart dragon processor this is one of the example we can take Intel processor and so on we have many features because these processors are sitting in our many of our mobile phone.

And now the mobile phone you use for gaming camera right then now we are talking about AI. AI processor; that means edge computation because you know we need to reduce the computational power. In some you know we have many safety features right. Even there can

be many other devices remote devices. Let us say if we use a smart camera right, like a CCTV camera, smart camera.

So, if we continuously take images right, then we cannot manage with the memory because that memory storage capacitor requires will extremely large. But if we can take if we can store if we find something going wrong because the cameras are used to detect certain event it may not be for the regular activity or even there is no activity why should we unnecessarily you know store or why should we take the image or why should we use.

The camera is on, but we are not taking the image. That means we are not processing the image. So, the want to first notice whether there is any activity and if there is any activity, then also even if we just because the activity can be normal regular activity day-to-day activity that also should not store unnecessarily there also we need to huge we need a huge requirement of memory.

But now, using AI processor, we want to detect whether the activity is desirable or is something undesirable. So, this kind of algorithm is used to identify you know if something is going wrong and then we want to take you to know the actual image with high-resolution image so that can be used as a proof.

So, in such cases you know these are all portable device they are sitting somewhere else where there may not be any access to the power supply because this may be a remote camera where it will operate by a battery and we need to extend the battery life. So, as I said, there are multiple stages of camera. So, camera is just monitoring, but not storing, not no processing, then the power supply requirement may be very low.

But suppose if there is some activity, but that activity the camera will slowly start you know activating its feature processing feature storing feature, but not to the full extend as long as it identifies that something goes wrong when it has to come to the full place. And then we require the maximum computation and there the voltage requirement will be different.

So, this performance requirement when we are talking about smart camera when we are talking smart phone when we are talking about 5G communication. Because even for communication also we may not need to use a high voltage or the volt same voltage level when there is no communication or where there is only very like a little communication.

Like we are just surfing internet then the data requirement is different, the speed requirement is different, but suppose we are watching a movie or we are playing an online game then the supply requirement will be different. So, all this requirement we should not use a fixed supply because otherwise your whole power will be battery will be discharged very within a short duration.

So, the dynamic power because all these processors are linked with the CMOS processor where we use a v dd to supply the CMOS and the v dd supply voltage decides the dynamic power. So, if we use a higher voltage; that means, we need a high power. One of the example suppose all of us has laptop right and you know if you take most of the laptop there are different battery feature like one of the feature is high performance mode the other feature is balance mode and the other feature is battery saving mode.

What will happen if we operate all this feature without you know only when the laptop is running in battery. Because we are not supposed we are not using we have not connected plug in to the power supply, it is running in battery? In that case, if suppose we connect, we use the high performance mode and suppose we are running. Let us say MATLAB simulation high extensive MATLAB simulation, then you will find the simulation is going fine. It is, you know, happening much faster.

But suppose you have suddenly changed the power mode to the battery saving mode you will find the MATLAB become very sluggish, it takes a lot of time ok and it can even hang. But if you use a balance mode, then you know it is a trade of. It will be lower performance than you know when it is. It was the first case in the high performance mode, but it may be better than the battery saving mode.

So, all these features nothing but changing this voltage and clock frequency of the processor. That means we have a processor where we have certain you know, I would say certain voltage requirement and the clock requirement of the processor because our processor actual rating can be very high.

We you know we are talking about gigahertz processor right few gigahertz in the clock. v dd should have a certain range, but we need not to operate the processor at the highest clock level. Even we can operate at a very low clock frequency if the activity depending upon the task or the activities.

So, if we can reduce the v dd then we can reduce the dynamic power and we can save the battery life even we can reduce the clock frequency we can save the battery life, but the penalty comes when you reduce the v dd of a digital clock. Let us say we are talking about a NOT gate, a simple NOT gate where this NOT gate has a v dd right.

And since we are applying this signal like say q you will get invert q, but this inversion will also come with a delay. That means it is about to get inverted that we are going to see the q bar, this is q, but they are not exactly. So, it is I can say it is not exactly q bar. I would say it is you know something like q 1 q 1.

So, you can see there is some delay right and this delay propagation delay will be different or it will increase if we decrease the v dd of this NOT gate because the propagation delay varies inversely proportional to the v dd. That means in one hand we can reduce the power by reducing v dd, but on the other hand the delay increases such.

So, that your computational you know the speed up computation or basically the speed of yeah computation task also deduces. So, it that is why your MATLAB you know when it runs you are running a MATLAB with a lower voltage; then it will take more time. So, that is a tradeoff between power and speed and that is what all about the dynamic voltage scaling ok.

And in order to adjust this power dynamically because we are talking about certain tasks which require certain voltage level and it also has a certain deadline. So, we need to meet within the deadline and we can reduce the voltage as much as possible without missing the deadline.

So, we need a dynamically adjusting or adjustable voltage for the processor and that has, but we only have a one DC source, which is a battery. So, that has to be done by a DC-DC converter or switched mode power converter. So, the objective of this converter to change this voltage in order to optimize the power consumption by this processor without sacrificing the performance or without missing the deadline.

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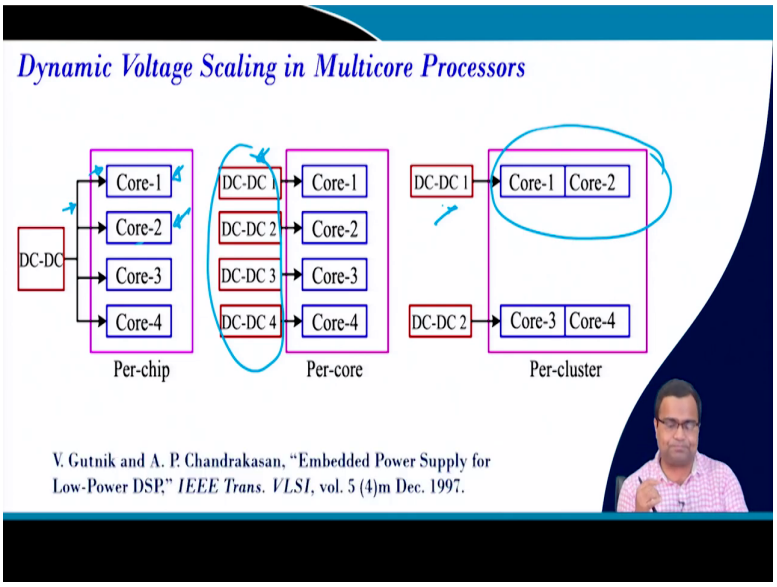

So, dynamic and if you take the multi core processor because now most of the processors are multi core because your computation requirement is increasing significantly and at the same time our task has to be divided such that we can throughout can be very high. So, very high throughput and that is what the multi-core processors are.

But if for each core if you use a single DC-DC supply then if the task of all cores is different from they may not we may not be able to optimize the efficiency or the utilization of this core by using a same supply. Because if you use a same supply to all the core then we need to select the highest voltage so that none of the core meets the deadline.

But maybe the core too may require a very lower voltage. So, we are unnecessarily giving a higher voltage. So, the losses the dynamic power losses in core to may be high. So, one supply for whole core may not be a good solution. So, can we then should we use dedicated DC-DC power converter for each core? That would have been best.

But that may not be you know practically recommended because that can huge expense. It will be expensive. So, many power converters because you have many core like a 16 core, 32 core processor. But it depends I mean whether you really need if each core current requirement is high it may happen that we need one converter for each core otherwise you can make a cluster where the cores can be clubbed together two cores can share one common supply and so on. And that can also be made; that means we need to also think of dynamic voltage scaling for multi core processor.

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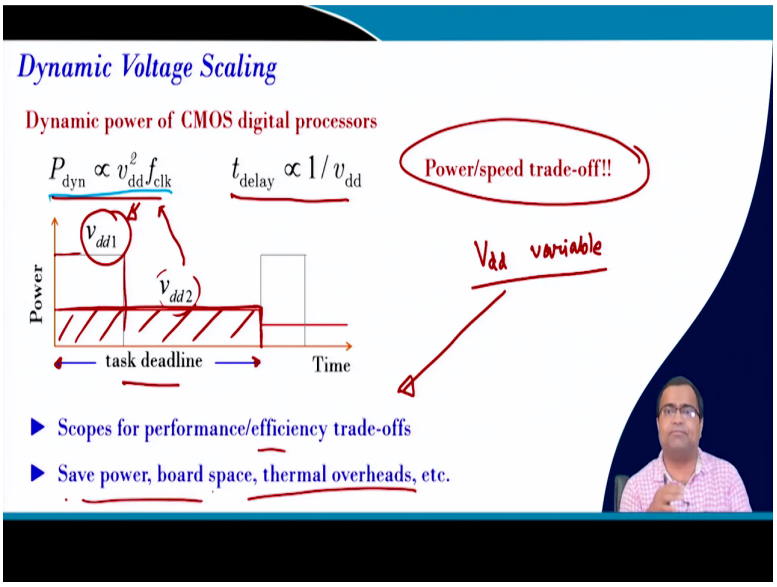

Now, the next question in dynamic voltage scaling what exactly we do. So, as I said, the dynamic power is the square of the v dd and it is proportional to clock frequency. Let us assume that and we have we already discuss this trade off delay and power. So, it is a tradeoff between power and speed. Imagine we have a task and the task is can be executed, it has to be executed within the deadline.

So, if we use v dd1 the task can be finished in short time, but as I said if you use smaller I mean higher v dd then the effective utilizations of the processor is low and if such computation happen more frequently than your v d square increases. So, dynamic power increases.

Another possibility you reduce v dd to a lower level in such a way such that you do not miss the deadline you finish the task and there you can save the dynamic power by reducing the voltage. But if you further reduce then it will mean the deadline, then your whole purpose is lost because we cannot miss the deadline that is our limit.

So, this technique can this provides us that means, using a variable voltage V dd you know we are talking about a variable V dd enable us to optimize performance and efficiency. That means we can we do not want to sacrifice the per deadline definitely if you reduce V dd your performance will come down, but if it is within the deadline that is fine, but we can increase the efficiency.

Energy efficiency because it is the energy area under the curve; that means power into time is the energy and each task requires certain energy and if you can do that, we can save power so that your thermal overhead can be reduced, heat dissipation will be reduced then board space and power can be reduced. So, it could save in many ways.

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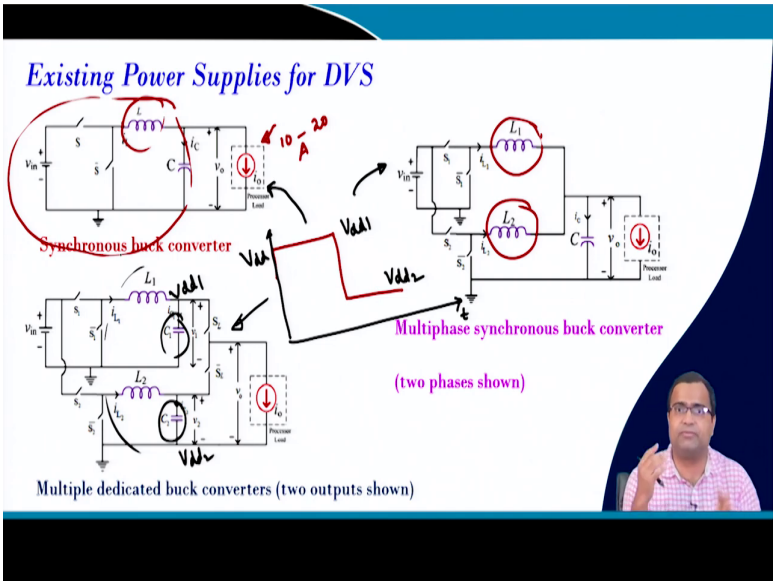

Now, we want to find what are the existing method. So, the simplest example is a synchronous buck converter, simple normal buck converter where it is supplying to a processor right. So, this is a very standard one. If the current requirement of this processor is low, let us say it is like 10 to 20 ampere kind of rating, a simple buck converter should be sufficient.

But if the current rating of these increases or even beyond 10 ampere some in some cases in some product people go for two-phase converter. So, here I am just showing two phase converter. But if the current goes above 20 ampere then natural choice is you have to go multiphase because we need to divide the current among various phases.

Because we should not use high current for an inductor because that will have a lot of losses and if we want to search for a higher current rating inductor than the cost of the inductor will go up and also the losses will go up. So, it is better to divide the inductor so, that they can share correct that is also another practice.

The third one we will see the dedicated different decent converter because suppose we need a V dd1 suddenly we need another V dd like this. So, if we consider you know this is my this is my time and this is my V dd ok. So, this is my V dd1 this is V dd2 and so on. So, we want to change different V dd level.

So, you have to do either by this converter and we will show you there are challenges. We can also do by this converter, but we can also do by this converter when V dd1 is sitting here and V dd2 is sitting here V dd2. So, two dedicated DC-DC converters and the processor can be connected to at a time one of them. So, you can change v dd1 and this will be very fast, but you know this is a very very you know number of inductors are needed more capacitor. So, it is a bulky solution may not be a very practically recommended.

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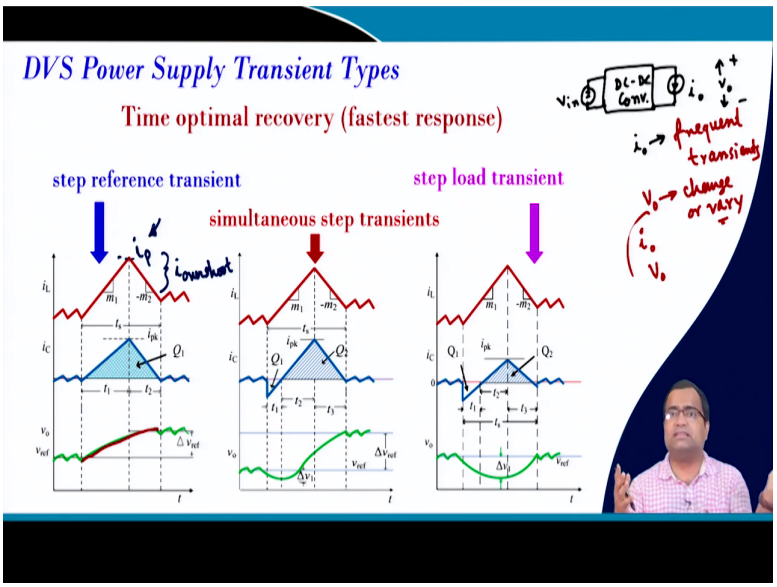

But before I move forward, we need to first understand what are the different type of transient in dynamic voltage scaling because you know as usual when a DC-DC converter is supplied a DC-DC converter a supply to a processor load; that means, here a processor load we have a supply here V in.

Then, in case of dynamic voltage scaling, first of all, for any case, the processor current will change it there will be frequent transient. Let us say there will be frequent transient that this is related to load transient because this transient happened due to the computational requirement that is going to check and that is something it is common very common.

But in addition to that in V dd we need to change V dd change it or vary or vary. Why? Because we discuss if you want to reduce the dynamic power we need to change V dd. So that means, we can expect transient in i 0 that is my load transient, we can expect the transient in reference voltage that is for reference voltage transient or their combination.

So, if we take the time optimal recovery because we discussed in the previous section we want to achieve the fastest response and which we can use a switching control scheme and in fact, we have discussed the large signal based controller tuning can be used to achieve this kind of response and that will get the fastest response.

We can also achieve that same tuning role, but maybe at different gain parameter. The fastest response for the reference voltage change when it is changing from 1 voltage to the other voltage using fastest time and the other possibility you can have a combination of load and reference transient. So, all these three possibilities exist and we want to now analyze what are the parameter and how are you going to design the power stage.

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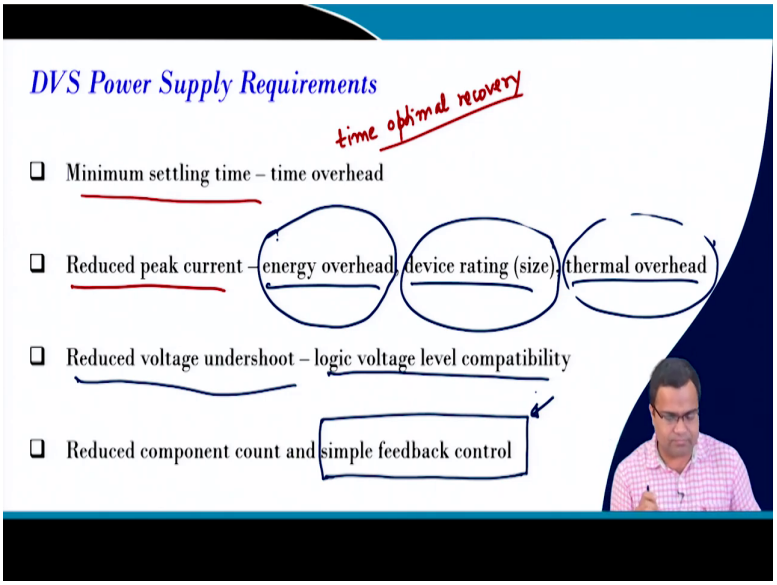

So, the DVS power supply requirement we need a minimum settling time or basically minimum recovery time and that is why we talk about time optimal control, time optimal recovery that will reduce because the linear control cannot meet that, right? Then, we also want to reduce the peak current because if the peak current during the transient if you go back to this, so, to the peak current, generally we determine this current, this is my peak current right.

So, with respect to the next operating point, what is my or I will say not peak current? I think the overshoot. This is not the peak current, the peak current is absolutely this one, this is my peak current ok, this is my peak current and this particular part is my current overshoot.

So, I am concerned about the peak current because this is this there is a limit due to the inductor because inductor cannot carry arbitrary current and even if we talk about the b h characteristic of the inductor, so, we should not go into the non-linear region or the saturation region. So, that also we have to check carefully.

So, the peak current and if we can, that is for the inductor point of view, but in general, if the peak current is high, then your energy overhead can increase and that we will discuss. The device rating that is the inductor rating as well as switch rating has to increase and also there can be more thermal overhead can be increased.

Reduce: so, if we can reduce the peak current, then we can reduce both energy overhead; that means, we can reduce the rating of the device inductor size. You know the rating of the inductor that coil or basically you know gauge rating of the inductor that can be reduced. Then thermal overhead can be reduced heating effect. So, we can save the space both space.

We can read we have to reduce the voltage undershoot because this is supplying to a digital processor where there will be a noise margin. So, we cannot exceed the noise margin. So, the logic level compatibility has to be made. And first we need to reduce the component count and the control should be simple feedback control.

And this path I think we have discussed that if we use our large signal tuning using a simple current mode control, that is a very simple technique that is used in many commercial products. By setting this controller tuning, you can get the fastest response. So, though digital control allows us to do very high performance control, but we want to make our control simple because ultimately it will be translated into silicon area and the price.

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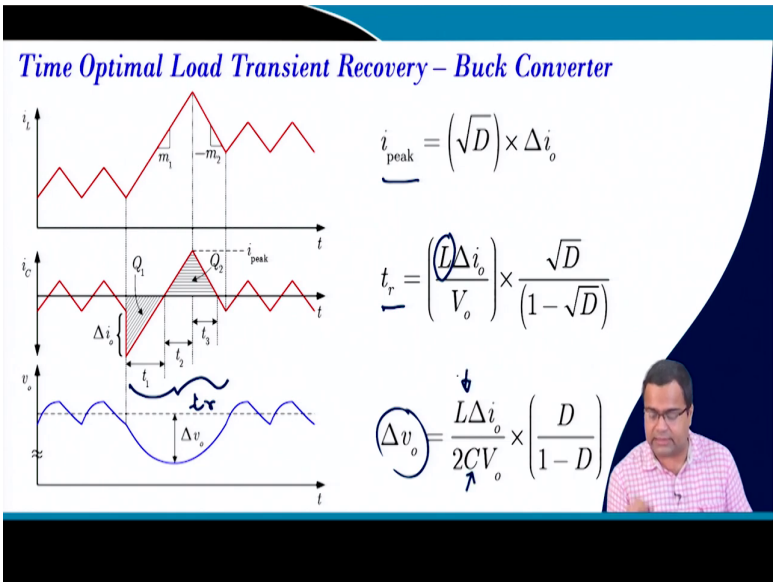

So, the time optimal recovery if we take a buck converter, then we are talking about the fastest transient, and that we have discussed already. We already have identified what is my peak current, we have already identified what is my recovery time. So, this time is my recovery time t r that we have already discussed and then we have also discussed the voltage undershoot, all the expressions we have already discussed.

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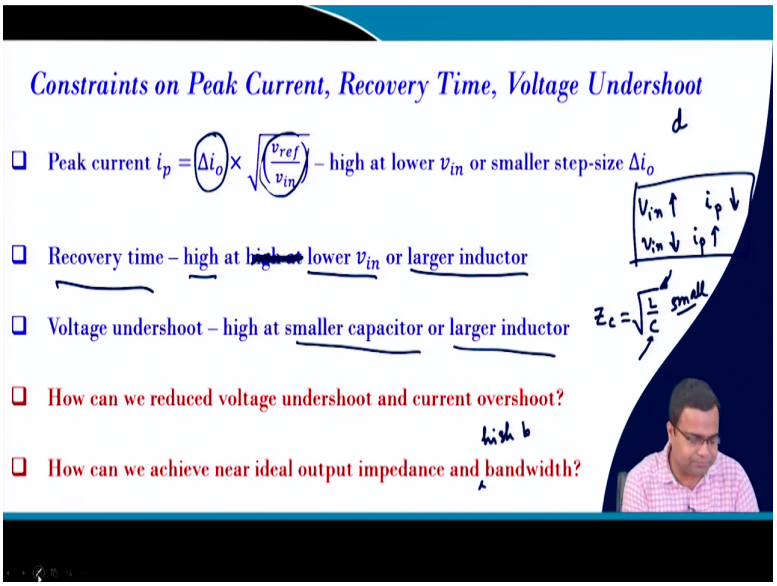

Now, what are the constraints on the peak current, recovery time, and the voltage undershoot? So, the peak current you find it is basically delta i 0 that we depend on the step size and

which is quite common, but it also depends on the square root of v ref by v in. So that means, if the input voltage increases, then your peak current decreases because this is in the denominator. But if the input voltage decreases, then the peak current increases. That means, if you operate at a lower input voltage, your peak current can significantly increase.

But if you operate a high input voltage, then there is a problem because the duty ratio will be smaller and we have found in you know in the very first or second week that high lower duty ratio will lead to higher losses because the RMS current will increase and also higher input voltage can affect the switching loss, it can increase the switching loss.

So, the losses in the converter will increase when we operated a high input voltage. So, another thing, the input voltages in most of the cases is not in our hand unless you use a two stage architecture. So that means our peak current is limited by this. Recovery time if we go to it is high at high input voltage and large inductor.

So, recovery time if you go if the duty ratio decreases then yeah recovery time actually it should be the other way around recovery time high at higher input voltage or the lower duty ratio no high at ok. So, there is a typo. So, high at lower input voltage or this can be larger inductor if the inductor value is large then recovery time also increases. So that means the recovery time high at lower input voltage or larger inductor value.

Then voltage undershoot high at smaller capacitor or larger inductor because if you go that go back voltage undershoot increases if you reduce the capacitor value or increase the inductor value. So, natural choice is that we should take the characteristic impedance. That is why in most of the power supply design we take L by C to be very, very small; that means, our inductor is small and capacitor is large.

But how can we reduce voltage undershoot and current overshoot even for a given inductor capacitor value? Because we cannot increase the capacitor value significantly because there is a penalty in the power density, we cannot decrease the inductor value significantly because there is a penalty in terms of r m S current right the losses.

So, can we increase without affecting the power stage or without can we achieve near ideal voltage regulator without very less output impedance and very low bandwidth a very highly high bandwidth high bandwidth high bandwidth? That means ideal, almost ideal output impedance and bandwidth. So, what is the ideal output impedance?.

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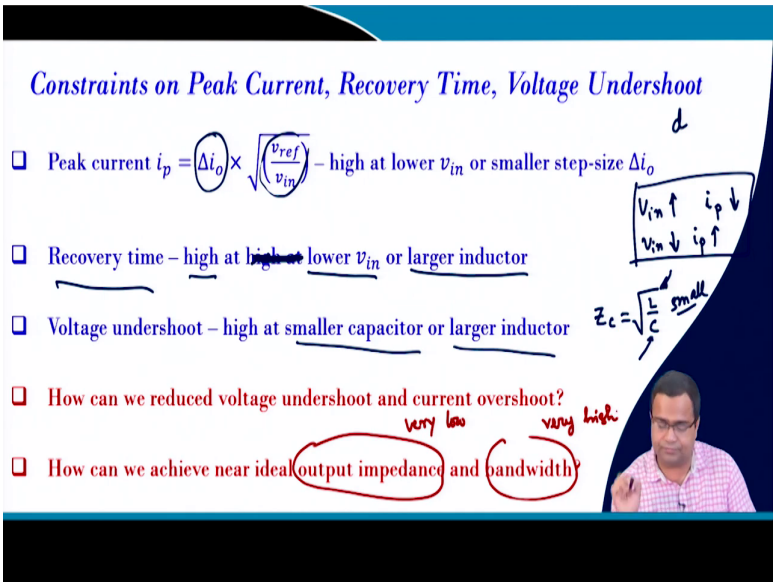

That means we have learned the ideal output impedance should be very low. In fact, negligibly low and this should be very high, very high, extremely high. It should be very high ok.

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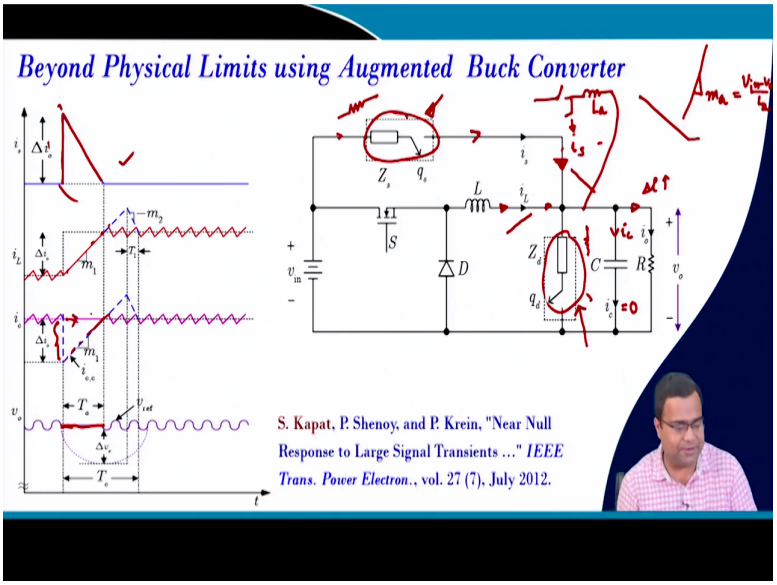

Then we have to go. We need to make some circuit rearrangement, otherwise it is not possible. So, during the load step up transient, we need to provide an extra path because what happens? During the step up process, suppose you know if you take the dash line your

capacitor current sees. When there is a load step transient, the whole step size appears across the capacitor current.

Because your inductor cannot change immediately because it has an inertia and it undergoes a load step transient of delta t it has increased. So, this step size will appear in the capacitor current and that is we are getting. And it takes time that current to capacitor current to become positive, but till then, your voltage will fall and that is the problem of voltage undershoot. So, it is bound to happen.

But what happen if we can anticipate by providing an external current that means, we are giving a current here from the source that is my source current in such a way in case of perfect anticipation in such a way that when there is a load step transient the whole step size will appear and then it will slowly decrease in such a way the capacitor current becomes 0.

That means, we want this capacitor current to be 0 during the large recovery so that the load step transient, whatever is happening it will be anticipated by this external current and since the inductor current is rising. So, this has to fall. So, that at some point inductor will take it up when it reach to the next steady state point and this current will slowly become 0; that means, it start decreasing and it becomes 0 and this is exactly what is happening.

And if you can do that, then you will find the capacitor current remain 0. So, there is no change in the output voltage, almost negligible change. And if you can do that, then I can we can say the output voltage is not changing at all or inductor is changing, but that it is not affecting the output impedance.

So, since there is no variation in the output voltage. So, we can assume that it has 0 output impedance as well as it has infinite bandwidth because it is not changing at all. But this is a practical converter. This is achievable if we can anticipate by this current, but what is this circuit? What is this circuit that itself is a question.

Because it is like a variable source and it is not so simple and it will also come with a price because we are adding extra component. So, the price will go up. And so, what we did in this paper we have used a resistive one like augmented path and if we same thing can happen during step down. That means, here we are providing this extra current through source to get something similar by using multiple resistance.

Similarly, during step down transient, we can anticipate by excess charge in the capacitor has to be removed and that can be dissipated by the resistance. As it said that since it is a resistive component, so, the power will be dissipated as a heat energy and that is the fallacy. But there are many other techniques where you know this can be replaced by another auxiliary inductor. That means you can use another branch of converter like these small branches with auxiliary inductor and that can be connected here, but this inductor can be very small.

In fact, in many multiphase solution these auxiliary phases are used to boost the performance is kind of booster operation where we can speed up the response by introducing an auxiliary phase where the slope is very fast. So, the current can be increased rapidly because the slope of the current depends on auxiliary phase. it is V in minus V 0 by L a, where L a is very small. So, we can speed up by providing this excess current.

So, ultimate objective get something similar ideally if we can achieve 0 capacitor current, but practically it is not possible. So, there are multiple circuits which can achieve some which can offer some practical solution. So, one of them is a resistive one, but this will be lossy if the transient happens more and more frequently.

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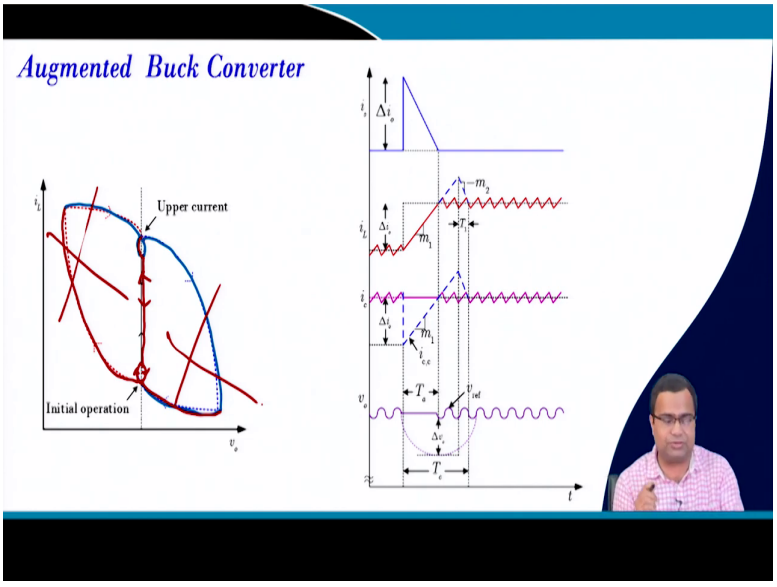

So, this converter we want to get the phase plane behaviour because you know we have discussed if this is my one steady state operation and when there is a load step up transient it goes like this, then it hit and it come back to the next operating point and stays there ok. So,

this is a first low state of transient. During step down, it is again coming here hitting and turning off right.

So, the turnoff, I would say, this is turning on, this is turning on. So, different color and this is the turning on path. So, here also if we can provide this auxiliary path from one point to the other point, it will simply go like this or it will simply come like this. So, there will be no overshoot undershoot and this path can be discarded if we can make that ideal arrangement. There is no problem, but practically it is not possible. So, what we have to do? We have to find out the solution.

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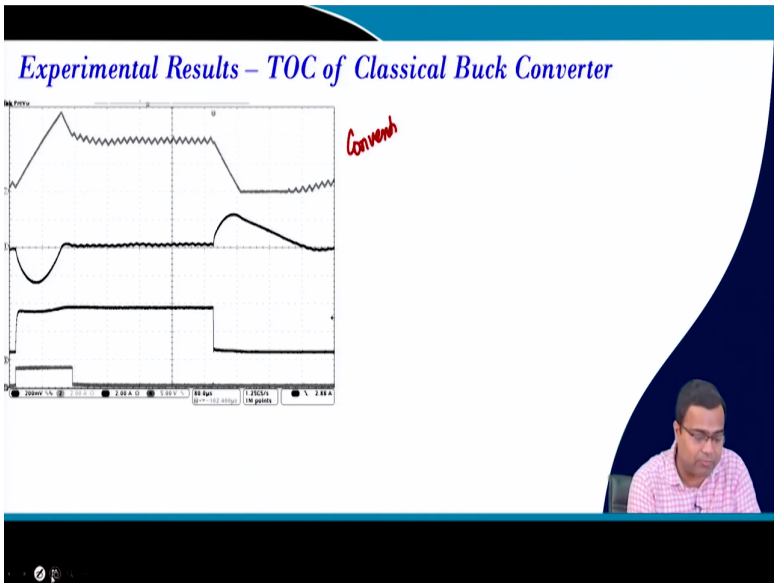

So, one of the way we told that we use a resistive network ok. And this is the time for optimal recovery of a conventional buck converter. So, this is like a conventional buck converter or I will say a classical buck converter, which is given where we are using a diode. So, we are using a diode base converter.

And you see, when there is a load step up transient, the inductor current is going from one point to the other point in time optimal recovery. There is no problem. And when it is coming from this point to this point, it is also a kind of time optimal.

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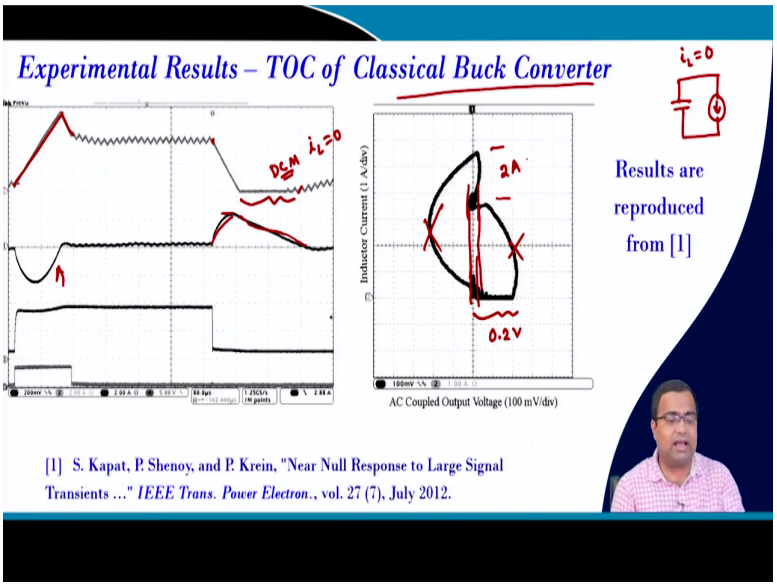

But because this particular phase, it is in DCM mode discontinuous current when the inductor current become 0, when i L is 0. So, as a result your capacitor is simply discharging across the load across the load during this you know when i L equal to 0. And since the load current is low, the rate of discharge is very slow and it is taking lot of time ok and there is a huge overshoot.

And this undershoot overshoot may not be acceptable in the future processor requirement where we are talking about cloud computing there can be hundreds of ampere load step and such high load step can result into large overshoot undershoot and that simply by power stage design and time optimal control it may not be enough. So, we need to think about some auxiliary circuit to cut down the transient. So, this is a time for optimal recovery. Again, these results are taken from this paper which we have presented.

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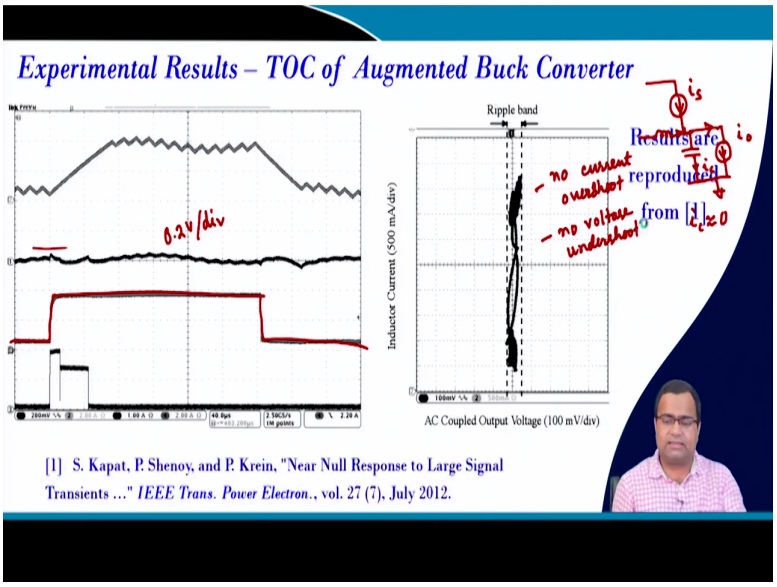

Now, if we consider the auxiliary path, suppose during the step up transient again, the load current increases here. But now we have enabled the auxiliary path and auxiliary path, we have used two resistances with switches and during that time the capacitor current is supplied or basically you know what it is happening; that means we have this i S current which is coming from the source through the resistive path. And it is getting added. This is my inductor, this is my capacitor, and this is my load ok.

So, this capacitor current since this source current is directly providing to the load, this is my load and inductor current is ramping up. So, the capacitor current changes negligibly. It remains nearly equal to 0. As a result, you can see there is an insignificant change in the output voltage ripple and this is AC couple result because this is 0.2 volt per division. And the ripple band, this is almost negligible change, and we found that the deviation in the output voltage is constant within the ripple band.

That means we have cut down the whole trajectory, which was there. You can see that there was a such high overshoot undershoot, and this is my ripple band, this is my ripple band ok. So, I want to cut down on the transient. I want to keep my voltage and current within the ripple band and I want to cut down this transient ok. So, this is possible through this augmented path and there is no transient.

Same thing. So, these results again are taken from taken from this paper where we have presented for detail and then there are subsequent methods are developed. But in this course

we want to just emphasize some aspect which will motivate to think that how can you develop an auxiliary circuit.

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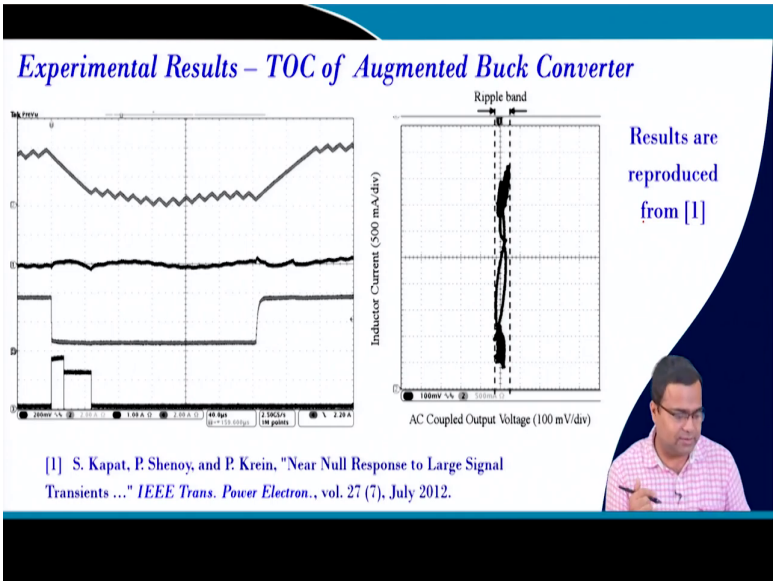

If you take the step down transient that is one of the problematic case and if you go here, you will find in the step down transient this undershoot of voltage undershoot was you know is AC couple around 0.2 volt 0.2 volt per division right sorry 0.2 volt is the magnitude 0.2 volt.

And the current overshoot in this case, in this case also the current overshoot was how much it is like a 1 ampere. So, it is roughly around close to 2 ampere right. So, here in this case, there is no current overshoot. So, no current overshoot, no current overshoot and no voltage undershoot ok. So, it is almost like an ideal converter.

Same thing happens for you know our step down. It is almost within the ripple band. So that means it is possible to cut down the transient by means of circuit configuration where we need to change it, but this method that we have used it is long back. It is a resistive method that can be lossy. If such transient comes more frequently, then you may have losses in the converter and those aspects are also discussed in this paper. But subsequently there are many methods are developed to cut down transient without penalizing too much of the efficiency ok.

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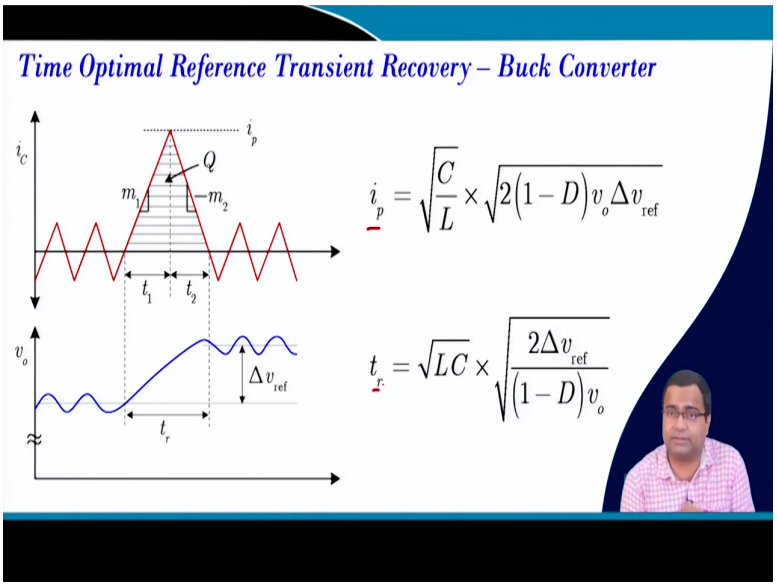

Now the time for optimal reference transient recovery. So, we talk about load transient recovery, now we are talking about reference transient recovery in reference transient you have a peak current and here the voltage has to change from v v ref to v ref plus delta v ref and we have discussed the peak current recovery time these two are the parameter that we are going to discuss.

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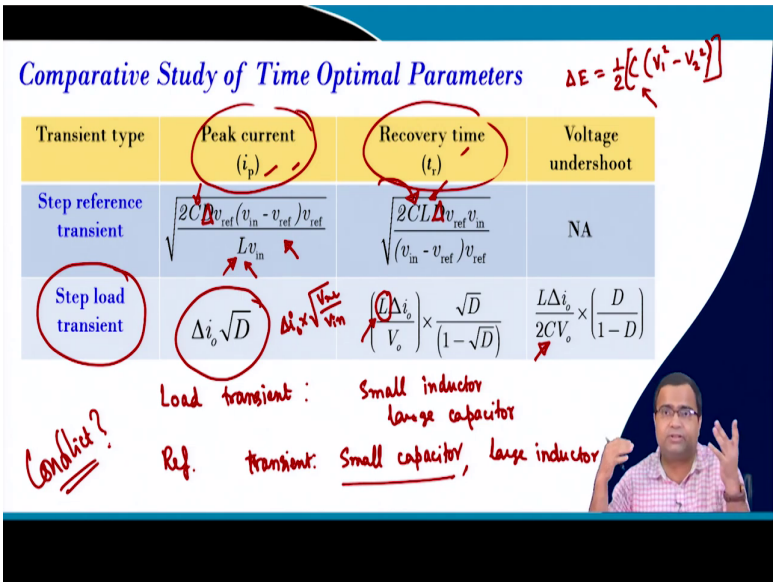

And if you compare the time optimal parameter, if you take the load step transient, we saw the peak current is basically delta i 0 D where it was like a delta i 0 into reference; that

means, ref by V in right and you saw at higher input voltage it was low, but lower volt voltage it was very high.

But if you take the peak current for the reference transient, you see it is a function of capacitor; it is a function of inductor; it is a function of you know there should be delta D actually delta D. So, this should be delta v ref this should be delta v ref sorry delta v ref. So, this reference voltage ok.

So, here this load step that means what does it indicate reference transient? If my for a given low reference step size if my inductor decreases, then the peak current increases. If the capacitor increases, the peak current increases and if we reduce capacitor peak current can be reduced if you increase the inductor peak current can be decreased.

But if you go to the recovery time for the load step transient, you see the smaller inductor achieve faster recovery that we have discussed, but of course, it has a penalty in terms of higher conduction loss, but that also has to decide. So, in the power stage design, we generally tend to design smaller inductor.

But here also recovery time using a smaller inductor you can reduce the recovery time, but you see it increases the peak current. So, smaller inductor increases peak current for reference transient. Similarly, if you go to the voltage undershoot generally for load transient, we use a larger capacitor to reduce the undershoot, but this is something opposite requirement for reference transient because a larger capacitor will increase the recovery time and larger capacitor will increase the peak current.

Because in reference transient we know that half C, you know what do we say V 1 square minus V 2 square. That means, if we use a larger capacitor to change voltage from V 1 to V 2 you need more energy from the source. If the capacitor increases, this energy requirement goes high as a result. Peak current increases and the recovery time increases.

So, in load transient for load transient load transient we generally need a small inductor and large capacitor. But, for reference transient for reference transient we need a small cap and we also need the inductor choice is also conflicting because if you take a large inductor peak current will deduce, but your recovery time will increase ok.

And the peak time will peak current will give you energy overhead and the recovery time will give you time overhead. So, it is a conflict right. Small capacitor is mandatory, but that is conflicting and even if you take a large inductor, you can reduce the peak current, but you will end up with longer recovery time. So, there is a conflict. In the fastest design, when we want to simultaneously we want to design the converter, which has to cater the first recovery for load transient as well as the reference transient.

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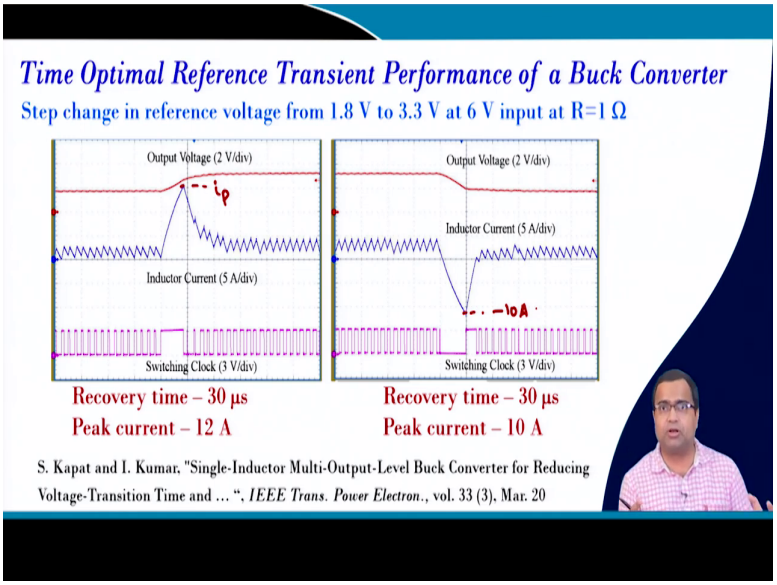

So, the time optimal performance if I show a result that has taken from this and it is given in this paper that if we want to change the voltage from 1.8 to 3.3 volt you can see it takes a longer duration right. So, it is 30, it is taking almost 30 microsecond and with a high peak current, the peak current is very high, this peak current is very high.

So, this peak current is very high. This is my peak current very high around 12 ampere and here the peak current is minus 10 ampere very high peak current ok. So, the regular converter when like a normal buck converter which we have designed earlier using load transient for small L, large C. This is detrimental for reference transient because we saw that there is a conflict.

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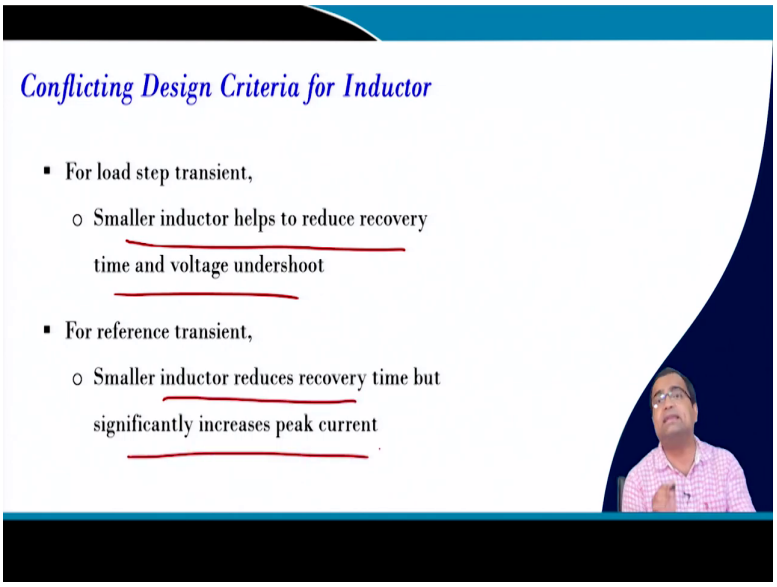

So, the design conflict for the inductor load step transient we need a smaller inductor for faster recovery and lower voltage undershoot for reference transient small inductor reduces recovery time, but it significantly increases a peak current that is what we saw.

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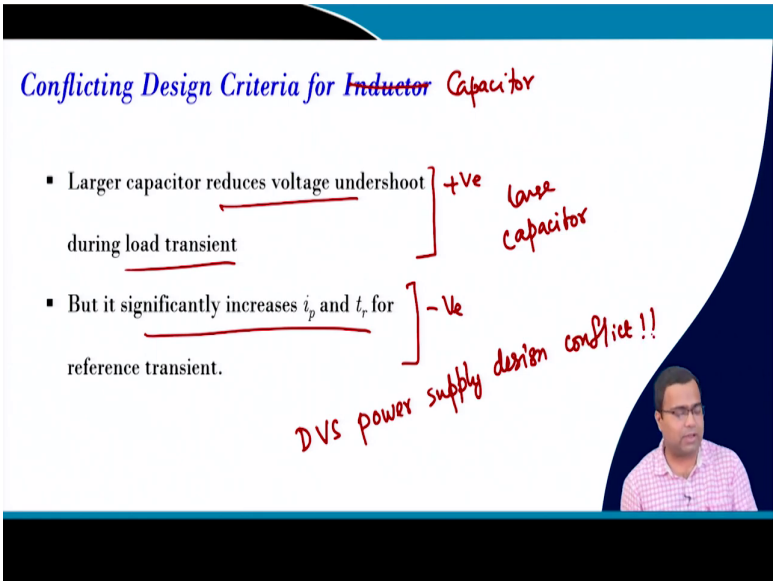

If we take the capacitor; that means this should be capacitor if we take the capacitor larger capacitor reduces the voltage undershoot during load transient. So, it is the good positive part for load transient, but it significantly increases both peak current and the recovery time for

reference transient. So, the large cap, you know if you take large capacitor and that makes the DVS power supply design. DVS power supply make design conflict.

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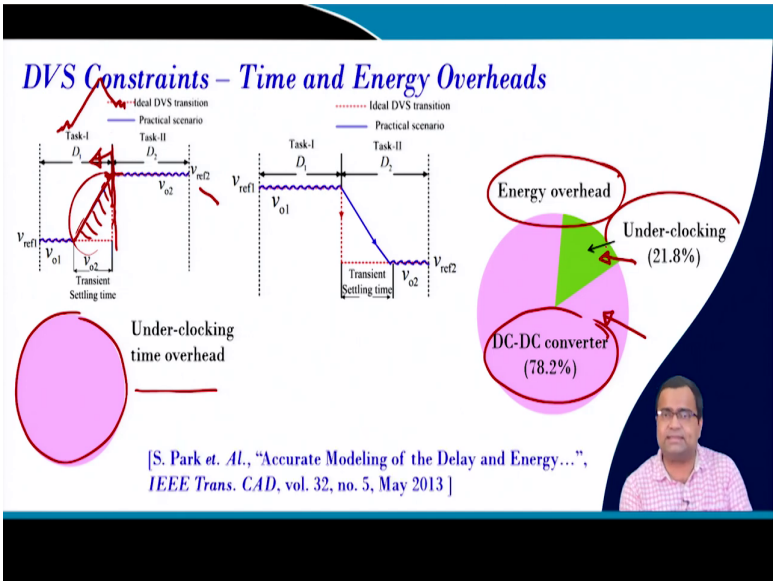

And because of this conflict, you know if we want to you know because if you go to various processors like Intel, Qualcomm, other processor the reference voltage has, we have to change from one to the other. So, in reality, the kind of converter is used. It takes time to reach from 1 voltage to the other voltage. It may not be obvious or immediate and that increases.

And that basically the recovery time gives rise to first of all time overhead under locking; that means, our required voltage is here. Because this voltage can be, let us say it is can be the voltage of the processor or it can be the voltage of a ring oscillator which generates the clock. But if we if it takes time, then you require more time before you actually start activating the ring oscillator locking.

Because in between the voltage is changing and you may not be able to correctly predict the actual frequency coming out of the ring oscillator because of this voltage transition. So, the under clocking time overhead is quite large, and it is mainly occupying the whole time is taken almost by the under clocking time; that means, when it is voltage, is transition.

But if you talk about energy overhead; that means, I told you so, there will be high peak current. During this time, your peak current will be significantly higher right inductor peak

current. So, it will undergo high energy overhead and it is primarily because of the DC-DC converter. It almost close to 78 percent is occupied.

And this voltage, also under clocking behaviour of this voltage, also creates energy overhead because this we are using excessive you know lower voltage. So, as if you cannot use the actual P LL before this; that means, before this as if we are using an earlier frequency, but using extra voltage. So, the frequency deviation.

So, we need to take care that P LL how to you know this transient time the voltage rising time will actually give an under clocking behaviour where the voltage is not perfectly locked. So, it will give rise to energy overhead. And this is discussed in detail in this paper.

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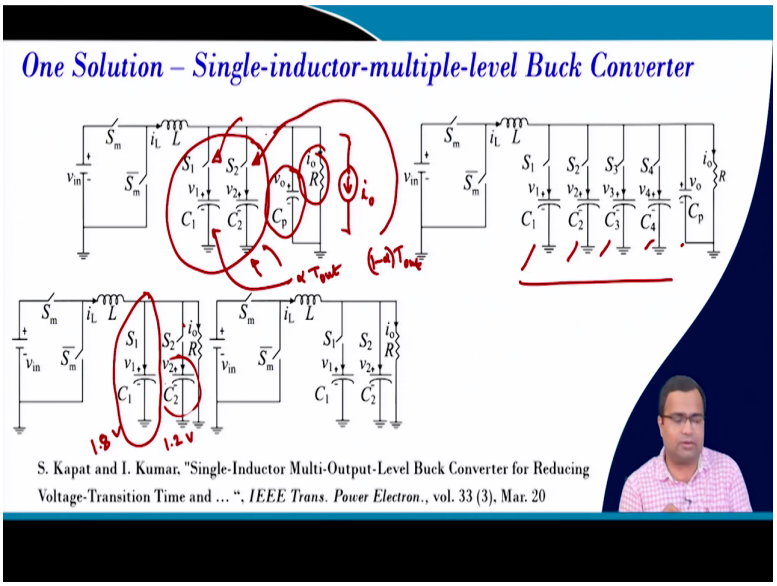

So, one solution how to cut down because we found the problem load transient and reference transient has some conflict in the design. So, one of the solution we take you know one inductor and two pre charge capacitor two pre charge capacitors. And at any point, suppose you want to change from one voltage to the other voltage. Suppose you use this capacitor as your output can and let us say this is sitting at 1.8 volt and let us say this is pre charged to 1.2 volt.

So, we can change between 1.8 and 1.2 very frequently; that means, you know we can increase the number of capacitor if the number of voltage levels are required right. So, here it is showing the two capacitor case where you can change the voltage from v 1 to v 2. This

parasitic capacitor is very, very small very, very small, but this is your load, generally this is your processor load i 0 and this will be connected either to this v 1 terminal or to this v 2 terminal at a time only one terminal should be used. So, you can change either 1.8 volt or 1.2 volt and that will happen almost immediately.

And if we require such number of voltage level, so, you can increase the number of capacitor right, but there is a penalty. Because more capacitor so, if you need let us say 100 number of such voltage level to optimize my DVS power consumption, then should I need a 100 number of capacitor? No.

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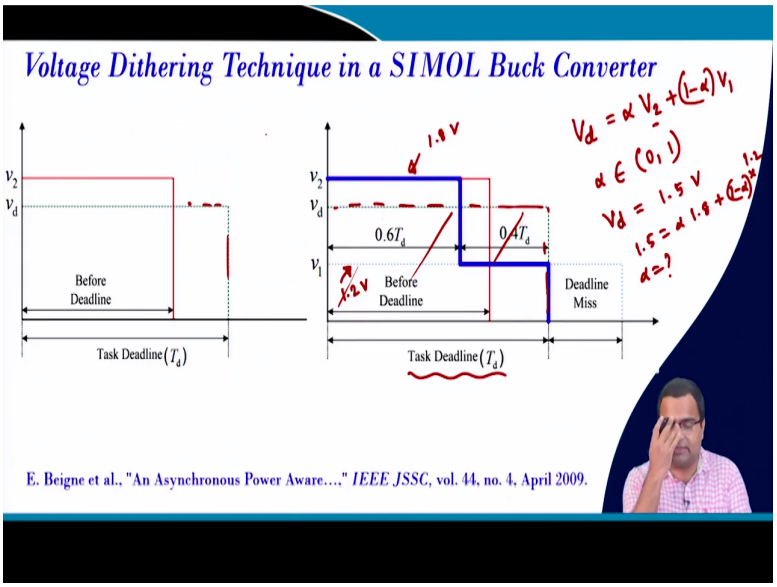

So, we can use a voltage dithering technique; that means, if my required voltage in the deadline is my dotted line right then I can use a higher voltage to finish early, but that I said that it is not a good way. So, you will lose more power than I can take two different voltages. Suppose I have two voltages are available. So, one voltage is my v 2 as I said maybe at 1.8 volt and other voltage is my v 1.

This is my v 1 which is let us say 1.2 volt. So, my effective voltage requirement v d which is this and this we have to finish within the deadline. So, if we use v d then our task will finish within T d time. That is my deadline, but ultimately it is an energy. So that means we are talking about the v d in T d. This area under the curve has to be same. So, this V d can be generated by alpha times V 2 plus 1 minus alpha time V 1 where alpha belongs to you know

0 to 1 and this alpha is a fraction of time when V 2 is 1, V 1 is 1 ok and that means, it will be decided.

So, suppose if my V d requirement is let us say I need something 1.5 volt and my V 2 is 1.58. So, what I am getting? 1. So, if I put it here, 1.5 is equal to alpha of 1.8 plus 1 minus alpha of 1.2. If you solve it then you can find out alpha. So, how long duration it can run? That means here only two capacitors that we have discussed. These two capacitors are enough, but we need to change it from 1.8 to 1.2 for alpha into T time and which we call duty ratio, but we are not saying duty ratio because it is not operating at the switching frequency. So, it is an output frequency which has to be changed.

And alpha into T times we will use for this terminal and 1 minus alpha into T out we will use for this terminal ok. They will interchange and this is some voltage dithering technique can be used.

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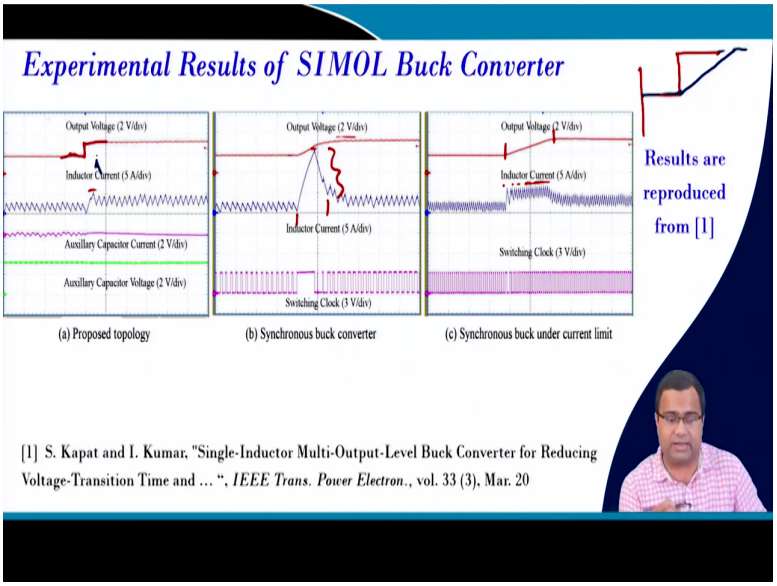

And since our technique support very fast transient response because you see here we are using the same design criteria of a load transient response smaller inductor larger capacitor. So, we can change the voltage level from this to this almost immediately, whereas, in a regular buck converter, it require large amount of time and these results are taken. this paper it is discussed. So, your time recovery is much larger and here it is like almost instant.

Secondly, you see the current overshoot is much higher. Here the current overshoot is almost cut down, there is no current overshoot. Now in conventional converter, if we want to put a current limit because there is a limit in the inductor because we are using a peak current mode control then naturally this recovery time increases time overhead increases the recovery time increases and that is something not acceptable.

And if the recovery time increases, then your processor power supply; that means, you want. This is the ideal processor power supply requirement, but it is actually changing like very slowly from this part to this part. So, your uncertainty will increase further because it is taking longer duration to reach from one voltage to other voltage, but here you can make it almost immediately without any current overshoot.

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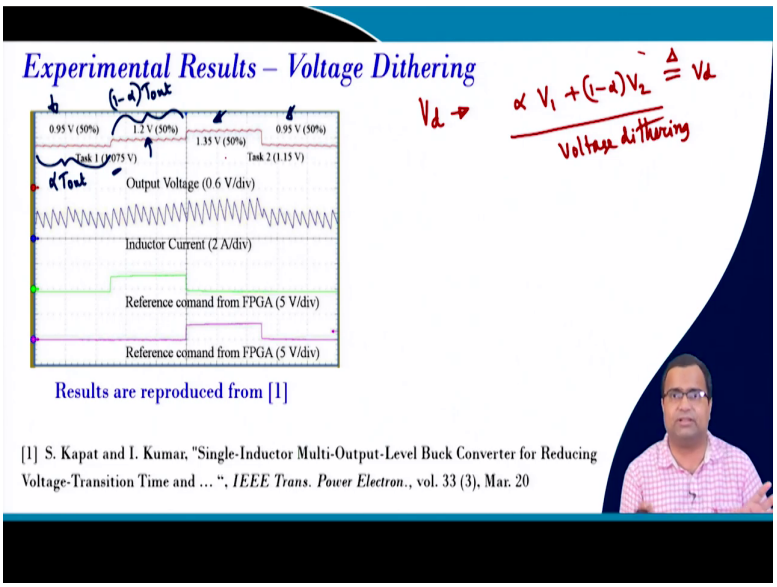

So, the voltage dithering technique that we have shown that if we change the voltage from 0.95 to 1.2, 1.35, 0.95 you can see there is no current overshoot undershoot in this method and it can change immediately because we have taken four different here three different voltage level we are switching.

And in the first case, we are switching between two voltage level alpha time T out. This is this duration I would say ok. So, here you can think of alpha time T out and here you can think of 1 minus alpha time T out. So, this is used to achieve the desired voltage of 1.075 ok. By changing this available voltage 0.95 and 1.25 we can achieve that.

Another task we can achieve by using 1.35 and 0.95 ok. So, you do not need too much of a capacitor in the architecture, you can reduce it and by that way we can achieve any voltage level using this voltage dithering technique and there is no current overshoot. So, this can this reduce significantly.

That means, so, what is the ultimate requirement? We need certain V d that is our desired voltage, but this can be achieved by alpha times our alpha times 1 voltage plus 1 minus alpha time V 2 voltage and by means of voltage dithering. And we can execute the task and this will be equal to equivalent to our V d, the task can be executed. And since our technique actually cut down all the transient, it can reach immediately this voltage, we cannot change it.

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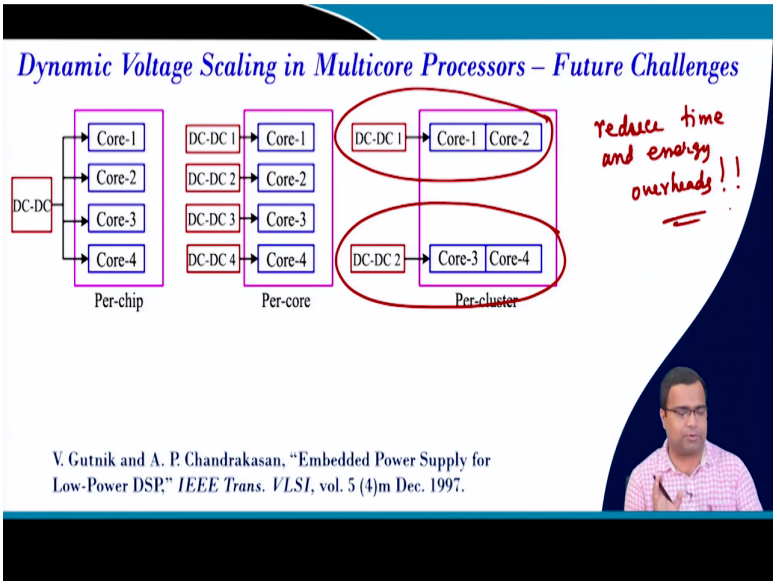

But still you know still we are using the number of capacitor because even if you use two capacitors more switches more capacitor. So, this can be reduced significantly in the multiphase of that multi core processor because that can be challenging. In multi core, if we want to optimize, you know, let us say cluster based approach and this cluster based approach, so, what should be the right strategy to do that. That is also another challenge. Because the future is going, you know it is already in multi core.

So, we can do DVS, but the technique that we have told it should not be scaled directly for multiphase. Then you have too much of capacitor requirement. So, there are scope for optimization for multiphase and that will motivate to come up with new and new architecture

where we can reduce time and energy overhead. So, those are that are the objective for future and in multi core it is interesting to see how it will happen ok.

So, I am not going to discuss in this lecture, but we have developed this, and we a filed a patent, but this technique I mean for multi core there are several challenges and future that can be a very good future research problem.

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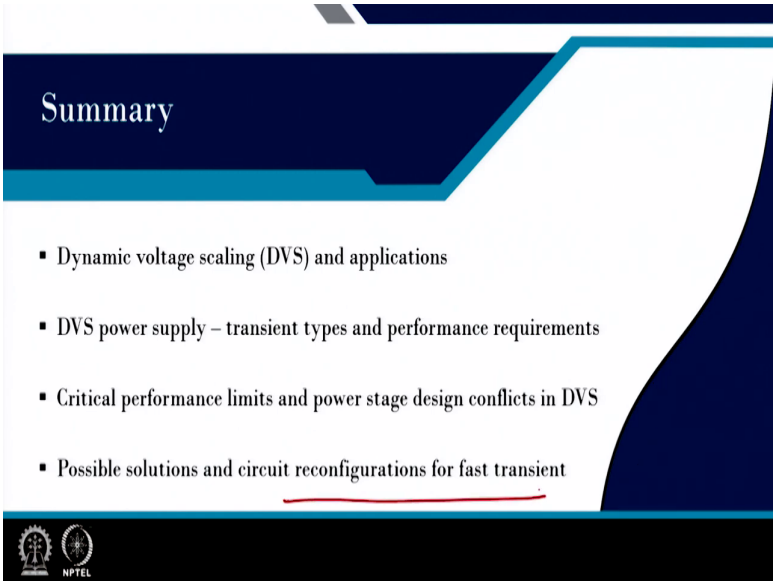

So, in summary, we talked about dynamic voltage scaling and application. We talked about dynamic power supply, DVS power supply transient type, performance requirement. We talked about critical performance limit and power design power stage design conflict and then we also talked about some possible solution and circuit configuration for fast transient, but there are still scope for further optimization and that actually kind of motivates us for future research. So, with this I want to finish it here.

Thank you very much.