**Digital Electronic Circuits**
**Prof. Goutam Saha**
**Department of E & E C Engineering**
**Indian Institute of Technology, Kharagpur**

**Lecture - 58**
**Dynamic RAM (DRAM) and Memory Expansion**

Hello everybody. We are discussing Memory. In the last class we looked at static RAM, in today's class we shall look at dynamic RAM, and after that we shall discuss how memory expansion is possible by using multiple memory blocks, ok.

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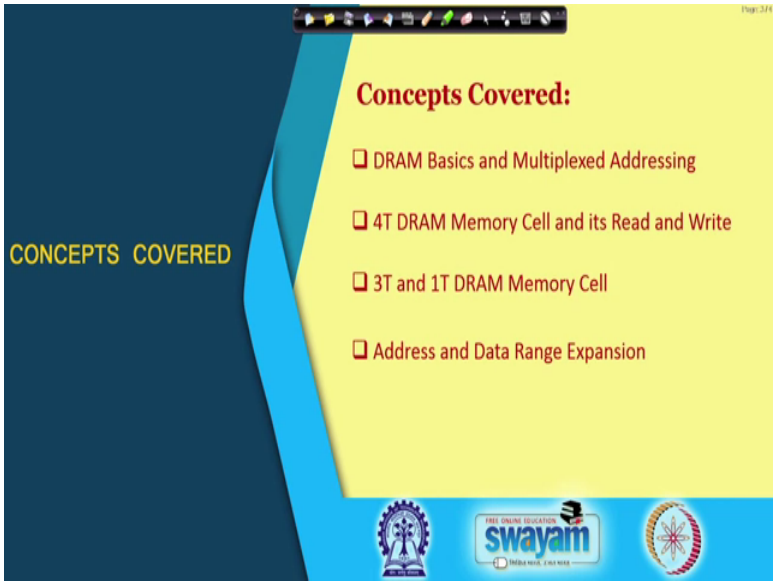


So, we will start from DRAM dynamic RAM basics and since the number of memory cell that can put into a DRAM memory unit is quite large the packing density is higher, so the number of address line will be a bit more for which to save pins we can utilize multiplexed addressing that part we shall see. Then we shall look at memory cell by 4 transistor, 3 transistor and 1 transistor and at the end we shall look at address and data range expansion, right.

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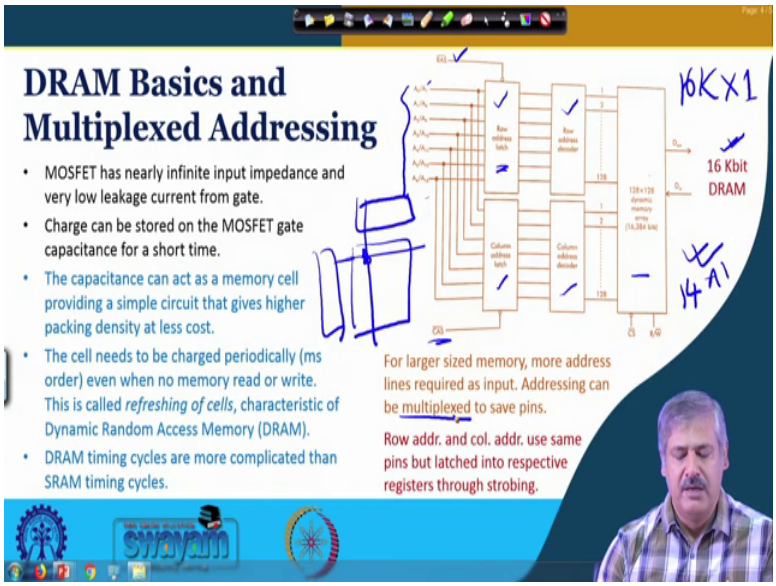


So, what we use in design of dynamic RAM based memory cell, is that the MOSFET by nature has infinite input impedance that we all know, ok, because it is a field effect device it is not a current controlled device like BJT, right. So, the leakage current at the gate is very small so the parasitic capacitance that would be there at the gate of the MOSFET that can be used to store charge for a short time. Of course, there will be small leakage; but for a short time it can be stored and that can be used for storing binary information, ok.

So, this capacitance acts as a memory cell and this provides us a simple circuit and a higher packing density, number of parts required becomes less, and the cost also per unit memory cell becomes much much smaller. So, this is the strength of this approach. Of course, as we see in any design there is always a tradeoff, the tradeoff is that what we just noted that the capacitance though the leakage is you know these can be is relatively small, but still it leaks. So, it requires periodic refreshing, otherwise the sanity of the data the data that is there will not be properly you know understood, when it is a 1 or a 0, because the level will become similar. So, that is one particular thing and this is called refreshing of cells.

So, periodically of the order of millisecond it need to be refreshed. Even when memory read or write operation is not taking place so that previous value whatever it is remain stored. This is one specific characteristics of DRAM, which was not there in SRAM for

which the memory cycles that are there the timing cycles for memory read write operation becomes little bit different, I mean some more complicated compare to SRAM.

Now, as I was telling that it has, it can pack large number of memory units, memory cells in one particular block, because of the simple nature of the circuit. So, you can expect that for a particular memory cell; the number of address pins will be quite large, because the it is what about the number of memory cell; log of that to the base 2 is the number of address pins address bits address lines that would be required. So, when it becomes higher, then the number of pins required to access the memory also becomes larger.

Now, this additional pins that requires higher cost. So, for which the concept that we can use in some such devices is the multiplexing of address lines. So, here you can see one such example, one such example where we are trying to address 16K into 1, that kind of memory block. So, this is that kind of memory block, right. So, 16K means you need 14 address you know pins, 14 address lines, 14 bit address.

So, in this arrangement what you can see that A naught to A 6 these 7, and A 7 to A 13 there is a stroke over there; both are fed through same set of 7 pins. We do not have separate 14 address pins, we have only 1 common set of 7 address pins by which both A naught to A 6 and A 7 to A 13 are send. So, when you send A naught to A 6, right, so if you consider them as a row address. So, this particular row address select this particular stroke, is exercised and that is lags into this particular resistor.

And then when you are sending A 7 to A 13, so this one will be at a different point of time of course. So, this column address select this particular input to this column address latch that will be stroked and it will store that information. So, this is going to row address decoder and this is going to column address decoder. And we have already noted the memory you know based addressing scheme, matrix based addressing scheme before. So, this is the row address that will come, and this is the column address that will come and at the cross point there is the memory cell. So, what is happening now because of this that we are able to save 7 such pins, but the address bits are made available at different point of time. So, this is the multiplexing aspect of it.

So, whenever the number of such pins requirement becomes high because of higher packing density we can think of some such way of addressing which is also known as multiplex addressing. Clear?

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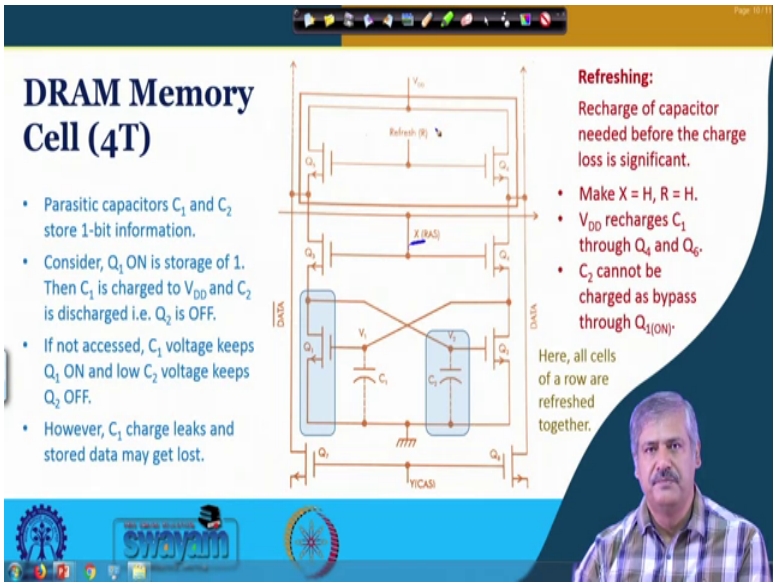


Now, we look at one DRAM memory cell, which is 4 transistor base; it is somewhat similar to what we had seen in case of 6 transistor base MOS based SRAM cell in the last class. So, there is some differences that we shall also tell.

So, first of all, so this is the basic memory cell whatever you see over here. So, this is the basic memory cell. In SRAM based memories SRAM using MOS what we had? After this we had a NMOS load connected to V DD. So, this was always connected, this was always connected and the transistors; these opposite transistors were acting as inverter and the memory cell was you know was basically made up of these 6 transistor put together, right.

So, in this case it is those low transistors are not there holding the cross coupled inverter in one particular state value, rather the capacitances that are there which can store charges for a short time they are used in this particular case. Of course, as we have noted even when the memory is not read or written into, so it need to be refreshed for which a separate refresh lines are you know associated. So, let us see how it works, right.

So, the first of all these parasitic capacitance is C 1 and C 2, they are used for storing of information to start with we consider that Q 1 ON. So, this is the Q 1 ON is storage of 1, and Q 1 ON; Q 2 OFF and Q 2 that is storage of 1 and Q 1 OFF and Q 2 ON is storage of 0. So, that is the nomenclature that is what we are following. And that time C 1 is this C 1 is charged to V DD by some mechanisms of these data lines or all those things that we

shall see during you know writing process how it happens. So, this is charged to be ready.

This is ON and at that time this is charged to a low value, low value. So, that will be the case because this is ON means this is a low resistance path, right. So, C o C 2 will be having a (Refer Time: 09:57) about 0 Volt. Is it ok? So, this is V DD and this is because this is ON. So, there is a path that is available. So, if not accessed means this X is low, Y is also low so that means, this is isolated from the rest of the circuit. So, it will maintain this value, if these capacitances are not leaking. So, C 1 it will maintain its value, C 2 will maintain its value this is at V DD and this is at 0 Volt but as we have noted that it is C 1 charge which is which is charged up to V DD it will gradually leak and it will come closer to the C 2 value then the information will be lost.

So, before it loses significantly it whatever charge it has there with it; we need refreshing, is it fine. And for refreshing then what we do? We need to recharge the capacitor, and for which what we consider here this X we make high, right and this refresh R input we make high, right. So, at that time what is happening? So, this is high, this is high, this is high. So, this is ON, this is ON, this is ON, this is ON, this transistors are providing path to this V DD.

So, what will happen? So, this V DD will get the path over here to charge the C 1, is it all right? Because Q 2 is OFF because Q 2 is OFF, so the path available over here is this; is it fine? And at that time what will happen? What about this path? So, V DD there is a path over here, but this particular paths this Q Q 1 is ON, right, so it will go through this you know a load resistance path over here and for which this C 2 will remain at you know low voltage only, is it ok? Because it is getting bypassed when this is 1 so, before it appreciably falls, we need to do this refreshing, is it all right?

So, all the rows, all the cells in a particular row, to which X is connected; so they get refreshed that you know together, by this particular line. So, this is the refreshing act that is happening at a periodical periodic interval; even when read or write operations are not taking place, right.

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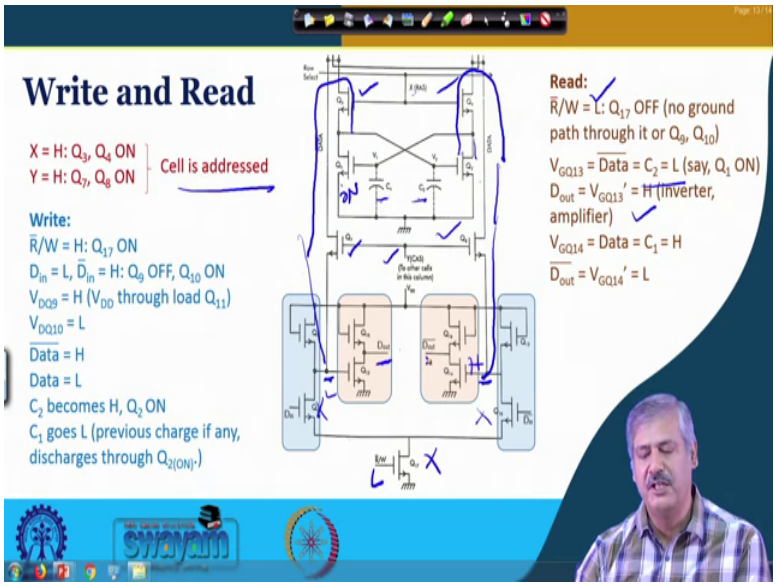


Next, let us see how the write and read operation takes place in this particular set, right refresh we have understood. So, what we see, this is the you know the control block; this control block is similar to what is there in the NMOS based SRAM that we discussed in the last class. This particular block is similar. This block is different. The control logic part remains as it was for SRAM, which we did not discuss in that detail, but we can apply this particular block there also and understand how it works.

So, coming back; so, for the write operation these block and these block comes into picture, right. So, at that time of course, this cell need to be accessed, so X is high, so row address select and Y is high, so for which this transistor is ON and this transistor is ON, this transistor is ON and this transistor is ON, is it ok?

So, now this is the data and these data bar line. So, this gets a path; this gets a path from here through it because these transistors are ON, like this to come here, similarly this address gets a path over here, sorry like this to come here up to this point. Is it clear? So, in the write operation, so this particular one is high, so this is ON. So, this is ON, right.

So, if D in is low, right, so if this is low then this transistor will be OFF. So, I put a cross mark means OFF and then D in bar will be high. So, this will be ON. So, at the time what happens? If this is OFF; so this is the transistor is used as a load. So, this will be high and this will be this one is ON means that is a path available this is also ON, this Q 17 is also ON. So, this will be low.

So, at that time you are forcing from external you know this through these data line, a high over here and a low over there. So, what would happen because of this? So, this high and this is low. So, this C 1 will become low because this is low and this is high. So, that will charge C 2 to high. Is it clear? It is being forced externally through the data lines. So, that is what is happening, right and what about charge C 1 has; now C 2 has become high, so Q 2 is now becoming ON, right, so it will get discharge through this, right through this. Is it clear?

So, that way earlier Q 1 was ON the consideration that we had with which we had started the discussion now this Q 1 becomes OFF and Q 2 becomes ON. So, earlier we considered Q 1 ON means a storage of 1, now Q 1 become OFF so it is now storage of 0. So, whatever data D in that was low so low that has been communicated that has been you know included now in the memory cell. Is it fine? So, this is the way. So, similar thing this is symmetric in nature if D in is high similar thing will happen for the other side from the other side. So, this side will be high and this side will be low corresponding transistors will be you know ON or OFF and you know the data writing we will takes place accordingly. Clear?

Now, what happens to read operation? So, during read operation this input will be low, this is low. So, this is off. So, if this is OFF means, this does not get a path in this direction so, and also this D input is not in consideration. So, at that time your of course this is accessed, this is accessed. So, this is ON, this Y is high and X is high. So, this is ON and this is also ON these two are also ON. So, this is the cell being addressed.

Now, if the C 2 is low say C 2 is low. So, C 2 is low; that means, C 1 is high; so Q 1 is ON. So, what will happen at that time? So, this V G Q 3; so this is your Q 13; so, this is your 13.This is the read amplifier and this is the 14, this is the another read amplifier. So, at that time what has happened? If this is low, it is low. So, this low will come through this and so, this is low over here, this is low over here. So, this is the inverter configuration amplifier. So, this will be a D out will be high, right.

So, this is high at that time. So, C 2 low that is Q 1 ON so, D out you see as high and at the time what will happen to this line? So, C 1 is high and Q 2 is OFF. So, this high comes over here. So, this high comes over here through this data line and comes to this

point. So, this is high. So, this transistor is ON all right V 14 is ON, so these output is low. So, this is the way data is read from the cell, fine?

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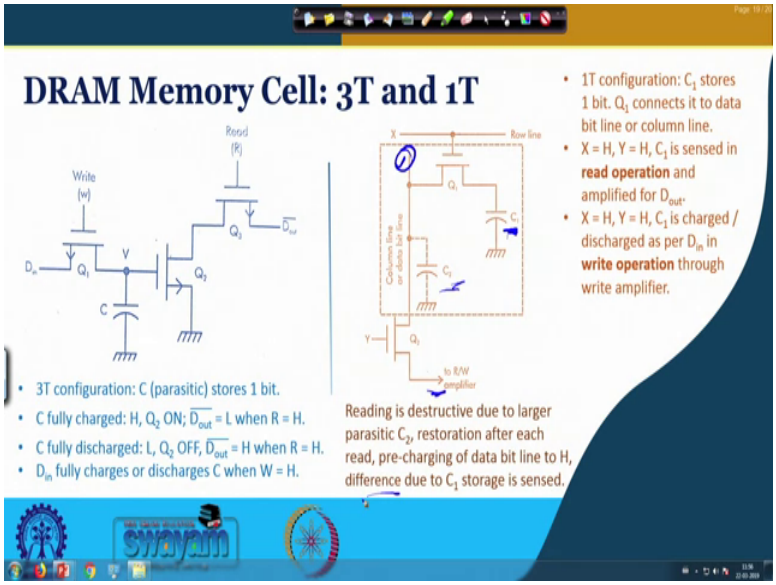


Now, looking at the other two DRAM cell configuration; memory cell configuration with lower number of parts. So, one is 3 transistor configuration. So, here what you can see that this is the parasitic capacitance between the gate over here at the ground that is there which is used for storing the information. When the C is fully charged, this voltage is high, so this Q 2 will be ON and then this ground is getting a path over here, so D out will be low. And if it is low then it is OFF and this D out bar will be high.

So, if just opposite things is available. So, if it is high this is low, this is low, this is high. So, that is why it is D out bar that is has been mentioned over here and for writing; so, then this is w is ON. So, at that time this D in if it is low, so it will be low and if it is high then capacitor will be charged to high value. So, this is the way it works over here.

And for one transistor this is the memory cell. So, this is a capacitor, this is not you know the parasitic capacitor we were talking about, this is an external capacitor which is storing the information this 1 bit information and so this is the Y address line and this is the X address line. So, this column line that you see is also data line so which increases you know packing density further, but there is a catch we shall see. So, when X is high and Y is high. So, both of them are high. So, whatever is the value of the C 1 that gets sensed when the read operation is done. So, this is the way it is sensed.

So, if it is low then it is sensed as low, if it is high it is sensed as high, there are some issue we shall now shortly discuss. So, that is the read operation and the write operation of course, when both of them are high so, from this side; so, this is from the right amplifier this one this transistor is ON, this transistor is ON; this C 1 gets charged according to low or high value that is coming from the right amplifier. So, this is the way this memory cell is storing information high or low.

Now, regarding the other issues that are there with this arrangement so, here there is a parasitic large parasitic capacitance that occurs as C 2, over here. Remember this is column line so many such lines will be in parallel, right many such you know cells will be addressed. By this particular line, so many such capacitance I am sorry there will be in parallel. So, that will increase the effective capacitance value of it which is roughly you know 10 times more than this capacitance value.

So, whenever you read it, because of the charge sharing charge dividing that is happening discharge coming over here; so, it becomes a destructive reading. So, this charge information here it gets lost. So, after every read you need to have a restoration. Restoration of whatever previous value was there in this C 1.

So, this is an additional thing though the density is more less number less least number of parts are used. So, this is a one transistor configuration and the other issue with this one is that for reading it is preferred that you pre-charge this particular data line the column line to high value, so that means, this capacitance etcetera is already pre-charged. Now, after that whenever this X is becomes high I mean this particular cell is becoming getting accessed, then depending on the value of C 1 which is low or high. So, there will be small increase or small decrease in this particular value, over here in this reading. So, that difference is actually getting sensed. So, this is the other way of you know reading this particular thing. So, that is also something which we consider in this case, but it provides the maximum density.

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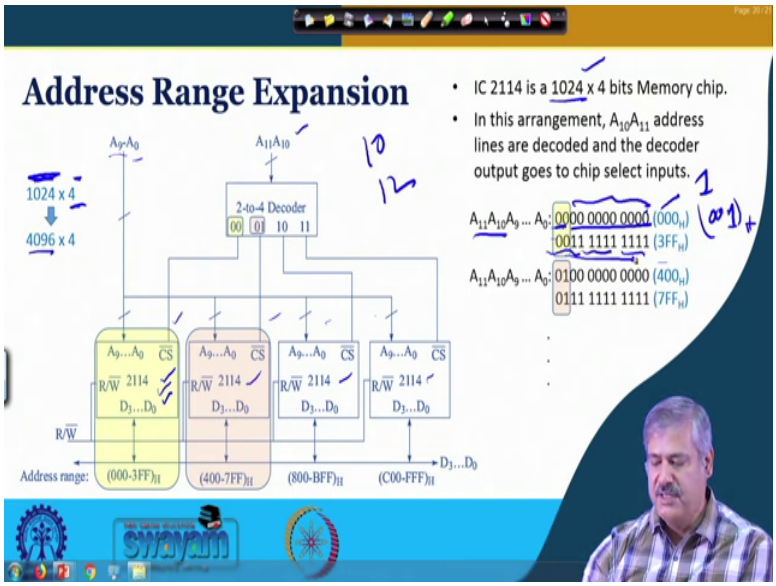


So, we now move to these memory expansion and when we talk about memory expansion there are two possibilities one is the address range expansion. So, what do you mean by that? So, there is an example. So, this is the number of rows, that number of addresses, number of locations, that is 1024 and each; in each address there are 4 bits of binary information is stored, so 4 bit word is there. So, when we talk about address range expansion. So, it remains 4, but now we want 4096, 4 K number of memory you know locations available for the designer.

So, how we can do that? If we have a 4 K cross 4 memory it is fine you can directly use, but if you have 1 K cross 4 like this, right; what you can do to expand the address range which originally is meant for 1 K address, 1 K you know memory locations. So, to do that one mechanism that you can see over here; so, 1 K means 10 address lines will be there, 2 to the power 10 is 1024, and 4 K means 12 address lines will be there. So, you take 4 such 1 K units. So, this is 1 unit, 2, 3 4.

And the lower this 10 bits A 0 to A 9, which is you know there as address bit inputs to each one of this 4, so you make it common. So, you connect it to all of them. So, higher 2 bit A 11 and A 10 you pass it through a 2 to 4 decoder to generate 4 such lines, so 00, 01, 10 and 11, and then that you connect to chip select lines of each one of them. So, what does it mean? When 0 0 is placed here A 11 and A 10; so, this particular block will be selected and not the others one, other ones. So, if this is 0 0, if this is 0 0 and this

address A 0 to A 9 is all 0, so basically you are accessing the location 0 0 0 in hex. So, all of them are 0 that particular location is accessed. You can read from there or you can write it, depending on what operation you are doing.

So, if you now change these A 9 to A 0, 2 00 0000 000 1; so, this 0 become say 1. So, it will happen. So, you will be reading from location 0 0 1, that is in hex, from that location you will be reading or writing; so, because this is remaining these two, A 11 and A 10 remaining constant at 00. So, whatever you do with the rest of the A 0 to A 9 bit, that is happening over here in this particular block and how much you can go ahead with this? So, all becoming 1, A 0 to A 9, so that is your 3FF, that is your 3FF that you can read in hex means group of 4. So, this address will be available here.

So, next if it is 01 so 01, this A 11 to A 10 so, this is what it will be considered. This decoder output will be considered. So, according this chip will be selected; rest are not selected, ok. So, when this one is 01 and rest all these A 9 to A 0 is 0, so basically you are looking the first address, of this particular memory block. So, that is 400 according to these expanded address range and last address one will be 7FF, similarly this one will be 800 and last address will be B FF and this is C00 and this will be FFF. Is it clear? So, that is the way we can increase the address range.

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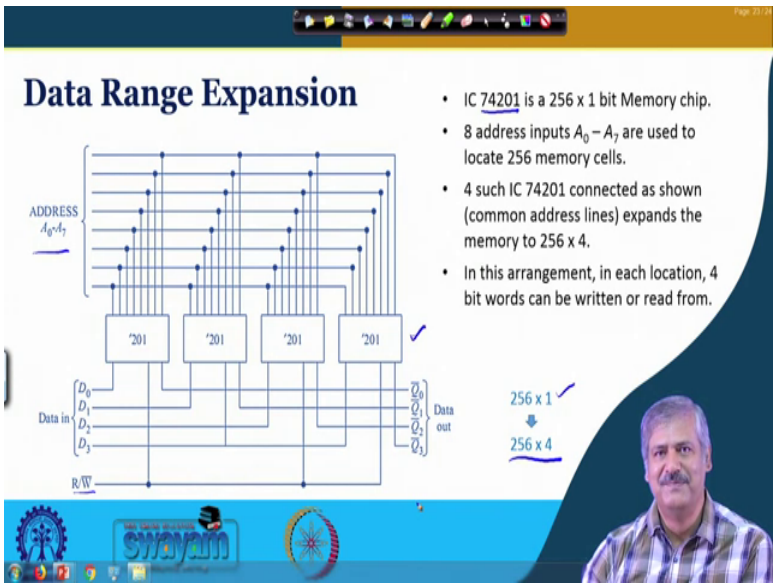


Coming to data range expansion. So, the number of address bits remain same, data bit we want to increase. So, here is an example. So, this is 7 4 IC 74201 is a 256 cross 1 you

know memory block memory IC. So, that means, 256 addresses are there in each address location only 1 bit information can be stored, on which information is there. And we want 256 cross 4, what we will do? We shall put 4 of them in parallel as you have see over here alright and the address line we will make common and the feed same address line.

So, whenever now invoke the a particular address, so each one of them will be you know invoke it each the first location for each one of them will be addressed, right and then you can write or read from each one of them, depending on your control inputs and each one will give you 1 bit of information and together you get 4 bit of information. Clear? Simple.

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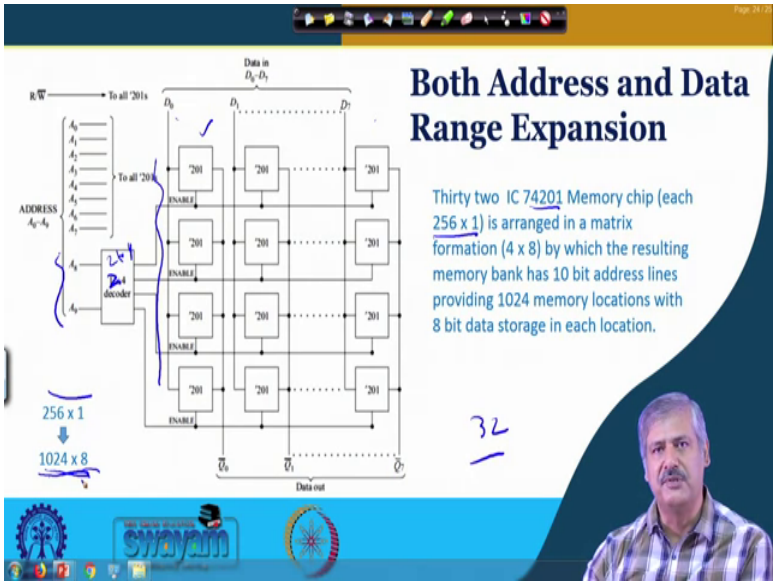


Now, if you want both address and data range expansion; whatever we have learnt just now we shall put them together. So, one such example over here say 256 cross 1 so that means, that example of 74201 which is 256 cross 1 memory cell and that is there and we want a memory which is 1024 cross 8 using it.

Then what we shall do? Right, we need to you know increase the address range otherwise also increase the data range. So, address range; so which was to start with 256 means 8 bit address was there and 1024 means 10 bit address will be there. So, for this additional 2 bits we will be having a; so this is a 2 to 4 decoder sorry, will be there 2 to 4.So, it will be generating 4 addresses the way we had seen before and in each location, I

will 1201 provides 1 bit of you know binary information and we want 8, so 8 such will be there D naught to D 7.

So, 4 such rows which is expanding the data address range the way we have configured it and 8 such columns increasing the data range. So, 4 into 8 32 such, memory blocks of IC 74201 will be required to get this one, is it fine? And this memory block could be any of SRAM, DRAM type of depending on whatever you are using.

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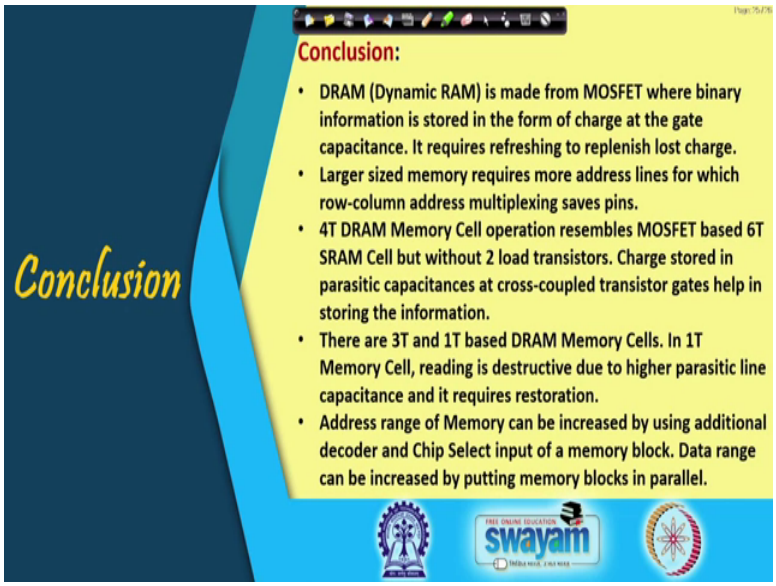


So, with this we come to the conclusion of this particular class. What we have seen? That dynamic RAM made from MOSFET stores charge, stores information in the form of charge which is available at the gate capacitance parasitic in nature because of the leakage it requires refreshing to replenish the lost charge. Larger size memory we can do better by multiplexed row column addressing which sets pins, number of pins that would be required for the memory IC.

And we had seen how 4 transistor DRAM memory cell, 3 transistor memory DRAM memory cell and 1 transistor DRAM memory cell works and their you know specific characteristics. And further we had noted that address range and data range of memory can be expanded by using additional units and decoder for increasing the data range and also using chip select unit together.

Thank you.