Digital Electronic Circuits
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Lecture – 57
Static Random Access Memory (SRAM)

Hello everybody, we were discussing Memory. And in the last class we got introduced to a memory organization where we had noted that each individual memory cell are the ones where the digital information is stored ok, in the form of one bit information ok.

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So, in this class we shall look more into this memory cells and we shall look into this BJT Bipolar Junction Transistor based memory cell, as well as CMOS and standard MOS based memory cell ok. And what you have taken up is called static RAMs, Random Access Memory you have already seen static we have already defined in the last class that static RAM is the one where the periodic refreshing is not required.

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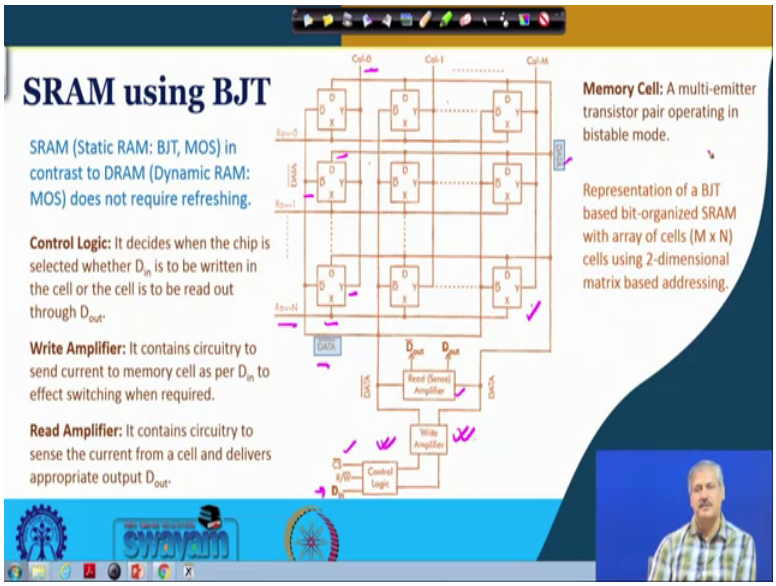

And we shall discuss the other type of RAM also called Dynamic RAM or DRAM in subsequent class. And at that there we will see that in that DRAM based you know memory organization the information is stored in a capacitor, which could be leaky which essential is leaky. So, it requires periodic refreshing ok. In static RAM the one that we shall be discussing now, that is not there ok. So, you do not require that kind of thing, but in DRAM the number of parts required is less ok. So, here the number of transistors and other things this circuit limits will be relatively more.

So, in DRAM the packing density will be a little bit what is that called a mode, but here SRAM it will be faster and it is this refreshing is not required. So, these advantages are there. So, more of DRAM we shall see later. So, today we discuss this static RAM memory unit and more specifically the memory cells.

So, here we begin with the BJT based this memory cell. So, we had seen some such organization before right, we had seen a memory cell in the last class if we remember and this memory cell had 2 lines. Now, we have redrawn it in a little bit different manner.

So, this is one line D, another is D prime that what you see basically so, from each memory cell 2 lines are coming out ok, it can be also called bit lines.

So, 1 bit so, this is data and this is data bar 1 is opposite of another ok. So, this is what we note ok, other than that what we see this is X and this is Y. So, basically these are the

addressing of a particular location in the memory block. So, this is coming from row and you know this is a matrix based arrangement matrix based addressing.

So, it is coming from a row decoder. So, this is the row line and this is coming from a column decoder. So, this is the column line ok so for which when both of them are I mean activated. So, this particular cell is addressed ok. So, other than that what we see, this is what we had seen before what we see that there is a control logic block. So, this control logic block a similar to what we had seen before in addition we have got a data in input ok.

So, this is chip select and this is read or write operation that we are doing, other than that what we else we see, this is a right amplifier block. So, when you are writing it. So, this is some additional circuitry which actually making it happen ok. So, we shall analyze it, we shall see what is there inside and then we have got read amplifier. So, this is the read or sensing amplifier. So, what is there in the cell, that we would like to sense and make it available to the outside world.

So, this is a typical SRAM you know memory block and we shall move forward and in the memory cell. We shall see that there is a multi meter transistor pair, connected in a cross coupled mode and which is operating in a bistable mode as well that is either it is one transistor is ON or it is OFF ok. And the corresponding transistor will be in the opposite state if one is ON another will be OFF. So, let us see ok.

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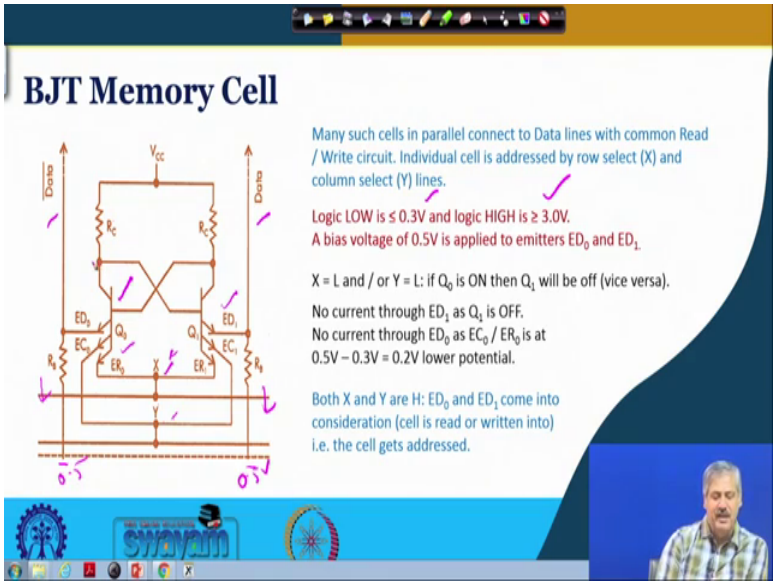

So, this is the basic memory cell all right. More of it how it gets connected to the other part that is sensing amplifier, right amplifier and all those things control logic we shall see in subsequent slides. So, this is the multi meter transistor pair that we have talking about and you see that they are connected in a cross coupled mode. So, each one of them as such can be considered as an inverter right. And this is the column and this is row and column address the select line ok. And when they are not selected; they are not selected the value are 0 and if their selected value is 1, that is high so, otherwise it will be low ok. And this is the line that is going to those data and data bar bit lines right.

So, this is E D 0 and E D 1 that you see over here ok. And other important thing that we note here that in a BJT based circuit. So, whenever the transistor or the one that is driving it is at logic low ok. So, the value is 0.3 volt or less. So, saturation will be you know 0.1, 0.2 or even lower depending on the level of saturation. So, logic low that is placed over here can be considered as less than 0.3 volt ok. And logic high we have seen before if it is a T l based circuit or you know this transistor the operation.

So, we can consider this to be greater than 3 volt when it is logic high. So, other than that we take note of that this lines has a bias voltage connected to a power supply and resistance, we shall see that circuit little later. For which 0.5 volt is presented over here, 0.5 volt is presented here. And now depending on amount of current etcetera flowing small drop might be there, but otherwise it is 0.5 volt ok.

So, when these are low or any one of them is low this X or Y are low ok. So, this is 0.3 volt right and this is 0.5 volt. So, current will not be flowing in this direction is it clear right. So, at that time these particular circuit right, this emitter, this emitter, this E D 0 and E D 1 is not you know contributing in anyway electrically not contributing ok. And these are remaining at you know when these are remaining at 0. So, the current will be flowing in this way in this manner ok, this is the first thing you observe.

Next is these two transistors can both of them be ON or both of them be OFF ok. Now, if you investigate you can see that both of them ON and or both of them OFF is not possible ok. So, if say this is ON then what is the voltage over here this is you know ground. So, this will be in you know we here ON means, we are it goes into you know saturation so, this R c alright.

So, this is say 0.3 volt or so, 0.2 volt whatever this saturation value. So, that will not be enough to drive it on. So, that is a small voltage small voltage, it is not you know more than you know the decimeter, you know voltage that is required 0.6 volt or 0.7 volt.

So, this will be OFF at the time, if it is ON this is OFF ok. Similarly, if it is OFF then this is not conducting so, this is the voltage will be high. So, sufficiently high so that will be 5 volt to drive it deep into saturation and vice versa is it clear ok. So, one of them need to OFF and one of them need to be ON and as long as this is remaining at 0 and all. So, this is what is happening. And how to switch them if say Q naught is ON alright and Q 1 is OFF how to make Q 1 Q naught OFF and Q 1 ON in the right operation that we shall see little later, is it fine right.

This part is the major thing. And this is similar for your MOS based cell or CMOS based cell also where 2 inverters will be connected back to back in a cross coupled manner rather, like this with we can see the feedback coming in this manner right; so, similar thing will be there for the other cases, which will you know offer a bistable mode of operation for this particular block right fine.

So, when both of them are high this X and Y are high; that means, this memory cell is now accessed ok. So, when these are high. So, basically this particular line will be now operating. So, the current now will be flowing, because this is a with during E D operation 0.5 volt or so, right operation we shall see what is happening at that time ok. So, the current will be directed in this direction.

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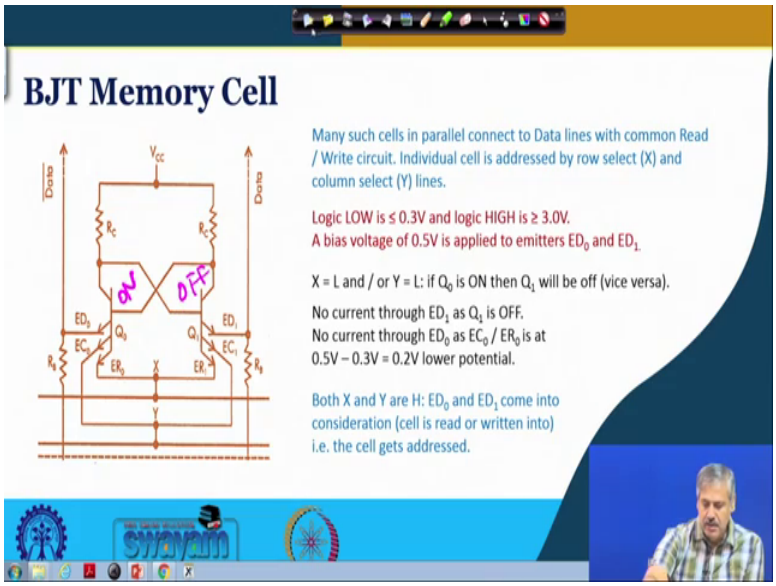

So, we consider for our general discussion that Q naught is ON and Q 1 is OFF ok. The similar discussion I mean this is just a analogues. So, if it is otherwise the similar analysis will follow ok. Just which is almost which is equivalent for whatever we discuss for Q naught being ON.

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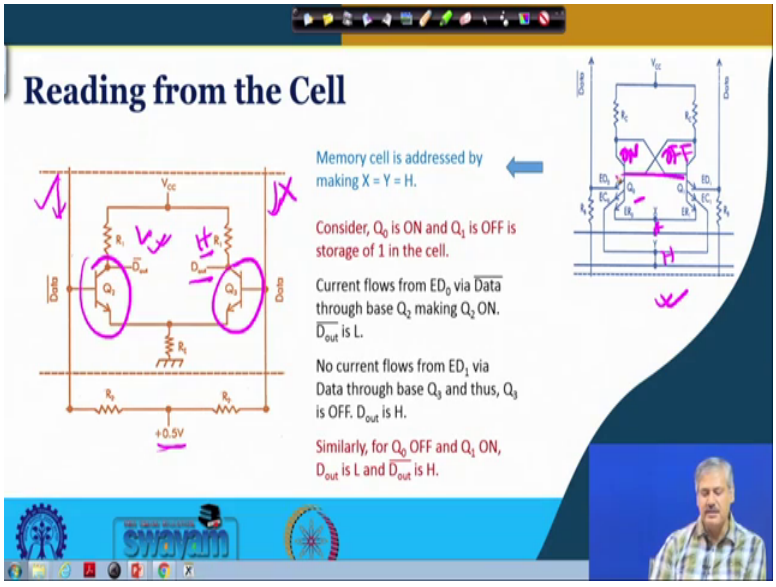

Now, we look at reading from the cell so, X so, this cell is already you know presented here. So, this is the cell that we had seen before. So, this is Q naught. So, this is ON now and this is OFF right. And X and Y we have made it high so, this is high and this is high

ok, more than 3 volt also right. And this is the bias voltage has been kept in the 0.5 volts. So, this is the bias voltage that I was talking about right ok.

So, now this transistor is ON so, this emitter from this emitter the current will flowing in this direction right. And this transistor is OFF so, no current is flowing. So, no current is flowing, current is flowing in this direction from through E D 1 no current is flowing, because this transistor is OFF is it clear right.

So, now, this current that is flowing right so, when it passes through this Q 2. So, the Q 2 will become ON and in this case this Q 3 no current is flowing. So, Q 3 will be OFF. So, when Q 2 is ON this D out will be low ok. So, this will be low and this will be high, is it alright. So, Q naught is ON then the data rate through D out is high so; that means, a storage of one is there for such configuration ON and OFF, is it clear.

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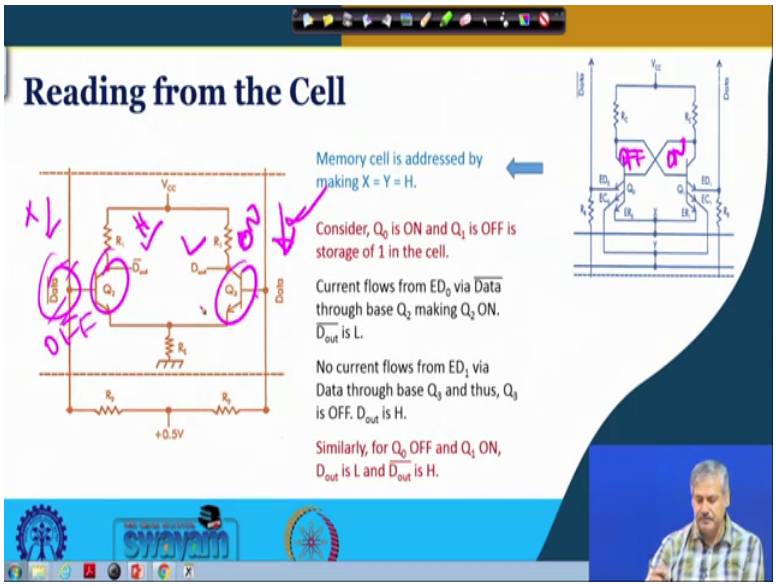

In contrast had been it been the case that this is ON and this is OFF ok, then current would have flown in this direction this is right ok. And it would not a flown in this direction because this is OFF so, this current is flowing in this so, this is will be ON and this will be OFF sorry not this one, this will be OFF right. So, this one will be high and this one will be low right.

So, Q 1 ON is then data out is low and Q naught ON is data out is high ok. So, this is the way we can visualize that storage of information and the reading that is taking place, is it fine.

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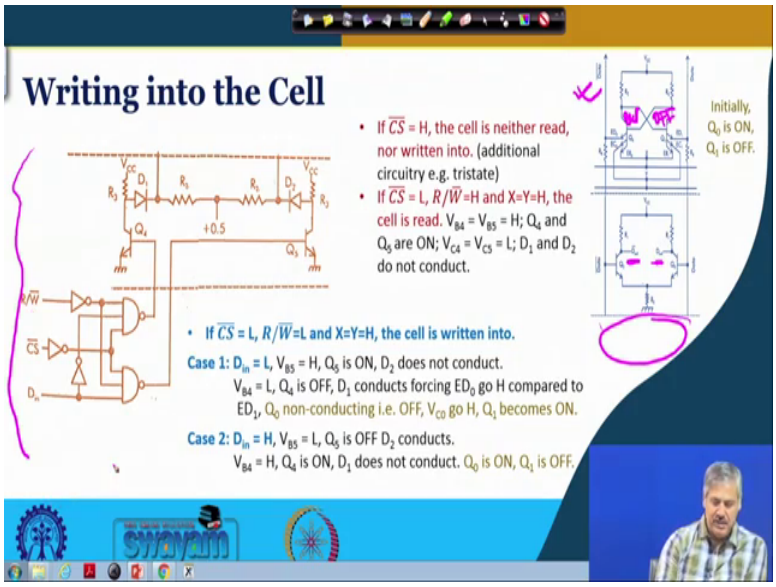

Now, we look at the writing operation ok. So, the circuit that you can see, now this is the basic memory cell ok. And generally we consider this is ON Q naught is ON and Q 1 is OFF right. And this is the data line or the bit line and this is the reading or sense amplifier.

So, this is D out bar and this D out which we have already seen. Now, here in this place we are having this particular block. So, this is extended to this a particular side ok. Now, what you have got here? So, we can see that this there is a read write logic control logic is there, chip select is there and data that we want to write ok, that is also there fine.

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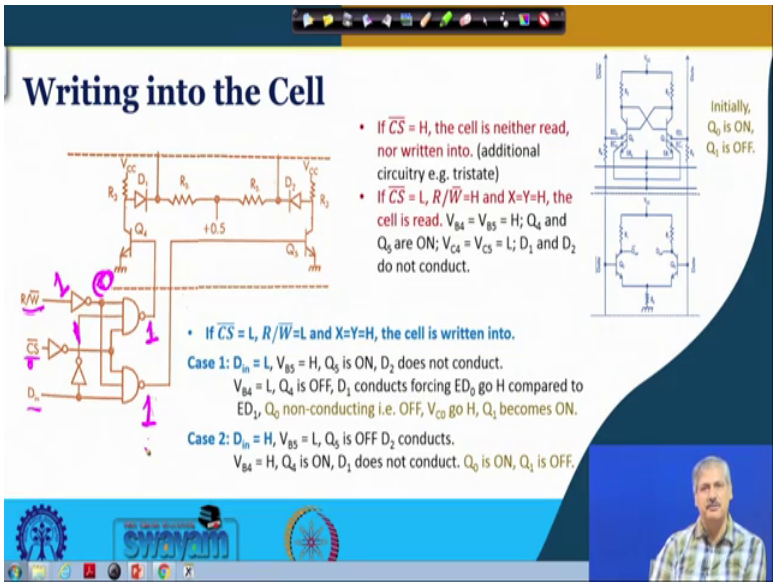

Now, if chip select is high, if chip select is high then the cell is neither read nor written in it ok. So, chip selecting is high means this is 0 ok. And so and there are other circuitry also to make these particular thing tri stated and when chip select is low when chip select is low. So, then this is 0 so, this is 1 ok. And at that time if this read write input read write bar input is high ok. So, this is your high ok. So, that is read operation that you know let us read the operation. So, this is your 1 and this is your 1 ok. So, this is your so, this one will give you a 0 over here is it clear ok.

So, this 0 will generate for this NAND gate output a 1 and it will generate a output this is 1 please understand. So, chip select is 0 and read write is read right bar input is 1. So, what we are having we are having a 1 1 over here. Irrespective of whatever be the value of D in ok. Because, this read input 0 means read input 1 means this node gate output is 0 and corresponding this to NAND gates output will be 1, this part is understood.

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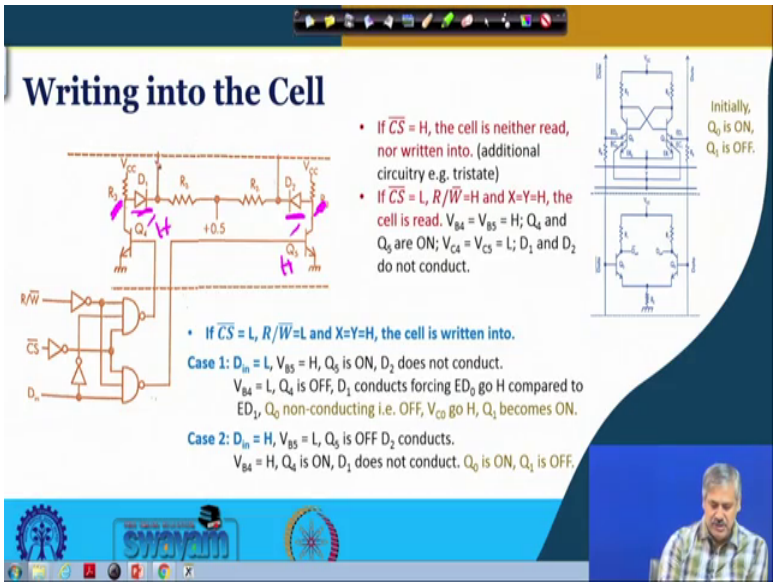

Then rest of the thing is if then this is high and this is high so, this 2 transistor Q 4 ON and Q 5 ON ok. So, this voltage over here is very small this voltage here is very small 0.3 volt 0.2 volt 0.1 volt any of that range alright. So, then this diode is OFF; this diode is OFF so this part of the circuit, so this part of the circuit; this part of the circuit as if it is not there ok.

Because no current is flowing from this direction and it is diode is you know current can flow in only one direction. So, it is not possible to flow current in the other direction as well. So, it is what we had seen before. So, standard read operation that would take place, is it fine. Now, we go to the other option.

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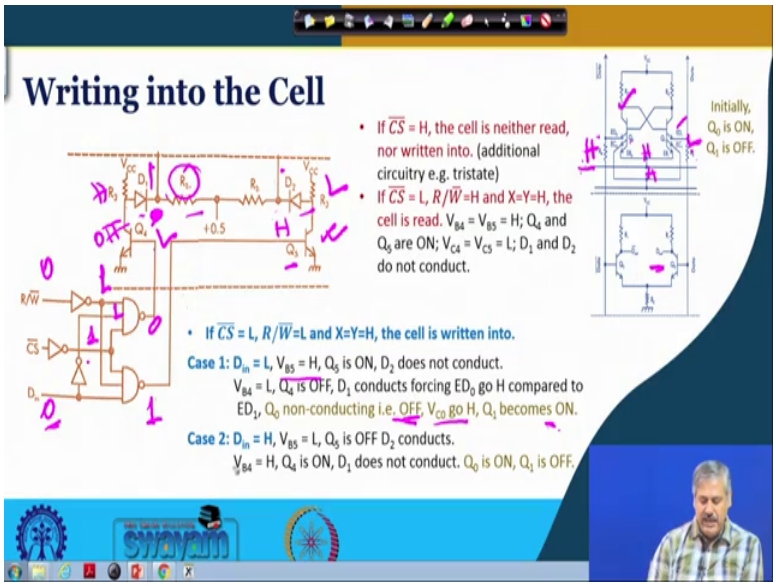

So, now, this read write bar input is 0 ok. So, this is 1 chip select is 0. So, this is 1 ok. Now, if D in is low. So, that is 0 ok. Then this is also 1 this is not gate. So, this is 1. So, this NAND gate output will be 0 and these NAND gate output will be 1, is it clear, this part is understood. Because of which this V B this particular base voltage of transistor Q 5 ok, this is high and this is low, what does it mean.

So, this will be on. So, this voltage will be low over here. And this is low; that means this transistor is OFF ok. So, this voltage over here is high. Now, this diode conducts. High means you know close to this is close to 5 volt depending on you know how much I C R C drop will be 3 right, at there is 0.7 volt drop over here. So, now, these voltages much larger than, what we had seen before? So, this shows that is a path over here, there is a path over here. So, rest of the voltage drop current drop will be over here.

So, that is what you can see now, that this voltage is now held at high. What about the other side this one, it is still at low because this transistor is at OFF. So, this side you have got this is now high this E D 0 and this E D 1 is at low ok. And E C 0 E R 0 E C this E C 1 ER 1 there all are high, because the this particular cell is addressed ok; now, when this thing happens Q naught, which was ON and Q 1 which was OFF.

Now, this is and it was just holding one you know these cross coupled you know structure, if one is ON it remains ON, another is OFF means it remains OFF. So, that was the case at the time. Now, because of this external forcing inputs that you get over here

that this is high and this is low, what to what would happen? So, this transistor now cannot conducting this direction ok. So, this transistor will go OFF and it raises the voltage over here ok.

So, that voltage will allow this transistor to go on right and this is low there is no issue, it is possible. So, Q naught now will go OFF will become non-conducting right. So, V C 0 so, V C 0 is this voltage will go high right which will make now Q 1 ON ok. So, Q naught which was ON now becomes OFF right and Q 1 becomes ON ok. After, if you stop the right operation and you know the circuit is goes back to it is normal state ok.

So, both of them are say 0 these at this is not invoke. So, this cross coupled nature will keep Q 1 at ON and Q naught at OFF the it was happening before for Q naught which was on was remaining ON and Q 1 which was OFF was remaining OFF ok. So, similar thing will happen here, it will remain stable and as I said it does not require refreshing and also basically they are holding each other in a stable mode, is it clear right.

How the switching is taking place within the memory cell for which was the transistors now switching I mean changing there ON or OFF value. And if Q naught ON was logic once or value 1 stored, binary value 1 stored, then Q naught of is binary value 0 stored the way we have seen before and now do the reading we will see that 0 was there. So, 0 will be read now at the D out over here, after this operation ok.

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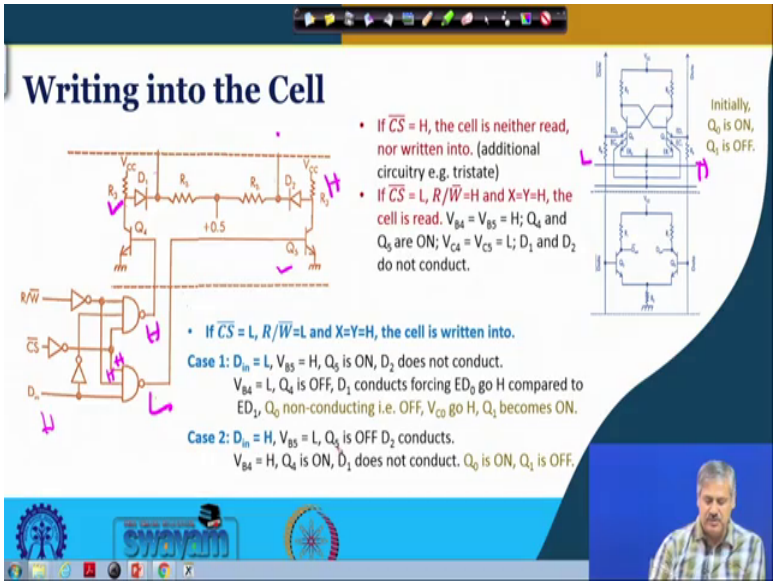

And instead if D in was high ok, then what will happen? So, D in was high means this would have been low and this would have been high if this was high ok. So, this is high, this is high, because of this read and C S inputs ok. So, this is low means this is high means this is conducting. So, this part is low. So, this is not conducting and this is low means this is not conducting. So, this is high.

So, this output will become high means this is high. So, this will become high and this will become low right; that means, Q 2 Q 1 will not conduct and Q naught will conduct. So, which was the previous case as such Q 1 is not conducting because this transistor is on.

So, it will continue to remain its previous value which was a logic 1 a binary value 1 that was stored in this particular cell ok, is it clear right. So, this is how it is taking place in writing operation.

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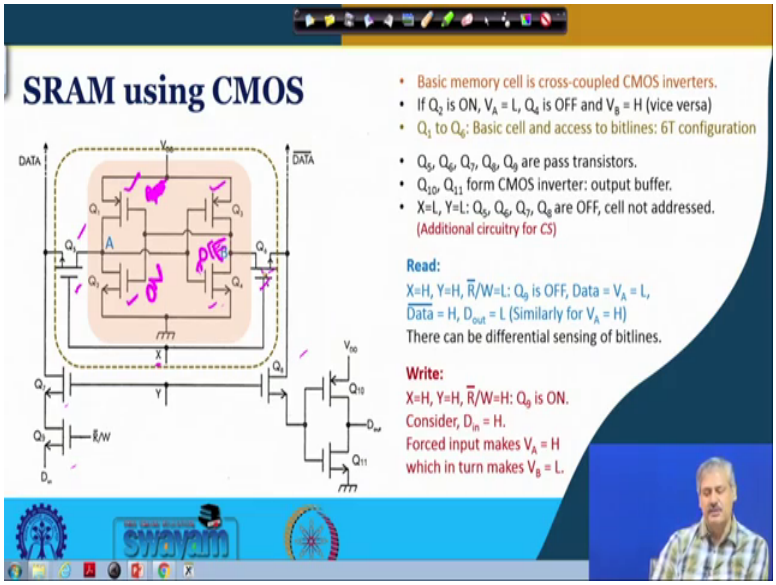

Now, we look at so, BJT if we have understood, similar thing is therefore, other you know types CMOS based or MOS based s RAM static RAM ok. Only that the way the current is driven etcetera etcetera those things are because it is a field effect device those things are little different, but basic understanding remains the same.

So, here we see one you know typical S ROM CMOS ok. So, this is PMOS and this is N MOS, PMOS, NMOS. So, 1 CMOS inverter this is another CMOS inverter and this is

again connected in a cross coupled manner. And we know that from the previous discussion if one is ON, then the other one need to be OFF right. So, if sorry if this NMOS is ON then this NMOS this NMOS need to be OFF ok.

And the way the BJT connection was there right and vice versa, if this is ON this will be OFF is, it clear right. And when this X and Y are you know low then it will maintain it state; now, when this coming from the column address right row and column address. So, this is these are the data lines. Now what you see that this X is the row address ok, coming from the address decoder. So, this transistors Q 5, Q 7, Q 9, Q 6, Q 8 ok, all these are pass transistors ok.

Pass transistors means; if the input is high then we have a channel getting formed. So, basically source and drain there is a pretty low resistance path. So, one is getting connected to the other. So, information you know value signal moves from one side to the other side ok.

So, that is you know the pass transistors that we are talking about ok. And so, whenever this X becomes high right so, the Q 5 and Q 6 mix you know data available to this data and data bar lines to bit lines ok. So, these are the providing access to the data lines ok. So, this over all you know these thing this memory cell; this memory cell and 2 this two of this transistors providing access to the data line ok.

So, there you know often pull together and termed as 6 transistor configuration for I mean this arrangement is called 6 transistor configuration for CMOS S line ok. So, 1 2 3 4 5 6 so, these are the 6 transistors is it fine right. So, when X and Y are low so, this circuit is not addressed ok. So, it is storing because it is in bistable mode whatever information it had and for read operation right. So, both X and Y are high alright and this now if see this is read bar and right ok.

So, this is has to be low for read operations. So, basically then this is a past transistor. So, D in is not allowed to go in that direction, is it fine. So, at that time what about information is there here in the data bar alright. So, this Y is high. So, this is you know getting passed by the pass transistor Q 8 right and then this is a CMOS inverter.

So, whatever is the data bar it is you know inversion is available as D out. So, if Q naught Q 1 Q 2 pair this one. So, this Q 2 is ON ok; that means, the output will be your high ok. And if this is OFF the output will be low is it clear right.

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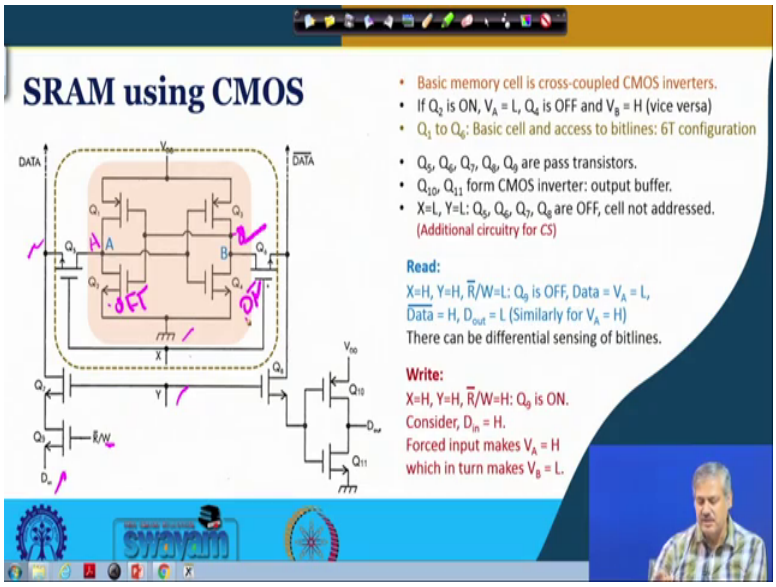

Now, how the write operation takes place again these two address should be high ok, chip select wherever it is providing you know access to this particular chip, that should be at proper value ok. Now this is one. So, D in is allowed to enter right and when this D in comes here again this is a forced input, which is you know and for which this particular output will be of a say high value, see if it is sending a high ok.

So, this high will make this one ON right and that will make it OFF this will this value will be low. So, this low will make this is OFF right and it will remain at high, then if you remove it because of it is bistable nature it will continue to remain this value. So, that is getting switched ok. So, accordingly you know this switching will take place right and for writing a 0. So, this will be low. So, this value will be low at that time ok. So, which will force this one to be ON and this one to be OFF so, this is one typical arrangement.

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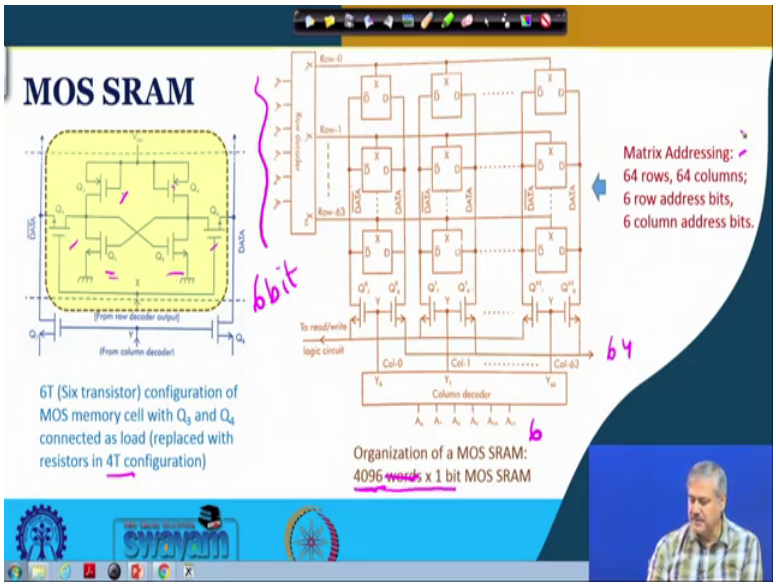

So, finally, MOS based SRAM ok. So, in MOS based SRAM it is compared to BJT based memory cell that you had seen ok. So, we had this two transistors there inverter. And here instead of normal transistor, normal resistor, you can have MOS based transistor, which is MOS based you know resistance made, which takes less space ok. Otherwise, one can make a normal transistor, normal resistor also in this place and this will also provide the same cross coupled bistable mode of operation, cross coupled inverters providing bistable mode of operation ok.

So, if these are again you know loads are you using made using MOS based transistor ok, then you have got 1 2 3 4 and this 2 providing access. So, 6 transistor configuration and if these are replaced by normal resistance right, which will take more space and all bit difficult, the kind of packing density that this MOS based devices provide it will not be able to you know get it is optimal you know uses.

So, then that will be called 40 and configuration or port transistor configuration ok. So, this is one typical organization and if you look at it you can see there are a naught to a 5. So, 6 bit address. So, 6 bit address 6 to 64 address decoding that is what is happening ok.

So, 64 rows right here also 6 is there. So, 64 rows right. So, 64 into 64 so, 4096 words are there and in each place you are storing 1 bit of information. So, this is a 4096 words 4096 into you can say 1 bit MOS RAM 1 MOS S RAM let bit organized is it fine right. So, and this is matrix addressing right fine.

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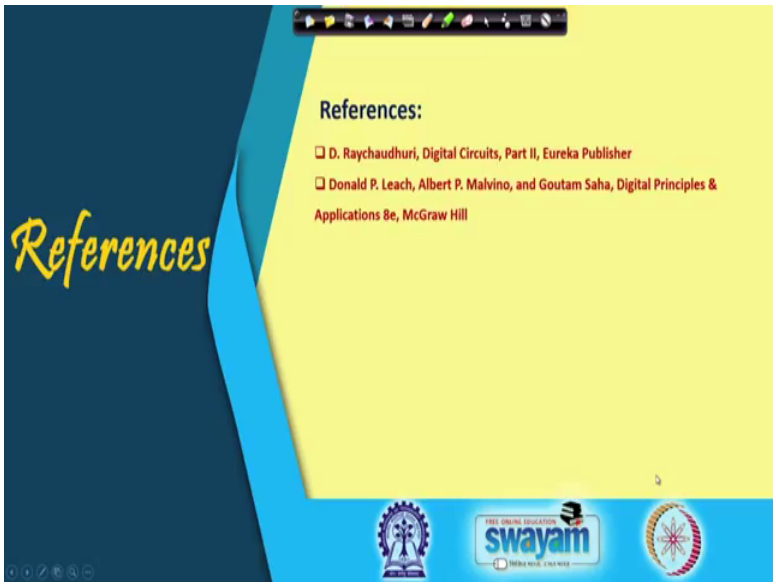

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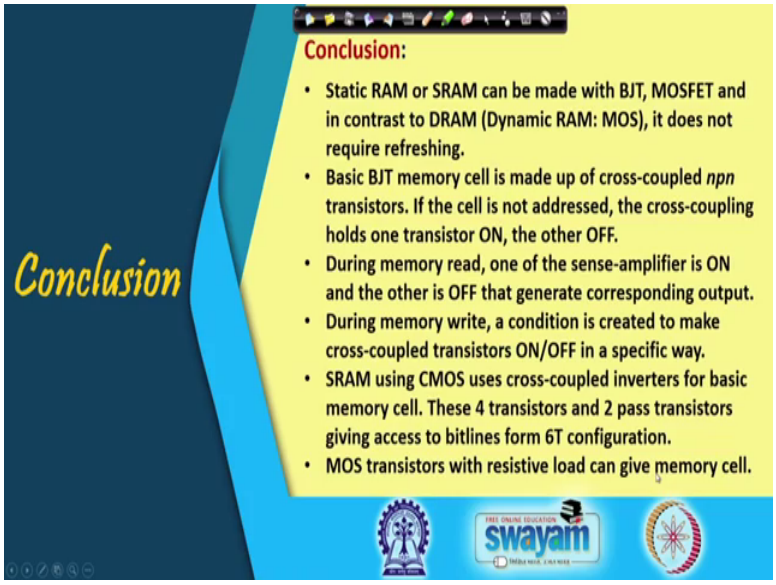

So, with this we conclude and what you have seen very quickly that static RAM or SRAM can be made with BJT, MOSFET, CMOS ok. And in each case we are looking at cross coupled inverters made up of transistors and their operating in bistable mode. And for BJT we have to seen how this sense amplifiers and write amplifiers work. Similarly, we had seen it the CMOS and normal MOS; so, the uses of pass transistors for reading and writing operation.

Thank you.