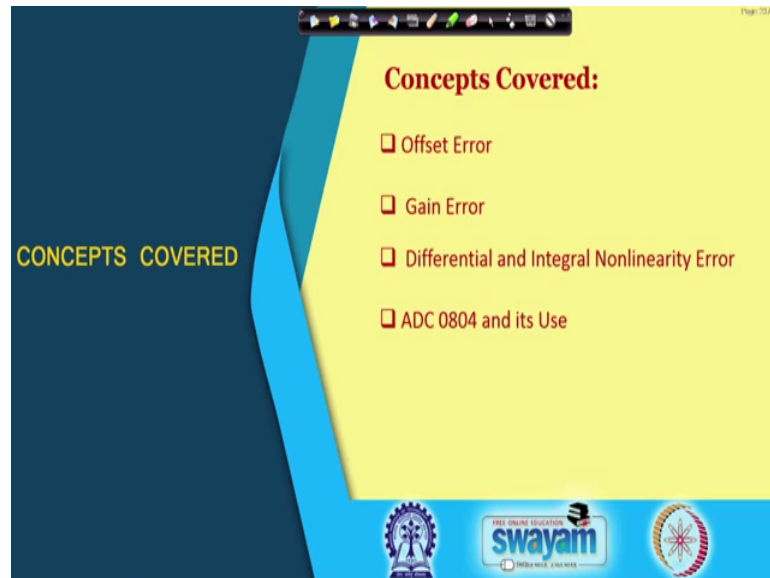


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**Lecture - 55**  
**Certain Performance Issues of ADC and DAC**

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Hello everybody. In this class, we shall discuss certain performance issues, which are having some common element for both ADC and DAC. And this is in the form of offset error, gain error, differential and integral nonlinearity error, so these are the terms that we shall get familiarized with. And we shall see how it matters for ADC and DAC operation. And also we shall look at one IC analog to digital converter IC 0804 ok, and how it is used so that also we shall see in this particular lecture.

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**Performance Issues**

- A/D converter is a closed-loop system involving both analog and digital systems.
- Digital error comes from resolution of the system.
- Inherent error due to digital step is called *quantization error*.
- If the comparator is centred, the quantization error is  $\pm \frac{1}{2}$  LSB.
- Increasing number of bits, quantization error can be reduced.
- Main source of analog error is comparator which is centred around variations in dc switching point.
- Variations in switching are primarily due to offset, gain, and linearity of the amplifier used in the comparator (depends on i/p voltage and temperature).
- Other sources are: Resistor, Reference Voltage, Noise.

mean square error  $\overline{E^2} = \frac{1}{q} \int_{-q/2}^{+q/2} E^2 dE = \frac{q^2}{12}$

For an input sine wave  
SNR =  $6.02n + 1.76$  dB

*quantization noise*

Now, when you talk about performance issues, and we have been discussing ADC in last two classes. So, we had seen that ADC is a closed-loop system ok, so it has got both analog components and digital components, is not it. So, the error will be contributed both by both of them. And the digital error the part is mostly comes from the what is known as quantization ok. So, how many bits, how many discrete levels that you are having that is actually given you some error right in the beginning. If the number of bits are more than number of levels to which the analog voltage can be associated with are more, so the in between steps are I mean where the ambiguity could be there ok, so that is less ok.

So, this is certain thing which is coming from the digital digitalization part or digital part of the error that is how it is you know visualized ok. And if the comparator is centred, then this particular error would be like this depending on the input voltage from plus half LSB to minus half LSB, it will be within that particular range. And if it is the analog voltage is such that each of these value within plus and minus half LSB is equally probable ok.

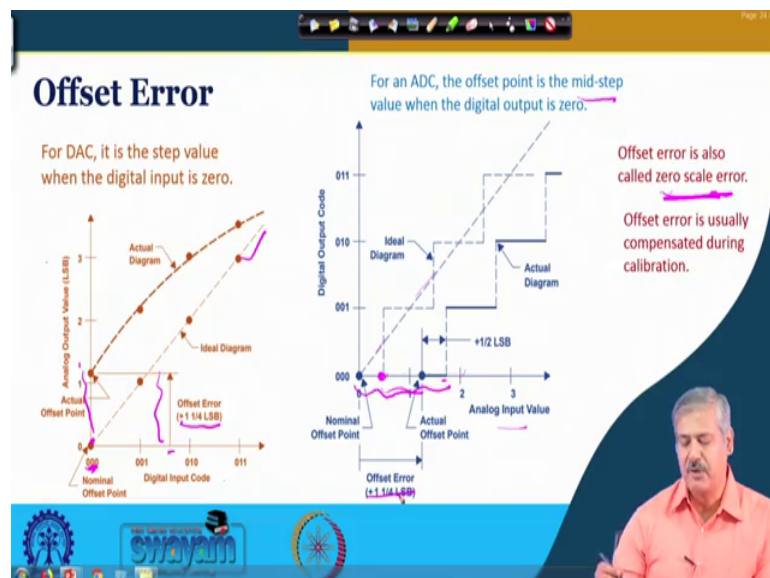
Then we can calculate the mean square error of it of this particular error, this is as  $E^2$  square  $dE$ , and it all of them are equally probable. So, probability of this according is one. And if you integrate, then you can see that it is  $q^2$  square by 12. And if the input is sine wave ok, then the corresponding signal to noise ratio for such ADC can be

calculated as  $6.02 \times n$  where  $n$  is the number of bits, and this value is often neglected. So, more the number of bits, more is the signal to noise ratio. So, noise here is related to quantization error or also it is called quantization noise.

So, if you want to know more, you can pick up any digital signal processing basic text, where this part is discussed with a lot of details. We take this result. Just here to know that this is an important performance issue of an ADC, it is fine. And also we take note that if we increase the number of bits, then this quantization noise or this part's effect is less; signal to noise ratio is higher.

So, the other thing that is important here is the analog part of the error, and which is for which the main source is the one that is coming from the comparator, the switching that is taking place. And you have seen the various things from the comparator, we are going to this counter. And various other places, where the actual account is you know happening all right. And variation in switching happens because of this offset, gain, linearity of the amplifier—all those things, and which often depends on the input voltage, temperature, etc. So, there are some other sources. So, we shall look into them, and understand them a bit more in the subsequent slides.

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So, we begin with offset error. So, offset error is also called zero scale error. This is also known as zero scale error. What is it? So, for DAC as I said this part is common,

when we discussed DAC performance issues. This aspect we said, we will take up together with ADC.

And when we discuss certain performances of ADC in the earlier classes regarding, how fast you know it works or how many bits that can be associated with cost and other things. These are certain things, we did not do did not discuss. So, we are taking them together. So, let us see for DAC, it is the step value, when the digital input is 0. So, as I said this is related to zero scale error, so when the digital input is 0 ok, ideal case the analog output should be 0. So, this should be over here right.

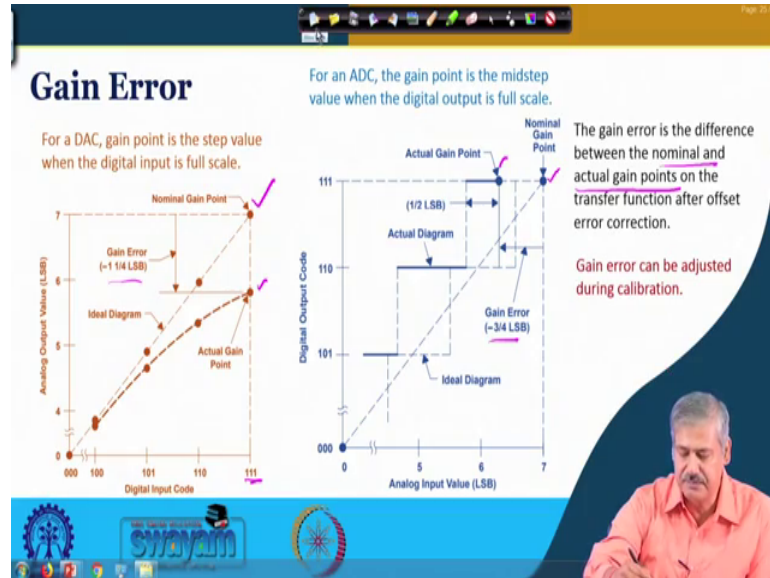
But, practical case if you find that the value is over here the value is over here ok, then there is a offset error or there is a zero scale error for the DAC. And how we measure, it we see that this value, this is the ideal line, this is the ideal line right. The digital and analog this you know mapping, it should follow this line. So, you see for what value of the this input digital code, this value is there. So, it term it in this manner. So, we can see that this is about plus 1 1 upon 4, so that is what we see over here right. So, this is the one that we see right. And accordingly, we say that the offset error is that of 1 plus 1 1 upon 4 5 by 4 LSB, is it clear right. So, this is the way it is measured this height.

Now, comes the ADC offset error right. So, ADC offset error, so again you start if it is 0, it is 0, then if you keep increasing the analog voltage, when the first transition occurs ok. So, the first transition is occurring over here. So, this is related to this offset error or zero scale error right. And the meets step value is somewhere here right, and the corresponding meet scale mixed scale value will be somewhere here. So, if you just note the difference if you just note the difference ok, so this is what will give you the offset error right, because this is following this line right.

So, either you take from this to this or you take from this to this right. So, either way you will see that it is if you just measure it, it is plus 1 into 1 upon 4 that is 5 by 4 LSB. So, in this particular example, this is like this right. And mid step is where it is your half LSB, this distance that is what we understand by mid step, is it clear? So, this is one actual diagram, and this is what we expect as ideal diagram. And the difference when it is at 0, and the first transition occurs, so that is the giving with the offset error. And offset error usually is compensated by doing adjustment in the beginning, when you calibrate the

ADC, and it is also called trimming ok. In some textbook, you will see that is same as written as trimming. So, by that process, we can compensate this offset error ok.

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Now, next what we see is called gain error right. So, the gain error is the difference between the nominal and actual gain points on the transfer function after offset error corrections. So, after off offset error was there, so we have corrected by appropriate compensation right. And then you are finding out nominal and actual gain point.

So, nominal gain points is basically following the transfer function right. So, this is for your this digital input code, and this is the analog output code. So, this is called the DSC right. So, this is where it should reach ok. But, for their full scale value, what it has gone, it has gone up to this right. So, this is your actual gain point. So, this difference is your gain error. So, in all these examples, you can see that some values have been represented values has been shown. So, here the gain is negative, so minus 1 by one into 1 upon 4, so minus 5 by 4 LSB is the corresponding value that you can see as the error ok.

For ADC, so this is again the nominal gain point. But, for this ADC, you can see that the actual gain point has come over here right. So, it has reached this place right. So, this is the difference that is the gain error, and if you calculate, you can see that this is minus for this particular example minus 3 by 4 LSB ok. So, this is the gain error again this can be adjusted during calibration trimming, and after that the ADC can be put to use ok. So,

initially we have to look at this offset error, gain error, if there is any, and then we look at how we overcome it through compensation, during calibration right.

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**Differential Nonlinearity (DNL)**

- Differential nonlinearity (DNL) error, sometimes seen as simply differential linearity error, is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB.

The counter-type and continuous-type converters usually have better differential linearity compared to successive approximation-type.

$\frac{1}{2}$  LSB DNL Limit  $\rightarrow$  Loss of 1 bit resolution

SNR (worst case) =  $6.02n + 1.76 - 6$   
 $= 6.02n - 4.24$  dB

Formulas shown on the slide:

- $DNL_k = (\text{Width}_k - 1 \text{ LSB}) / 1 \text{ LSB}$
- $DNL_k = [(O_k - O_{k-1}) - 1 \text{ LSB}] / 1 \text{ LSB}$

The slide contains two graphs: one for an ADC showing a step function with a differential linearity error of -1/2 LSB, and one for a DAC showing a staircase function with a differential linearity error of +1/2 LSB. A presenter is visible in the bottom right corner of the slide.

Next is differential non-linearity error. So, this is another important thing. So, differential non-linearity error, often it is called DNL ok. So, in some context, it is also called differential linearity, I mean it should follow linear thing, but it is not following, so it is becoming non-linear. This is the difference between an actual step width ok, and the ideal value of 1 LSB for ADC. And for DSC the actual step height and ideal value of 1 LSB ok.

So, here first ADC is you know drawn right. So, this is the way you can see an actual ADC is working right. So, this is the analog input voltage, and this is the corresponding digital code ok. So, here what you see, it should have been it should have gone from this place to this place right, then only the change should have taken place, but it has occurred earlier ok. So, this error is that of here, what you can see minus half LSB.

If you just note the difference of it ok, difference of actual step, and what 1 LSB would have given you right. In this case it should have been over here, but it has gone beyond that right, so this is plus half LSB. So, for each of these you know code, the code that is getting generated here; so, 0 0 1 or 1 0 0 ok.

So, you can have certain DNL value right. So, this DNL is associated with the code  $k$  right, it is given by width of  $k$ . So, this is the width that you can see minus 1 LSB, what is the actual width divided by 1 LSB width, so that is how for ADC that is what you can see. How DNL  $k$ , DNL for  $k$ -th code is defined, is it fine right.

Now, DNL for DAC, so this is your DAC right. So, this is your step height, and the ideal value. So, this step height should be you know what 1 LSB should give you, so this is the digital input code, and this corresponding analog output for the DAC right.

So, here what you can see that this step height is step height is from here one a particular code to another. So, the value is more than what an LSB one 1 LSB would have given. So, this is plus 1 upon 4 that is magnified, and you can see over here. And in this case it is less than that, so this is minus 1 by 4 in this representative diagram ok. And in this case, this output whatever analog output, you can see minus the previous value whatever, so that gives you the step height. Analog voltage for  $k$ -th code and analog voltage for  $k$  minus 1 code, then minus 1 LSB, what is the ideal value divided by 1 LSB, so that is your  $k$ -th DNL for the DAC is it all right.

And what we can see that the counter-type or continuous-type converters usually have better DNL characteristics compared to successive approximation type right. And if the this DNL limit is higher like that of say half LSB for such a case, we had earlier considered for the quantization noise etcetera that it is within this plus minus half LSB. Now, DNL is you know adding another half LSB because of this, then we have got a one big loss of resolution right, whatever we had considered for the you know the quantization part of it.

So, in this case the SNR, so one bit loss means basically  $6.02n$ , if  $n$  bit are used, so one bit will roughly that is  $6.02$  into  $n$ . So, roughly 16 dB less case that is happening. So, the SNR will correspond correspondingly decrease for a DNL value of that order ok, so this is something we need to take note of ok.

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## Integral Nonlinearity (INL)

- Integral nonlinearity (INL) error, sometimes seen as simply linearity error, is the deviation of the values on the actual transfer function from a straight line.
- INL is the summation of DNL from the bottom up to a particular step.

$INL_k = V(\text{ideal})_k - V(\text{actual})_k$

The absolute accuracy or total error of an ADC is the maximum value of the difference between an analog value and the ideal mid-step value. It includes offset, gain, and integral linearity errors and also the quantization error.

And from there, we go to something which is called integral non-linearity ok. And corresponding error is called INL error integral non-linearity error ok. And what is it, this is the deviation of the values on the actual transfer function from a straight line ok. And so let us see, how it is looks like, so this is the ADC right. So, this is the analog input value, and the corresponding digital code right.

So, this is the your this ideal you know transition the dotted line, and actual is the bold line that is what you can see right. And what you can see these, the deviation occurring over here ok. So, the deviation occurring over here, so these are the different deviations ok. And if you can measure that is happening from the actual transfer, the straight line that is happening for the actual transfer function. So, these are the different values minus of LSB minus 1-4 LSB or so.

And for DSC, so this is your ideal, and this is your actual ok. For any you know digital code any k-th code, you can see what is the you know actual value, and what is the ideal value the difference that is giving you INL error this is giving you INL error ok. These are the some examples that you can see ok.

Now, we have already seen DNL error. So, if you add them up, up to a k-th point from the beginning, then you get the INL error of that particular value from beginning up to that particular state ok. So, it is summation of those values right. And so from this



definition, we have already seen the ideal. And actual if you subtract, you get the INL for both the cases ok.

And then there is another term called absolute accuracy or total error of an ADC, which is the maximum value of the difference between an analog value and the ideal mixed up value, the one that you have seen the maximum of it. It includes offset gain integral naught linearity errors, and also quantization errors. So, all those things included, what you come up with is called the total error or absolute accuracy. So, these are certain important (Refer Time: 18:39) matrix matrix or issues that we need to take note of when we talk about ADC and DAC ok. Other than how many bits, it requires and the time requires for conversion and all ok. So, these are also issues by which one has to pick up one from the other.

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**ADC 0804**

- 8 bit, successive approximation type.
- Analog input range, 0 to + 5V.
- Single power supply, usually 5 V.
- Pin 9 is input ref. voltage, if left open it is internally set at  $V_{CC}/2$ .
- Output TTL and CMOS compatible.
- Frequency of internal clock  $\approx \frac{1}{1.1 \times RC}$   
 $f = 1/(1.1 \times 10 \text{ k}\Omega \times 150 \text{ pF}) = 607 \text{ kHz}$
- Conversion time  $\approx 100 \mu\text{s}$
- Total error (maximum)  $= \pm 1 \text{ LSB}$   
 8 bit, eqv. to  $= 5/2^8 = 19.53 \text{ mV}$
- Output tri-stated.

00000000:  $0V_H = 0 \text{ V}$   
 11111111:  $5V_H = 5 \text{ V}$

Now, we look at one particular ADC, because you have not discussed any ADC circuit IC example in the previous classes. So, we take this opportunity to introduce ourselves with ADC 0804 ok. So, this ADC 0804 is popular of when you use it in the lab ok, so this is a 8 bit ADC. So, this is 8 bit ADC right. And this is successive approximation is not it?

And the analog input voltage range that you see over here is 0 to plus 5 volt ok. As such, but we shall see how we can increase, when you can change it ok. This is the input reference voltage as it is it is you know on it own internal it is set by  $V_{CC}$  by 2 right,

this is your V<sub>CC</sub>. If you want to set it to a different value, we shall see, how it can be set. Output is TTL and CMOS compatible ok.

Frequency of the internal clock is given by this formula and R and C, you can if you put in this manner 10 kilo ohm 150 Pico farad; these are some standard value. So, the f is 607 kilo hertz right, conversion time is roughly 100 microsecond. And total error maximum that we have discussed is plus minus 1 LSB ok, and a so that is if you are talking about this 5 volt reference and all. So, in terms of voltage, so this error becomes 19.53 volt or so plus minus 19.53 milli volt error. So, output is tri stated ok. And if this output is all 0, so you get 0 volt; if all 1, you get 5 volt right.

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**Span Adjustment**

$V_{ref} = 2.5 \text{ V}$  allows full scale for input 0 to 5V

By making  $V_{ref} = 1 \text{ V}$  full scale utilized for input 0 to 2 V.

Resistive divider:

$$V_{ref} = V_{cc} \frac{R_2 + R/2}{R_1 + R_2 + R}$$

LSB is equivalent to  $2 \text{ V} / 2^8 = 7.8 \text{ mV}$

0-5V  
0-2V

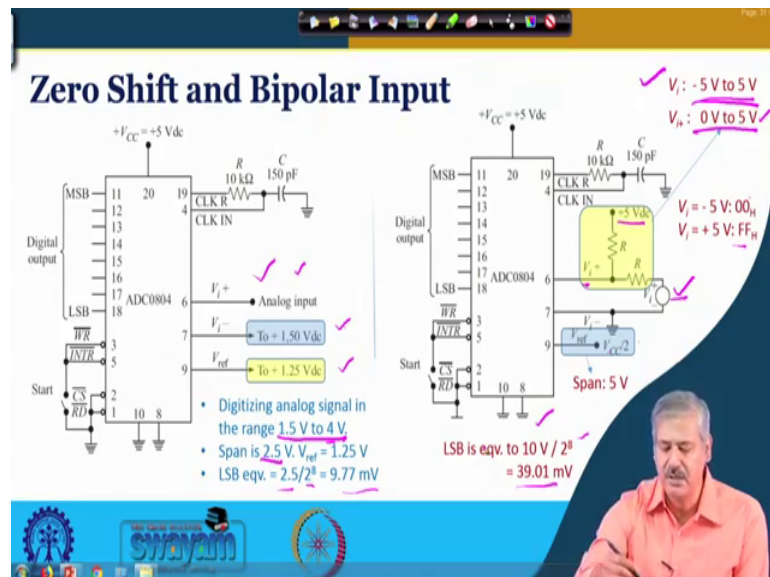
Now, what we discussed is the span adjustment ok. So, what is it, so let us see, so in this case here earlier it was 2.5 volt right, v reference was 2.5 volt. And the input voltage that was getting analog input voltage that was getting converted to digital equivalent was 0 to 5 volt right.

Now, if you make this V reference 1 volt ok, then the full scale becomes 2 volt and the small value the lowest value remains 0 volts. So, this span which was 0 to 5 volt, now becomes 0 to 2 volt ok. So, all 1 is now 2 volt. Earlier all 1 was 5 volt, now all 1 will be 2 volt ok. So, this is useful, so that you can utilise the entire range. So, all the beats to encode and analog signal which is having a lower range right, otherwise it will use lesser number of bits ok.

So, accordingly the quantization noise will be reduced ok. If you use the full range of all the bits that is available ok. And to get that particular reference voltage of course, you can use a resistor divider circuit something like this right. And generate reference voltage which is 1 volt DC ok. And if you do that, you will get 0 to 2 volt.

So, in this case the 1 LSB is equivalent to what, so 2 volt is the entire range right. So, 2 volt by 2 to the power 8, so 7.8 milli volt ok, which is a better proposition. If you had stuck to this one, then your this value you had seen it is around 19 milli volt or so, the resolution would have been worse fine.

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So, so we look at other aspect of it. So, if you want to have a zero shift ok, so what is it? So, in this case, so let us look at one such you know configuration right. So, here this is your this analog input right. Now, this is connected to 1.5 volt right V reference is 1.25 volt. So, V reference is 1.25 volt means the span is twice of that. So, 2.5 volt is this span right. So, this is 2.5 volt right. So, this  $V_i$  minus the voltage you have connected as 1.5 volt. So, this 1.5 volt and the span is 2.5 volt. So, the lower range is 1.25 volt. So, 1.25 plus sorry 1.5 plus 2.5 right, so that is 4 volt.

So, analog input now is going up to you know 4 volt ok, so that is the range 1.5 volt to 4 volt that you can do through this particular arrangement ok. So, zero shift means earlier it was the low lowest value was zero right. So, if it is 0, then it is it will do with this kind of

reference voltage 0 to 2.5 volt ok. With this arrangement, now it will do it will convert from 1.5 to 4 volt ok.

So, LSB equivalent since the span is 2.5 volt, so  $2.5 \times 2^8$ , so 9.77 millivolt is the LSB equivalent or the resolution that you can get fine. And can we use bipolar input. So, earlier we had seen you know all the inputs in earlier examples from you know zero to some other value or 1.5 to some other higher value the positive value. So, here is an example where we see that how we can use a bipolar input ok. So, the  $V_i$  in this case is minus 5 volt to plus 5 volt right, minus 5 volt to plus 5 volt right. So, this is your  $V_i$ .

And we connect a circuit like this a plus v 5 volt dc supply and a resistance you know network like these. So, in this case through this resistance divider you know network and all. So, if you calculate, you can see this  $V_i$  plus, when  $V_i$  changes from minus 5 volt to plus 5 volt, this  $V_i$  plus changes from 0 volt to 5 volt right. And then we are in the business, your this span is this is 2.5 volt, so this whole span 5 volt that we get. So, this is your span of 5 volt ok. And so this is your minus 5 volt will be your 008 and plus 5 volt will be your all 1 FF in x H means x right.

Now if you look at it from this  $V_i$  point of view right then the entire range is 10 volt right. So,  $10 \times 2^8$ , so 39.01 millivolt is the 1 LSB equivalent or the resolution that you get for this particular circuit is it right. So, these are certain important aspect. So, other things that are associated with this ADC operation that you can start by you know pressing this switch and all. And there are this interrupt and various other you know inputs are there when you are using it with a microprocessor or other circuit. So, we can make use of them, but basic ADC operation, the functioning the conversion of analog to digital, so that we have just discussed these are the control inputs as and when you use it, you find out from the data sheet and make use of them ok.

(Refer Slide Time: 27:59)

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill
- <http://www.ti.com/lit/an/slaa013/slaa013.pdf>
- <http://www.ti.com/lit/ds/symlink/adc0804-n.pdf>

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Conclusion:

- In ADC, the source of error comes from both digital and analog part. Digital part error is related to quantization.
- For an ADC, offset error is found by giving zero to analog input and increasing it till first transition occurs. For DAC, it is the output when digital code is zero.
- The gain error is the difference between the nominal and actual gain points.
- Differential nonlinearity (DNL) error is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB.
- Integral nonlinearity (INL) error is the deviation of the values on the actual transfer function from a straight line.
- ADC 0804 is an 8-bit successive approx. ADC providing useful options such as span adjustment, zero shift etc.

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So, with this we conclude and what is we have seen that in ADC the source of error comes from both digital and analog part. And digital part error is related to quantization. And in ADC offset error is found by giving zero to analog input and increasing it till first transition occurs. For DAC, it is the output when digital code is zero ok. The gain error is the difference between the nominal and actual gain points. And we have seen it how it is calculated for both ADC and DAC.

DNL error we have seen is the difference between actual step width for an ADC and step height for DAC and the ideal value for 1 LSB ok. INL error, INL error also we have seen and this is the deviation of the values from the actual transfer function from a straight line ok, the ideal transfer function so that you also you have noted. And finally, we have seen how ADC 0804 is you know works, and how we can use it for different kind of operation by using span adjustment zero shift even for bipolar signal, analog to digital conversion ok, so all these things we have seen ok.

Thank you.