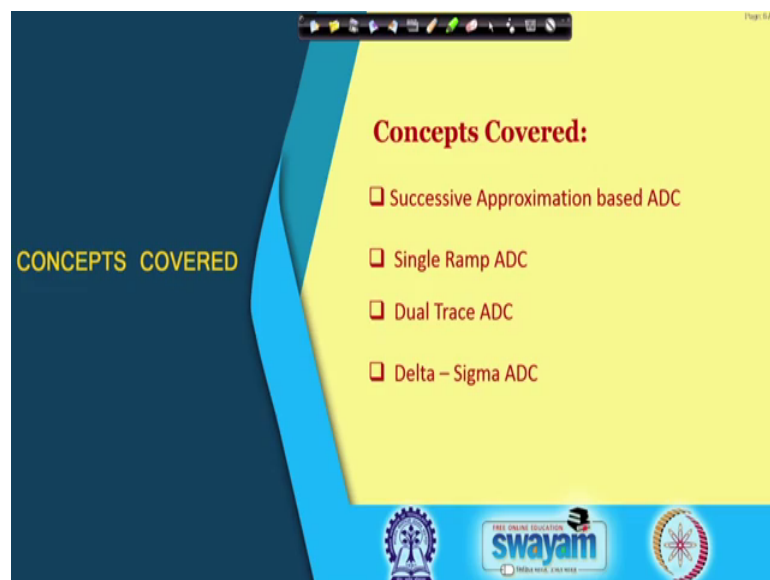


Digital Electronic Circuits
Prof. Goutam Saha
Department of E & EC Engineering
Indian Institute of Technology, Kharagpur

Lecture - 54
Analog to Analog Conversion – II

Hello everybody, we started the discussing Analog to Digital Conversion and we had seen certain type of techniques by which analog signal can be converted to digital equivalent ok.

(Refer Slide Time: 00:28)



We shall look at few more techniques like successive approximation based ADC, ramp based ADC, single ramp dual trace then text double ramp and delta-sigma, often it is also called sigma delta ADC.

(Refer Slide Time: 00:47)

Successive Approximation

Continuous A/D Converter is not advantageous if input is multiplexed. For that, successive approximation is suggested.

- Successively divides voltage ranges in half.
- n -bit register is first reset.
- Then, MSB is set to 1.
- DAC output is compared with input by a comparator.
- From comparison, MSB Flip-Flop remains set or reset.
- Second MSB is set to 1.
- The process is repeated.

Example:

$$\frac{10 \times V_{ref}}{16} \leq V_A \leq \frac{11 \times V_{ref}}{16}$$

So, in the last plus when we ended, we discussed that continuous approximation, continues tracking type of ADC is good, but the problem with that is if multiple input is there; I mean, that need to be converted using a multiplexing kind of scheme, then it is not very suitable because it locks loses the tracking part of it and it is begin from the beginning which is not very advantages.

So, people thought about some other method; one such method is called successive approximation right. So, in this case for, what we do? We follow a scheme which is illustrated in this particular diagram. So, let us see how it works. So, when it begins the countered that we have with us which stores the final value. So, that counter is initially reset with all 0 ok. So, this is the beginning of it right. Then control logic is such that the most significant bit of the counter is set to 1; most significant bit of the counter is set to 1 right. So, in most significant is bit is set to 1; so, in this particular case say it becomes 8.

So, the corresponding DAC output the corresponding DAC so, this counter will go through this ladder and other things and all and DAC output you know in digital (Refer Time: 02:32) it will be generated. So, that will be compared with the analog input that will be compared with the analog input. So, this MSB 1 is basically whatever is the full range your dividing into half right, the range is now made half. So, the half key voltage so, these if the full range is V . So, V by 2 is now getting compared with the analog input

voltage right. So now, if V_{in} is greater than $V_{ref}/2$ so, then you go this way and if V_{in} is less than $V_{ref}/2$ you go the other way ok.

Now, if V_{in} is greater than $V_{ref}/2$, what does it mean? The counter the digital equivalent is more than this value which is now currently stored in the register so, 1 triple 0 is not enough right. So, then what you will do, you will look at now second MSB.

So, you will make the second MSB 1, when such a situation occurs, but if V_{in} is less than $V_{ref}/2$ what will happen? So, this voltage what is stored in the counter is more than the input voltage right. So, what do you do, you make this 1; this MSB which was 1 we reset it ok. So, it becomes 0 and we make next MSB 1 is it fine.

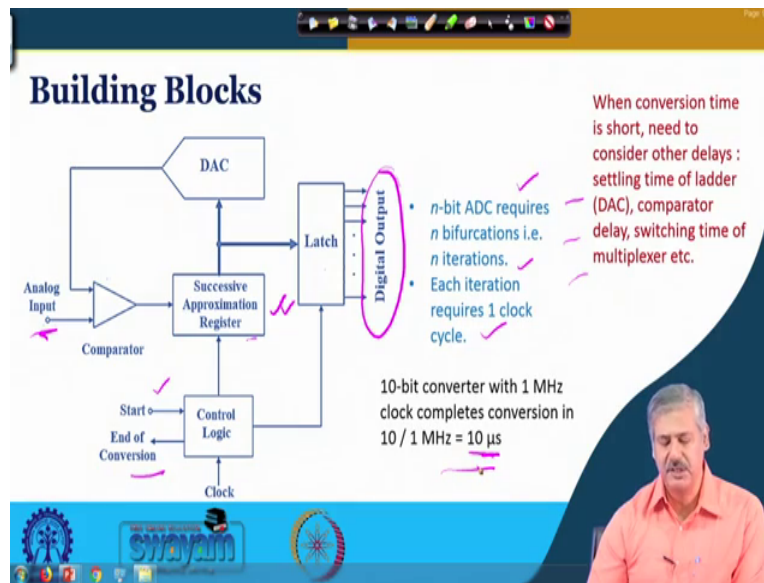
So, this is done in this comparison and setting the value will be done in 1 clock cycle right. So, next when it is 1 1 0 0 this is the 1, again we do a comparison; similar comparison if the input voltage is more than that will go this direction and if the input voltage is less than that we shall go in this direction. So, this is how it goes on and we can see one example then it will be clearer. So, this is the marked in this yellow right. So, the input voltage is in between what about the reference voltage that we were talking about within 10 upon 16. So, this fraction is because 4 bits, 1 up on 16 is the fraction and 11 so it is within this value ok.

So, then of course, it is more than 8 so, it go this way. So, it is less than 12, so it go this way then it goes in this direction 1 0 1 0 right. So, it is more than that, more than 10 into V_{ref} ok. So, it goes in this direction ok. So, when it is more than this direction so, there are two possibilities, 1 0 1 1 and 1 0 1 0 right and then it has become 11. So, this is your 11, but it is less than 11. So, finally, this is what is it clear.

So, same thing what we were discussing, the same example, similar example you can take up and understand how this is achieved or this is achieved right or this is achieved right. So, this is one such example right and the first value will be 0 0 0 0 means this is 0 into 0 voltage and V_{in} is the input voltage is $V_{ref}/16$.

So, that is all 0 case and rest of the cases are like this fine. So, if you have understood this, then rest of the things are simpler.

(Refer Slide Time: 06:13)



So, whatever we have discussed this same thing is now put into this logic block right. So, this is the successive approximation register where these you know these MSB's are successively set right and this is the control logic. So, that is it is just you know this initial start signal comes right and the first is MSB's set, the corresponding DAC takes the output and compares with the analog input, the way we are looking at example right. And when the end of conversion risked the signal is made out, comes out and you know next conversion can get initiated and at that time whatever is stored in register is finally, latched right and that is the corresponding digital output ok.

So, n -bit ADC will require n bifurcations, the one that we have just seen; so that means, n irritation will be required and each irritation required 1 clock cycle right. So, when 10-bit converter with 1 megahertz clock, if where thinking about then the conversion is completed in to 10 microsecond ok. Each clock requires 1 micro second so, 10 clock cycle means 10 microsecond ok.

And here we need to take note that when we are considering conversion time which is very small, very short then other delays which are there in the circuit like settling time of ladder, comparator delay, switching time of multiplexer all those things need to be counted ok. And, together the actual conversion time whatever we are talking about this is you know becomes off significance right ok.

So, that was successive approximation register is very successive approximation based ADC which is very popular, it is inherently low cost.

(Refer Slide Time: 08:21)

Use of Ramp Signal

DAC used at the input of comparator in ADC design is driven by binary counter / register and generates staircase waveform.

$v_o = -\frac{1}{C} \int i dt = -\frac{V_i}{RC} \times t$ when $V_i = \text{constant}$

Slope = $\frac{V_i}{RC} = \text{constant}$

Constant slope is a key requirement.

Now, we look at another method where we are using ramp signal ok. Now, it has got certain advantage, it is little bit slower lower, but it has got certain advantage which we shall discuss little later. So, first of all see how it works ok? So, this is a op-amp OA stands for Op Amp ok, this is op amp right and this is working in a integrated mode right and then the output of it is given by this formula.

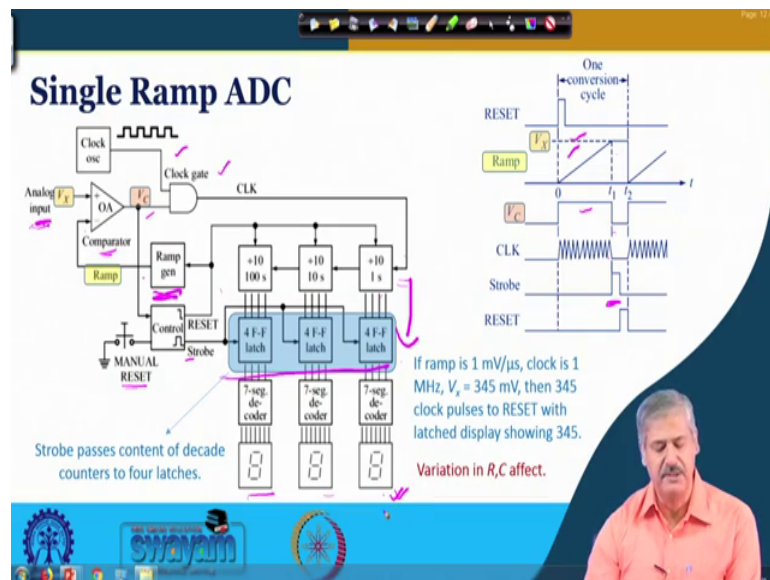
So, basic op-amp, analog electronics or basic electronics that you have studied so, you have seen such configuration. So, the output is something like this right and it with this is analog input which is remaining constant when you are trying to make use of it in the it would be conversion. Remember that in all these cases because of this requirement for each of these ADC type we are talking about a sample and hold. So, analog voltage is there to sample it and hold it in a capacitor, the one that we have you know similar thing we have discussed in DAC ok. So, that the input remains stable for during the time of conversion, it does not change then you know the output will become ironies so, that part we consider that is there.

So, this V_i is we can consider as constant during the conversion time. And, what is happening, when V_i is constant? So, with respect to time RC is constant. So, it changes like this it increases like this ok.

Now you see this wave form if we send it to a comparator, compared to the kind of waveform we had send before earlier you know from the DAC through the counter. So, those where staircase kind of you know wave form right and this is a continuously increasing kind of thing. So, this is something which we take note as a difference, if we are using this in a ADC design right.

Now so, this slop is like this, V_i by RC which remains constant ok. But one issue is there, when we are using this time for the calculation of the digital equivalent that this ratio should not change, but if you know R and C value changes with you know temperature or some environmental condition and all. So, then this kind of arrangement becomes a bit problematic ok.

(Refer Slide Time: 11:07)



So, that we know in order limitation and how we can make use of it so, here is a single ramp ADC arrangement. So, initially these are the decade counters, this 3 are decade counters that you can see right. So, initially when you start so, it is it reset ok. So, these counters are already set you can see this reset signal going there ok.

And after that so, this is your this comparator and this is the ramp generator, the circuit that you have just seen ok. So, this particular ramp generator is initially reset and then it is you know generating the ramp, the way you see over here and this is your analog input voltage so, this is your V_x and whenever this ramp voltage goes up to this then the comparators (Refer Time: 12:10) ok.

So, this comparator is remaining high because analog input voltage is higher than the ramp output which is at the negative terminal of the comparator, inverting terminal of the comparator.

So, this is remaining high and whenever it exceeds it, it goes low ok. So, when it goes low the clocking stops, you can see this is the you know clocking to the counter. So, the clocking to the counter stops is it fine.

So, whenever as long as it is remaining high, this V C is remaining high; that means, ramp output is less than the analog input voltage, the clocking comes here and counter starts counter is increasing, note that this counter value we are not using through DAC for comparator, we are using the ramp instead ok. So, this counter output is not fed through a DAC to be comparator or like the previous case. So, the counter output is actually going in this direction to come up with the digital equivalent of the analog input right.

So, once you know it reaches, it reaches this particular point and these clocking gets stopped right; so, this is what you see the clocking gets stopped, a strobe signal is generated by the control logic ok. So, this strobe signal that you see over here, it latches the latches these counter output to a set of flip flops ok. So, that is what you see over here right.

So, it will remain latched till the next strobe signal comes ok. And this output; now through a 7 segment display 7 segment decoder, it goes to 7 segment display and the counter output which is the digital equivalent ok, we shall see an example of the analog input that will be displayed over here ok, that will be displayed over here.

So, let us see how you know you know it works out with using some numbers. So, if your ramp is 1 milli volt per micro second so, that is the kind of ramp you are having and clock is your 1 megahertz the clock is 1 megahertz and V X is 3.45 milli volt.

Then how many clock pulses will be required? So, 345 clock pulses will be required to reset, is it fine right? So, V X is 345 milli volt; so, 345 you know this micro second of time will be required 1 millivolt per microsecond and we are considering the clock is as 1 micro hertz, 1 megahertz ok. So, then each clock is 1 microsecond so, 345 millivolt; 345 micro second and 345 clock in that will be happening here. So, this particular

counter we will show 345 value and that is getting latched and it will come over here this is it clear.

So, you have to set these values appropriately or a proper decoding or mapping need to be done if the other values are set ok. But, as I said that in these cases these ramp, the slope is key and the value of R and C is something need to remain constant, if that varies then 345 will becomes 346, 347 or you know less ok. So, that is a cause of concern that we will conclude to the error.

(Refer Slide Time: 16:19)

Dual Trace ADC

The slide contains a graph on the left showing two ramps. The first ramp starts at 0 and goes down to $-V_C$ over a fixed time t_1 . The second ramp starts at $-V_C$ and goes up to 0 over a fixed time t_2 . The slope of the first ramp is $V_C = \frac{V_X}{RC} \times t_1$ and the slope of the second ramp is $V_C = \frac{V_r}{RC} \times t_2$. The word "Fixed" is written in orange above t_1 and below t_2 .

The circuit diagram on the right shows an integrator op-amp (OA) with a resistor R and capacitor C. Its non-inverting input is connected to an analog input V_X through a switch. The inverting input is connected to a reference voltage V_r through a resistor. The output of the integrator is connected to a comparator (OA). The comparator's other input is connected to a control signal. The comparator's output is connected to the switch.

Formulas and notes on the right:

$$\frac{V_X}{RC} \times t_1 = \frac{V_r}{RC} \times t_2$$

$$V_X = V_r \times \frac{t_2}{t_1}$$

- V_r and t_1 are constant.
- t_2 value varies as per V_X .
- Variation in R, C values cancel out.

So, what people have thought off? In such a case that use of dual trace analog to digital converter ok. So, here what is happening you can see, that in the beginning so, if this is the circuit. So, this is the analog input voltage right now the first the ramp is generated this part, this is inviting so, the ramp will be in the negative direction right. So, this is the integrator op-amp that you can see have seen before so, this depending on this V_X for a fixed time t_1 , the ramp is generated.

And depending on this V_X value so, it will come here or here or you know in some other place. So, this is what is deciding the slopes V_X by RC V_X by RC ok, if V_X is more or V_X is less so, this point will be different ok. Right now, it is here, it will be here or it will be here, is it fine. So, that is the first part.

So depending on this thing, it will come somewhere here and after that this term; so, t_1 is fixed right. And then what happens? It switches to a reference voltage so, this is a fixed reference voltage, so this is a negative reference voltage ok. So, this is negative means and this is a negative right so, negative it is becoming the positive; so, it will now going upward direction right.

So, here it is starting from here, if the V_X was less it will start from here, V_X was more it will start from here, but in this case the what is that called? This reference voltage is fixed. So, it will take different point of time. So, if it is starting from here, it is taking this t_2 , if it is starting from here because this slope is same it will reach over here at a smaller t_2 , it starts from here it will reach there at a larger t_2 . So, this t_2 gives me an idea about what the V_X was, right and if we get a digital equivalent of t_2 so, that is something can be you know shown as a representation of the analog input voltage.

So, this is what is considered over here and what is the benefit? Of course, time required another thing is one aspect because we are always you know this making t_1 , so it is not it is not need to go to the you know the maximum value of the V_X . So some fixed value, some fraction of V_X is sufficient all right. And the other thing over here, you can see the relationship so this is it is going up to V_C is V_X by RC into t_1 and for the other case V_C is equal to V_R by RC into t_2 , this is reference voltage we are talking about right.

So, when you are you know putting them together. So, the RC and RC in the either side cancels out and this is the relationship that you are getting. So, V_R is known the reference voltage and t_1 is also known so, V_X we can get from t_2 .

So, this RC at one side, if there is small you know variation of R and C because of temperature and another things, the same way it will affect the other side also. So that way, this variation part is taken care of in some sense in this particular arrangement right. So, this is what we can see in dual trace ADC right.

(Refer Slide Time: 20:03)

Dual Trace ADC

- When the counter reaches the fixed count at time t_1 , the CONTROL unit generates a pulse to clear the decade counters to all 0s and switch the integrator input to the negative reference voltage V_n .
- The counter at the end of the conversion cycle stores t_2 (clock is disabled).

Consider, 1 MHz clock, $V_n = -1$ V, $t_1 = 1000$ μ s, RC time constant = 1.0 ms, $V_p = 1.25$ V.

In time t_1 , $V_c = -1.25$ V
During t_2 , slope = 1 V/ms
 $t_2 = (1.25/1)$ ms = 1250 μ s
requires 1250 clocking.
Counter shows 1.250

So, here if we look at the arrangement, the dual trace ADC circuit arrangement. So, certain things we can see which in the which is similar to you know single trace ADC, single slope ADC that we had seen before. So, this is the latch ok, this 7 segment display the 7 segment decoder driver, display, this is strobe of it so whenever this count as been completed.

So, initially what you see? This is the count of you know t_1 the fixed time that is taking place right and this is the control block which is doing the switching. So, from V_x to reference voltage and from this comparator ok. We can see the clocking will take place, the way we had seen it before and the final circuit will be will put it would look something like this ok. And we actual counting which is happening for t_2 right so, this is the one, similar to what we have had seen in case of previous single ramp arrangement ok. So, now the comparator is now comparing with 0 because it is coming down and then going up right.

So, this is a fixed 0 over here compared to the analog voltage input that had in the previous case ok; in single ramp case. So, rest of things are similar for this part of the circuit right. So, the disabling of clocks all things are similar the way we had seen it before in the control logic right.

Now if you take an example, some numbers how it looks like. So, if you consider a 1 megahertz clock; that means, 1 microsecond is the time period and the reference voltage

is say minus 1 volt, t 1 is fixed say 1000 microsecond, reference voltage is also fixed and it is negative. So, minus 1 voltage we are taking about and RC time constant is 1 millisecond, and the input voltage that the analog input voltage that we were trying to convert to digital equivalent is 1.25 volt, then how it works? So, time in time t 1 so, V C becomes because of this time constant 1 millisecond. So, it will go to minus 1.25 volt, you can calculate right and for the t 2 slope is this is 1 volt right; so, 1 volt per millisecond because of this time constant 1 volt per millisecond ok. And then the t 2 will be requiring so, from 1.2 volt, minus 1.2 5 volt it has to go to 0. So, 1.25 divided by 1; so, 1 2 5 0 micro second.

So now the counter, this counter will be having 1 2 5 0 value because so many clocking has taken place each clocking is 1 microsecond right. So, at the output of it, when it is, you know strobe comes and latched it will show 1 here 2 5 0. So, the output if there is a decimal points, so 1.25 ok; so, volt that it will show. So, this is the way it will work, but if for some other value according you know corresponding mapping need to be done.

Now, one important issue that I told that though it is slower so, this integrated type of approach, but because of this integrating action at the analog input voltage ok, if there is any noise or so, that gets averaged out ok. For which these are considered these kind of you know ADC are found to be more accurate and multi-meter, voltmeter construction etcetera these measurement purposes we have seen that these are used.

(Refer Slide Time: 24:28)

Delta-Sigma ADC

CK	A	C	D	E	B
0	5/8	0	0	0	0
1	5/8	5/8	5/8	1	+1
2	5/8	-3/8	2/8	1	+1
3	5/8	-3/8	-1/8	0	-1
4	5/8	13/8	12/8	1	+1
5	5/8	-3/8	9/8	1	+1
6	5/8	-3/8	6/8	1	+1
7	5/8	-3/8	3/8	1	+1
8	5/8	-3/8	0/8	0	-1
9	5/8	13/8	13/8	1	+1
10	5/8	-3/8	10/8	1	+1
11	5/8	-3/8	7/8	1	+1
12	5/8	-3/8	4/8	1	+1
13	5/8	-3/8	1/8	1	+1
14	5/8	-3/8	-2/8	0	-1
15	5/8	13/8	11/8	1	+1
16	5/8	-3/8	8/8	1	+1

- Input needs to be oversampled (=100 times)
- Works well for slow changing signal
- High resolution possible but low speed

Average = (13 - 10) / 16 = 5/8

A Comparison

Delta-Sigma: 8-32 bits, <1MS/S
Dual Trace: 12-20 bits, <100 S/S
Suc. Approx.: 8-18 bits, <10MS/S
Flash: 4-12 bits, <10 GS/S

Flash: expensive, high power
Dual Trace: noise immune (use in digital voltmeter)
Suc. Approx.: Low cost

Note: Technology is changing fast and accordingly, limits.

We shall the last topic on ADC we shall discuss is called delta sigma ADC or sigma delta ADC. It has got more analog component than digital or digital circuit digital electronic circuit. But still it is, what discussing and there are methods also like pipeline ADC, but that is under scope we wanted to have you know fairly good idea about how this ADC and DAC works.

So with this we shall conclude this part of the discussion. So, let us see how it works; so in these, this is the analog input and this analog input is compared with a voltage which is coming from 1 bit DAC ok. So, you need to go through this example which will be which will make it clear how it works right and this has got a reference plus V or minus V right, and in this example we have taken it as either plus 1 volt or minus 1 volt.

So, this is now I mean this is a you know comes as a negative feedback. So, difference of this is coming over here. So, this is point C right and then it is integrated and then there is integrator and then there is a converter, which is this converter clock which is this particular system in a over sample systems. So, for a analog signal, there is a particular sampling frequency that is required from coming from the Nyquist rate. So, it is over sampled to the extent of you know almost 100 times right for this kind of conversion and because of which this requirement it works well for slow changing signal, but we can get high resolution ok.

So, more of this internal aspect of it, the background theory will be clearer to you; when you study digital signal processing and those aspect, but for this particular course from the digital electronics point of view. We take note of what we mean by over sampling? Ok That is much higher than the sampling Nyquist sampling rate that is there right. And this comparator output is now coming back to this DAC right.

And since it is a oversampled case right, if you want to come back to the normal sampling to use it with rest of the circuit, other part of the circuit. Then it needs to be decimated; that means, for every n sample one signal, one sample is taken that is the process of decimation and for that we need to put a digital filter before that ok.

So, these are as I said these are part of some advanced study that you can take up later ok. This we are discussing here for this sake of completion since you have taken ADC right. So, this is the whole arrangement and let us see how it works; this example will

make it clear right. So, let us consider that initial voltage that you would like measure say 5 by 8 volt.

So, initially all are you know reset this latch and other things so, these are all 0. So, the first is 5 by 8 volt, then this since it is 0, 5 by 8 minus 0, this C is also 5 by 8 ok. Then if you integrate so, earlier value was 0. So, C so this value is also 5 by 8 now, this is more than the reference voltage of the comparator so, the output is 1 output of here is 1 ok.

So, this is coming as 1 so, this is 1 bit DAC so this is 1 bit DAC; so it will take because it is 1, it will take plus 1 volt here. So, this is how the first row is C ok. Now, this is plus 1 volt; so, this plus 1 volt and this is your 5 by 8. So, plus 1 volt is coming as a minus; so, this is your minus. So, 5 by 8 minus 1 so, minus 3 by 8; so, earlier it was 5 by 8 over here. So, it is getting integrated; that means, added up; so, 5 by 8 plus or minus 3 by 8. So, the result is 2 by 8, 2 by 8 is still more than ground 0. So, this is still plus 1.

So, if it is plus 1 so, this is the DAC. So, output will be 1 so, output is 1 over here. So, this output is this is fixed 5 by 8 volt that you know we are trying to convert. So, this 1 is coming over here so, 1 and this is 5 by 8. So, if you subtract it will becomes again minus 3 by 8; so, this is minus 3 by 8 and earlier it was 2 by 8 this integrator. So, if you add them together so, it is minus 1 by 8.

Now, in case minus 1 by 8, the comparator output is 0 ok. So, this is what you can see over here and when it is 0 right for this DAC, we are this is negative reference voltage that is minus 1 volt it is coming over here. So, if it is minus 1 volt ok; so, minus minus plus so 5 by 8 plus 1 so, it will becomes 13 by 8 so, that is over here. So, 13 by 8 earlier it was minus 1 by 8 so, it is getting integrated so, it is 12 by 8.

So 12 by 8 means, again it is more than your 0 so, this is what? This is plus 1. So, this way it continuous you understand, you can you know for this is for 5 by 8 any other voltage 3 by 8 or 4 by 8 anything that you can you do in a same manner and when you do it these are the you know you know these 0's and 1's that is that you are getting. So, as you said this is 1 bit ADC that you can see and this is 1 bit DAC right.

So, these this series if you consider, if you just take a average of this output over here ok, for large number of these values, then you will see this average value is close to this analog input ok. For example, you have taken 16 such cases; so, in this case plus 1, you

can count as 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13 and minus or 3. So, total is 13 into 13 into minus 1 divided by 16. So, you can see the 10 by 16 that is 5 by 8 ok. Here it is coming exactly the same ok, but it will be coming close depending on the fraction and other things you take large number of this thing.

So, you will come to the approximation of this and this output this 0 1's ok. So, this density of 1's so, how many 1's are there ok, that from that you can get the idea of the analog input that is there ok. So, this is how this delta sigma ADC or also it is called sigma delta in some you know text so, it works more of it you will learn, in some other course, in some other context ok.

So, a quick comparison I said that, some numbers we shall see, but remember this numbers are changing with that you know the technology landscape very quickly. So, delta sigma it is high resolution is possible. So, 8 to 32 bits conversion is there and the speed of conversion the number of sample per second is in the order of maximum is 1 mega sample per second.

Dual trace 12-20 bits, but it is slower you can see, that is much slower, but it has the capacity of this noise immunity, I mean you know the handling the noise ok; so, that is the good thing about it.

Successive approximation 8 to 18 bits, but 10 mega sample per second this much faster ok, but number of bits is this less ok. Flash number of bits are a bit smaller 4 to 12 bits for 10 Giga sample per second. So, it is very fast that we had seen and we expect also and of course, it is costlier right.

(Refer Slide Time: 33:32)

References:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill
- <https://www.digikey.com/en/articles/techzone/2018/apr/match-the-right-adc-to-the-application>

The slide features a dark blue background on the left with the word 'References' in a yellow, stylized font. The main content area is yellow. At the bottom, there is a blue banner with the Swayam logo and the text 'FREE ONLINE EDUCATION swayam'. A presenter in a pink shirt is visible in the bottom right corner.

(Refer Slide Time: 33:33)

Conclusion:

- Successive approximation type ADC overcomes the limit of continuous type ADC when converting multiple inputs. It successively divides voltage range in half.
- n -bit successive approximation type ADC requires n clock cycles for conversion.
- Slope of single ramp ADC is highly affected by variation in R and C .
- The integrator of dual trace ADC averages out noise and shows better noise immunity. However, it is slower.
- Delta- Sigma ADC needs to oversample the input and works well for slow changing signals. It provides higher resolution but at slower speed compared to successive approximation and flash ADC.
- Flash ADC is fastest but takes more power, costs more.

The slide features a dark blue background on the left with the word 'Conclusion' in a yellow, stylized font. The main content area is yellow. At the bottom, there is a blue banner with the Swayam logo and the text 'FREE ONLINE EDUCATION swayam'. A presenter in a pink shirt is visible in the bottom right corner.

And with this we come to the conclusion and very quickly we have had seen that successive approximation type ADC overcomes the limit of continuous type ADC when converting multiple inputs. It successively divides voltage range in half, n -bit successive approximation type ADC requires n clock cycles for conversion. Slope of single ramp ADC is highly affected by variation in R and C and dual trace ADC average is noise and shows better noise immunity. However, it is slower. Delta-Sigma ADC needs to oversample input and works well for slow changing signals ok. It provides higher

resolution, but slower compared to successive approximation type and flash type ADC.
Flash type ADC is fastest, but takes more power and cost more.

Thank you.