Digital Electronic Circuits
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Lecture - 53
Analog to Analog Conversion - I

Hello everybody. In this class, we start discussing Analog to Digital Conversion.

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So, in this we shall cover these concepts. So, simultaneous conversion and use of this method for flash converter type analog to digital converter ADC. And then we shall discuss counter based conversion and also continuous conversion ok. So, these are the 3 things that we shall take up in today's class.

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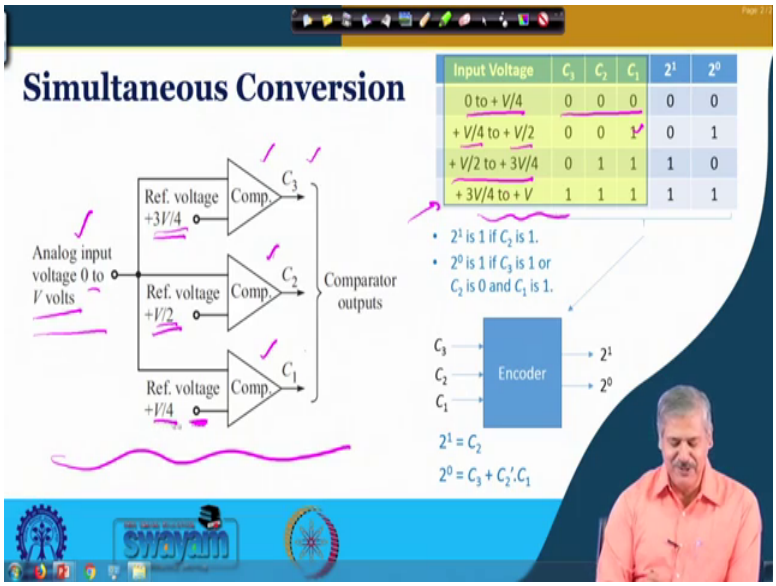

So, first we try to understand the concept of simultaneous conversion ok. So, for which we look at 1 small example, what you see in the left hand side. So, there is an analog input voltage, which is restricted to which is restricted in the range 0 to V volt, let us consider it that way ok. And this is going in parallel to 3 comparator inputs. There are 3 comparator in inputs 3 comparators C 1 C 2 and C 3 right. And each of this comparator has got 3 different kind of reference voltages ok. So, for first it is V by 4 plus V by 4 second plus V by 2 and third plus 3 V by 4 is it fine right.

So, what will be the output C 3 C 2 C 1 for different voltage ranges of the analog input voltage ok. So, that is seen in this part of the truth table, that you can see where this yellow box is the one, yellow box 1 is the one, where you can see how the input and output of this particular block is related ok. So, in the input is 0 to plus V by 4 in this range.

So, what is happening, for each of these cases this input is less than the threshold voltage or the reference voltage that is set for each of the comparator, is not it. So, for each of the comparator then the output will be 0. So, this is the case, is it clear. Now, when the input is from plus V by 4 to plus V by 2 ok? So, then what happens. So, it is for this particular comparator it is about the threshold, is it clear? So, these comparator we give you a output 1 C 1 will be 1 for rest of the cases it is below threshold this is V by this will this

threshold is V by 2, it is less than V by 2 and it is V by 4 that is also this is also less than V by 4 ok.

So, this is the case that you can see, when it is in this range plus V b y V by 2 to 3 V by 4 then what happens. Of course, it is more than this threshold voltage and also more than this threshold or difference voltage right. So, C 1 and C 2 will be high at that time ok and C 3 is 0 is it fine. And what happens when it goes to 3 V b by 4 2 plus V b V this in this range right. So, the analog input voltage is more than the difference voltage for each of the comparator right.

So, all of them will be giving a output 1 as you can see in this particular case is it clear right. So, with 3 comparators, we can see 4 dangers are mapped in this manner for the analog input voltage at the output of the comparator right. Now, with this kind of thing C 3 C 2 C 1 that is there at 4 such ranges, if you want to encode it into digital ok, this analog voltage into digital. So, these 4 ranges we know from what we have discussed before. So, 2 binary code is sufficient right, because it is 4 dangers are there. So, 1 could be 0 0 0 another 0 1 another 1 0 another 1 1 right.

So, instead of 3 outputs the way we have seen C 3 C 2 C 1, we can have a scheme and encoding scheme, where C 3 C 2 C 1 are the input ok. And we get binary output where the scheme that we follow, that when all of them at 0 that is 0 to plus V by 4 right, the output will be 0 0 plus V by 4 to plus V by 2 C 3 C 2 C 1 is 0 0 1 it will be 0 1, next 1 is 1 0 and next 1 is 1 1 this is one kind of mapping we can think of is it ok.

So, how we can get this encoding done? So get this encoding done we look at this particular relationship which is there within this bracket a bit closer ok. So, we can see that these output which is 2 to the power 1 output we are mentioning is just to give associate with the binary weight of that particular output ok. In a binary number representation the way we have done for DAC. So, similar thing we have thinking about ADC right. So, this one is 1 whenever C 2 is 1 you see C 2 is 1 over here and 2 to the power 1 is 1 over here C 2 is 0 and this is 0. So, this is what we can identify, is not it?

So, from that we can write 2 to the power 1 is output is equal to C 2 just like that ok. So, in the encoder within it the logic circuit that we can have is just C 2 is connected directly 2 to the power 1. So, no other gates and nothing else is required is it fine ok. Now, for 2 to the power 0 this output what we can see, this is if C 3 is 1; if C 3 is 1, C 3 is 1. So, this

is 1 when C 3 is 0 ok, it does not you know I mean it is not something I mean whenever it is becoming 1 it is becoming 1 C 3 is 0, in this cases we have to see some other relationship by which we have to figure out this particular 1 which is existing is it in a some of product method.

So, this is the first thing that we can identify and for this particular 1, we can see an unique combination when C 2 is 0 and C 1 is 1, which is occurring only on the ones in this particular you know C 3 C 2 C 1 combinations that is possible ok. When you are doing a competition like this of the analog input voltage and generating comparator outputs ok. So, at that time we can see that C 2 is 0 and C 1 is 1 and output is 1.

So, we can write it this particular in this statement in the form of a logic statement logic C 3 plus this is C 2 prime C 1 is it fine ok. So, within this encoder what we have got we understand. So, this is a analog input voltage these are the comparator outputs. So, this will go to a logic block right and that is the encoder and at the output there will be 2 outputs to digital outputs.

So, 1 analog input, 2 digital output and we are getting this 4 particular you know the conversion analog to digital conversion with 2 bits 2 bit conversion, is it fine by simultaneous conversion method right. Now, if we want to you know better resolutions 3 bit conversion ok. So, they will be 8 levels. So, let us see that kind of proposition right.

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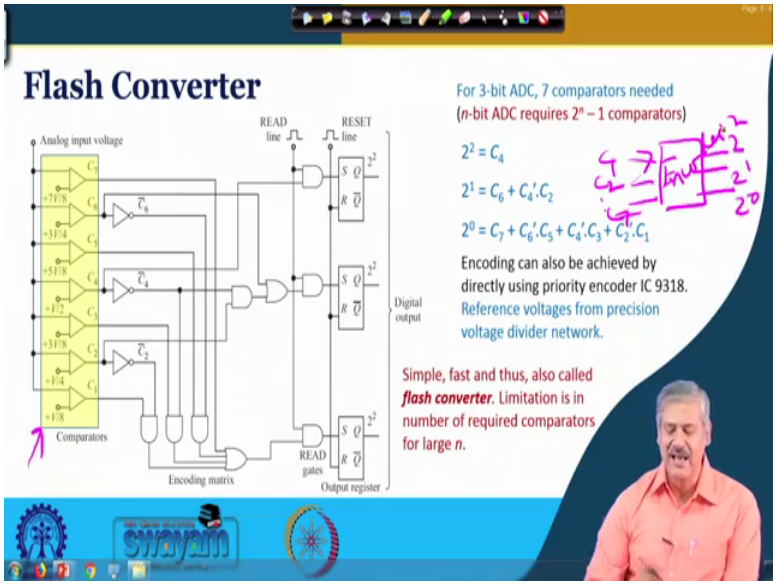

So, we are looking for 3 bit you know conversion. So, 8 levels so, 8 levels how many comparator will be required, as we have seen for 4 levels 3 comparators are required, because the first one was coming that all of them are below the threshold for each of the comparator right. So, for 8 levels right 3 bit you know conversion ok. So, we shall required 7 comparators is fine right.

So, 7 comparators will be generating output the way we have you know that particular table can prepare right. And from that this C 1 to C 7 output we can pass it through an encoder ok. So, this is C 1 this is C 2 up to say C 7 this we can pass through an encoder.

So, 2 to the power 2 2 to the power 1 and 2 to the power 0, so, this is your encoder right. So, we can develop the logic for that the way we have seen the relationship in the previous case. So, similar thing we can find out ok. And if we do then what we shall see we shall see that 2 to the power 2 that output can be directly taken as C 4. The way you had seen earlier 2 to the power 1 was directly taken for it you know 2 bit conversion case was taken from C 2. So, similarly it is second from C 4 ok. 2 to the power 1 in this case C 6 plus that is or C 4 prime C 2 and 2 to the power 0 will follow these relationship.

So, this we can do, but just by drawing the table and then mapping it to the 3 bit you know relationship the way we had done for 2 bit representation for 4 level. So, 8 level, 7 comparator output and 3 bit mapping and this way we can get the encoding done is it fine you understand this part. So, this can be extended to n bit ADC and we know the number of comparators required will be 2 to the power n minus 1. So, number of comparator increases you know with the number of bits that you are using ok, but this method is very fast because parallel you know comparison is being done ok. And that is why when you make a ADC out of this is called flash converter right, but the limitation of course, is the number of comparators required.

So, for which power requirement is more it becomes more expensive also and regarding how fast it is some numbers we shall see later when we discuss some other types of ADC and then we can have a comparison right. And this reference voltages this V by 8 V by 4 this reference voltages are required earlier also you have seen V by 4 V by 2 3 V by 4. So, this is obtained can be obtained from precision voltage divider network ok. So, that is how we can get it right.

And also we take note of that this encoding can be achieved by using priority encoder which is available of the shell as IC 9 3 1 8 ok. And here whatever logic you see over here so, see this is the logic this logic block that you can see right. And finally, the output is are stored in a output resistor so, that you can use it you know subsequently is it fine. So, this is how flash converter this ADC can be achieved.

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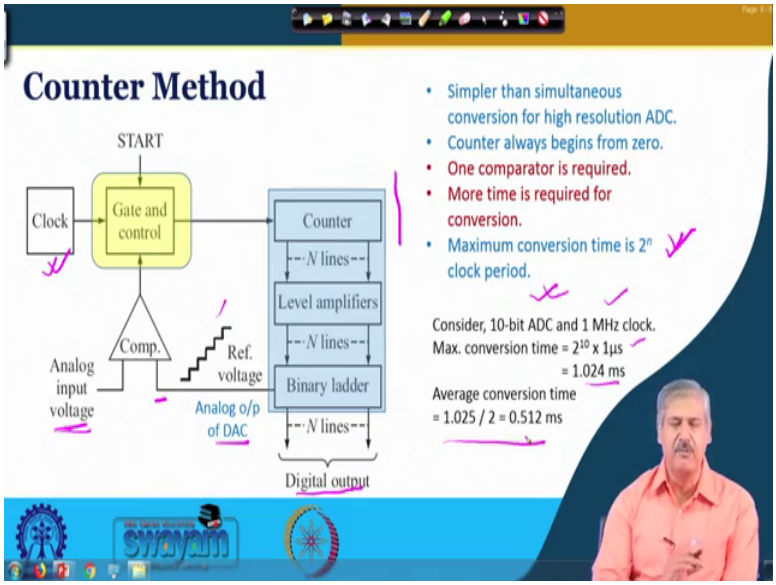

Now, this number of comparators getting increased and also you are not very comfortable with that cost is increasing power budget is increasing right. So, can we think of something by which number of comparators requirement you know comes down ok. So, one such scheme is counter based method where the number of comparator required is only one ok.

So, what was parallel before now we have made sequential. So, of course, you can see you can understand the tradeoff is with the time ok. So, more time is required right. So, let us see how it works?. So, what you see over here is a block ok. So, there is a counter right. So, this counter is initially reset that is it is initially at 0 ok.

And then it increments right and when it increments you have seen this kind of arrangement for a DAC. So, there is a level MP fan there is a binary ladder. So, this ladder output this analog output that DAC that you get which will be a step like this thing output. So, this output comes over here and that is a comparator that I was talking about right and this is the analog input voltage right. As counter value increases this voltage

will keep increasing and whenever it exceeds; whenever it exceeds the analog input voltage, the comparator output changes right.

And this comparator output goes to a gate and control circuit, which we shall see little later right and that now inhibits the clocking to the counter ok. So, whatever is the counter value is something which is related to the analog input voltage. And this counter value can be taken as the digital output a converted inner value is it clear ok. So, one comparator which is comparing the value, in each clock cycle till the DC output of it the counter output converted through a DAC. That is why we actually started discussion of this ADC DAC with DAC because DAC is that concept this ladder network is you know inherent in this type of ADC construction right.

So, this is in this case if the number is more the analogue voltage is more and if you have got n bit. So, you have to you know use all the bit. So, it will go up to the you know 2 to the power n count. So, the maximum conversion term time ok, e can be up to 2 to the power n right. So, if it is a 10 bit ADC we are talking about n bit 10 bit ADC and 1 megahertz clock is used here right, then maximum conversion time is 2 to the power 10 into or 1 micro second, so, it is 1.024 millisecond.

And if you take on average because some numbers some input will be high some input will be low. So, it will be just average of 27.512 millisecond. So, it is much slower, but number of comparator requirement is less and this circuit is simpler ok.

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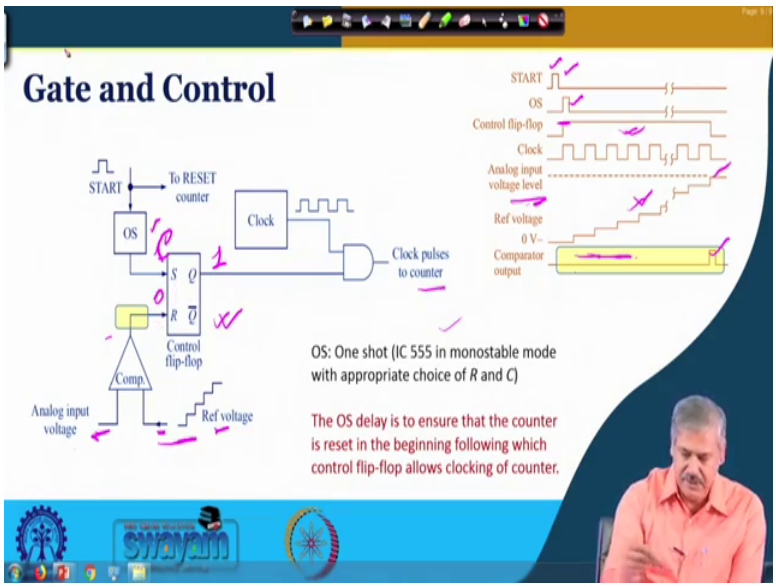

Now, let us see how the get and control works for this particular circuit. So, this is the comparator this is the analogue voltage, this is the output of the ladder, which is effectively working like ADC within a ADC right. And this is the comparator output which is remaining low right, when this reference voltage coming from DAC the counter converted counter output converted to analogue output right through a DAC ok.

So, this output is lower than the analogue input voltage. So, at that time the computer output is low ok. So, this comparator output is low right and then what you see OS is a one shot. So, that is a 555 working in a mono stable mode right. So, when you start the conversation. So, this is your start right.

So, immediately the counter is reset immediately, the counter is reset and this particular control flip flop that you see is reset ok, after sorry it is set it is after sometime ok. So, that the clocking of the counter is staggered is delayed by some amount. So, first it is ensured that the counter is reset, by this and then this one shot output is coming here. So, one shot output it is becoming high 1 ok. So, this is 0. So, this output will become 1 right, after that it remain becomes 0.

So, 0 0 means previous value will be written is it fine so, that when this is 0 this is remaining at 1 and this clock is coming. So, these clock will go to the a countered and counter will start you know increasing, it is value with every clocking ok. So, that is the clocking that is happening right. And counter is increasing it is value and corresponding ladder output the reference voltage that is also getting increased ok. And this is the analogue input voltage level. So, that is the dotted line you see and whenever it exceed it what happens these value becomes 1 right, this comparator output becomes one. So, this is already 0 right.

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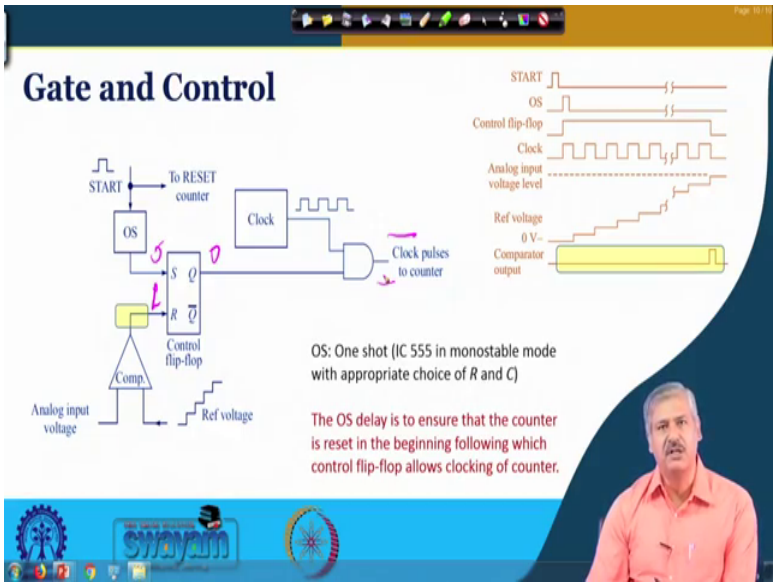

So, 1 and 0 now it becomes this becomes 1 and this is 0 it becomes reset right. So, this is reset means clocking is now stopped. So, at the output of the AND gate the clocking is stopped is it ok. And now whatever is the value that is the value related to the digitally coded value of the analogue input is it fine.

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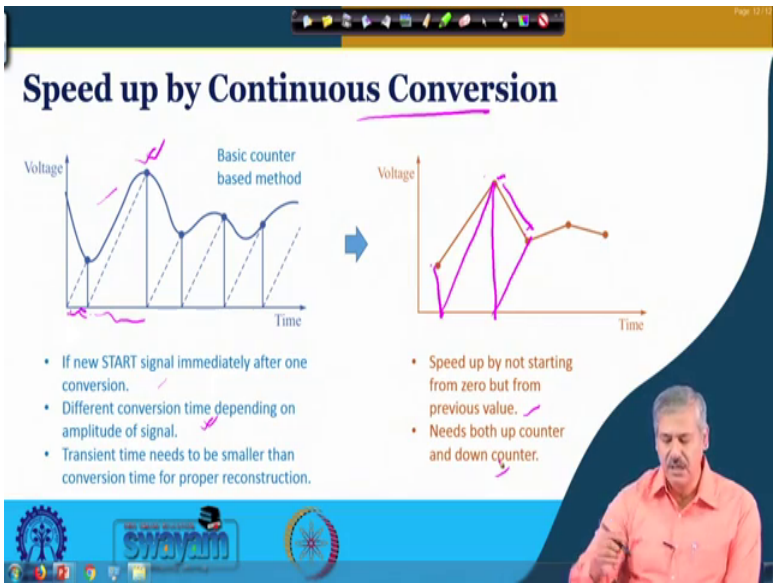

Now, in this counter based method, what we can see, that it is starting from here, if the new start signal comes immediately after one conversion of the analogue input voltage

and the analogue input voltage is something like this. The one you that you see over here right.

Now, it is starting it is converting then it is getting reset right immediately we are considering, that it is again next conversion starts immediately after it. So, next reset up you know next count begins and it will go up to this level. So, for each of this cases you can see the this axis is tie. So, conversion time is different ok. So, this is what we can see from here, depending on the amplitude of the voltage right, it takes more or less time ok, with respect to one another right.

Now, when this particular digital codes are sent for reconstruction from say another digital to analogue. So, reconstruction time a has a certain value right. Now, if it comes very close to one another like this particular case right. So, there could be any issues with the reconstruction right. And also the other thing that we see that every time it starts from 0 counter start from 0 ok. The requirement of the time getting increased I mean a maximum could be as I said 2 to the power n depending on the magnitude of amplitude of this value right.

So, to overcome is this you know so, sort of limitations encounter this method what people have thought about a method of continuous conversion ok. So, in this say it has reached this value. So, then it is not coming to 0 and again beginning from the 0, it is going from here to hear ok. So, it is not coming from coming to 0 and then again it is trying to reach this value, it is coming directly from here to here ok. So, this is the modification that is done ok. So, by which a speed up is achieved right. And for this you can see here the counter is going up from the previous value and here the counter has to come down right. So, we need both up count and down count you know options with in the circuit ok.

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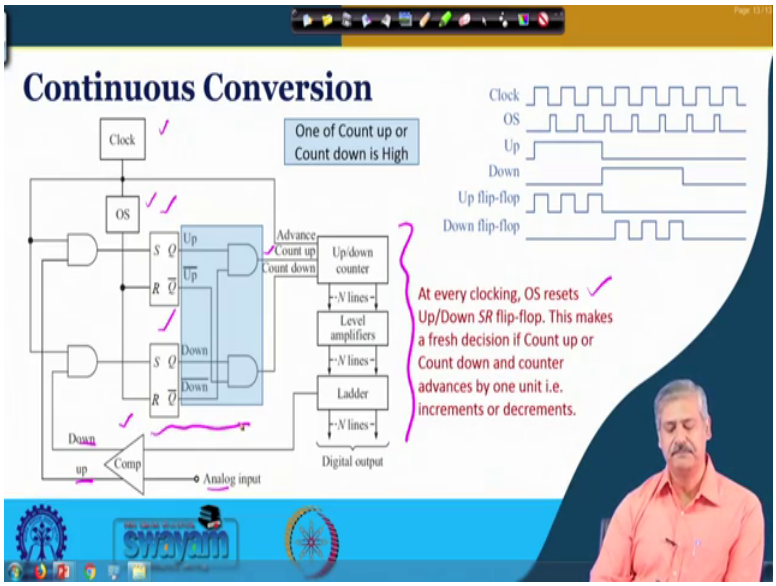

Now, for this we employ a circuit which is of this nature, which is a you know upgrade of the counter based circuit that we had seen before. So, we are already seen this block before ok, this block before right. Now, this is the comparator. So, depending on the value without this analogue input value is more or less right we are getting 0 or 1. So, we can convert it to up or down ok.

So, up means it need to be increased counter need to be increased and down means counter need to be decreased right. And this is now going to this control flip flops ok, these control flip flops this is it works in this manner. So, every time you know the clock comes this one shot this mono shot the mono shot that you had seen before ok, it actually is you know resetting this particular flip flop.

So, at every clock this one shot resets the up down this S R flip flop ok. And after that depending on this output so, it decides whether it will go for a up count or it will go for a down count, please understand the difference right. Earlier, if it was up count then it is going on up count and then coming back to 0 again, it is continues to up count right.

Here every time in every clock it looks at this comparator output and based on that ok, it decides whether this count up will be high and countdown will be low or the other way ok. So, that is the logic that you can find out here is it clear ok. So, one sort output this one it is going to reset. So, it will get reset after that is becomes 0 and after that

depending on whether this one is I 1 0 or this one is 1 0 depending on that this up or down 1 of them will be high and this will be count up or count down 1 of these 2 ok.

So, next clock again if it is decision is made right. So, that is what you can see. So, this is up count is happening and then again it is down count is happening based on this flip flop and every time the clock is coming over here and it is continuously happening. So, this counter is not getting reset, is it clear. And this is the DAC output and this is final digital output.

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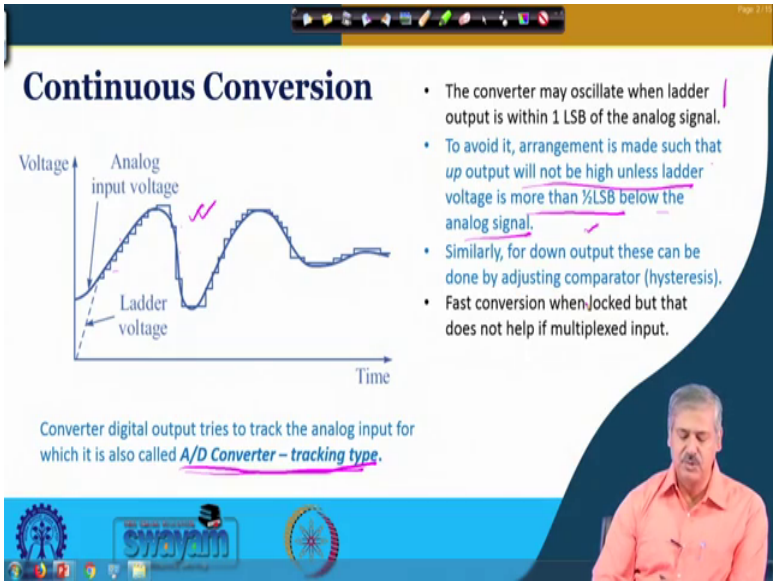

So, for continuous conversion so, this is what you would see happening for the input voltage and the analogue input voltage (Refer Time: 23:54) the ladder voltage, that is the digital to analogue conversion of the counter value, that is there. So, how they you know map each other. So, this is what you would see for a continuous type conversion ok.

So, this is the change and this is the corresponding change is over here. So, it is higher value. So, it is going up here it is coming down because it is lower value ok. So, this is the way things will move right. And this converter of this in this particular converter, the digital output, tries to track the analogue input and for which it is also called analogue to digital converter tracking type ok.

So, once it is locked it is very fast right, you compared to the basic counter based method we discuss before ok. So, once it you know gets locked to the analogue input voltage. So,

either it is going up or going coming down. So, smaller number of clock cycles are required, it does not need to begin from 0 for the basic method.

Now, there are certain additional things that goes into this kind of you know analogue to digital converter where continues conversion is employed. So, it make oscillate when the ladder output is with in 1 L S B of the analogue signal. So, a you know either it is going up or it is coming down the comparator output. So, it will always you know oscillate ok.

So, to avoid that it arrangement is special arrangement is made ok, that when the up output we the such that the up output will not be high unless ladder voltage is more than half LSB below the analogue signal always ok. So, this is something that is included in the circuit in addition right. So, this avoids oscillation. And similarly for the down out put generation ok. So, the same thing is done right.

And another issue we one of an things of an one particular ADC use used for multiple inputs is there a are multiple input is there and we are trying to convert them ok, sequentially right in a multiplex manner. So, in such a case, in such situation, this kind of conversion is not suitable, because it comes out of the locking right, once it is locked it is very fast. So, every time it has to go through these transients this you know the fresh conversion is starts. So, that is where it is not suggested.

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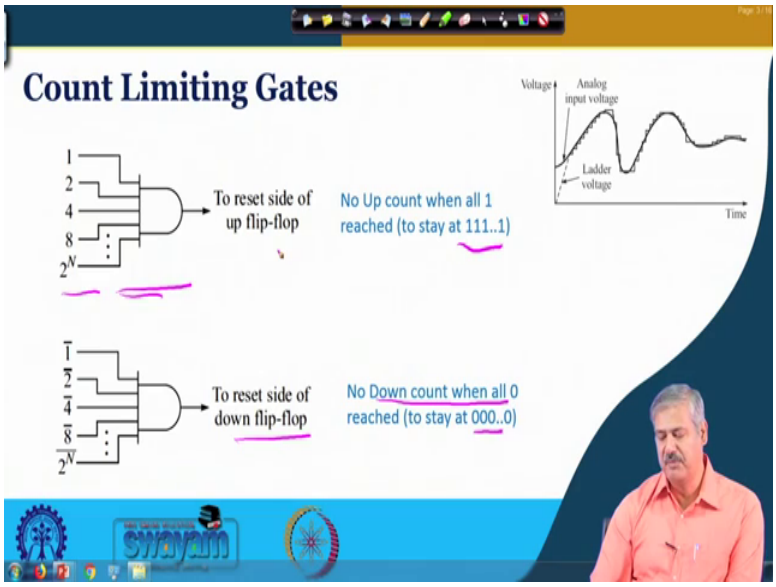

Finally, another important thing that comes with this kind of you know a Ato D conversion as additional circuitry, that when the up count has reached the highest value, that all 1s are there right all 1s are there ok, like this right. And still the analogue voltage is more ok, then it will try to go again further, but if you the counter goes further, then it will go to all 0 is not it.

So, at that time it should not you know, it should remain at that value only ok. So, that is what is ensured by putting this additional circuit no up count when all one are reached right, no further up count. And similarly no further down count when all 0 are reached ok, where you are putting in this case all inverted outputs, complimentary outputs ok of this thing. And to reset side of the down flip flop and here, it is all un complimented to the reset side of the output flip flop is it clear.

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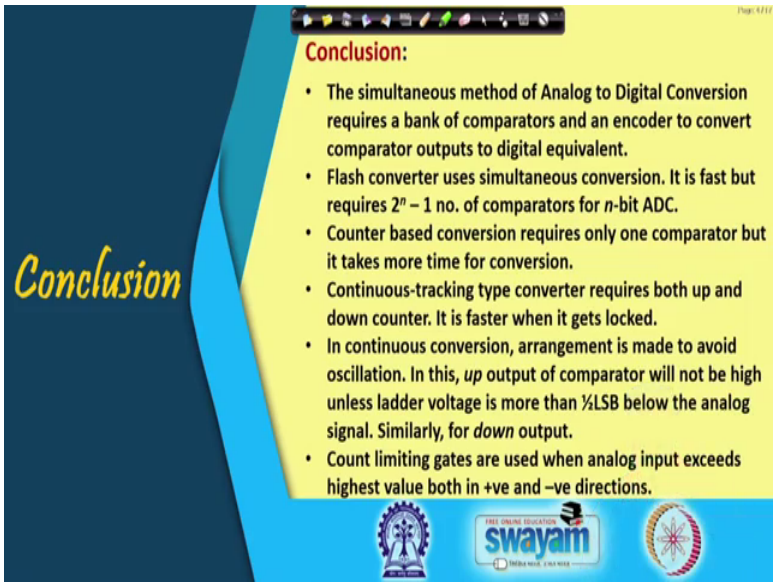

So, with this we conclude what we have seen very briefly that simultaneous method of Ato D conversion requires a bank of comparators and an encoder to convert the comparator outputs to it is digital equivalent ok. Flash converters are useful for a flash convertors use a simultaneous conversion it is first, but it requires large number of comparators. So, for n bit it requires 2 to the power n minus 1 ok. Counter based conversion is simple the basic one that we have seen, that only one comparator is required, but it requires more time.

So, we move to continuous tracking type converter using counters, which requires both up and down counter and little bit of additional circuitry and when it is locked to the input voltage it is very fast ok. And for, but multiplexed input it is not advisable and in the additional circuitry we also include count limiting gates when the analogue input exceed the highest value both in positive and negative directions ok.

Thank you.