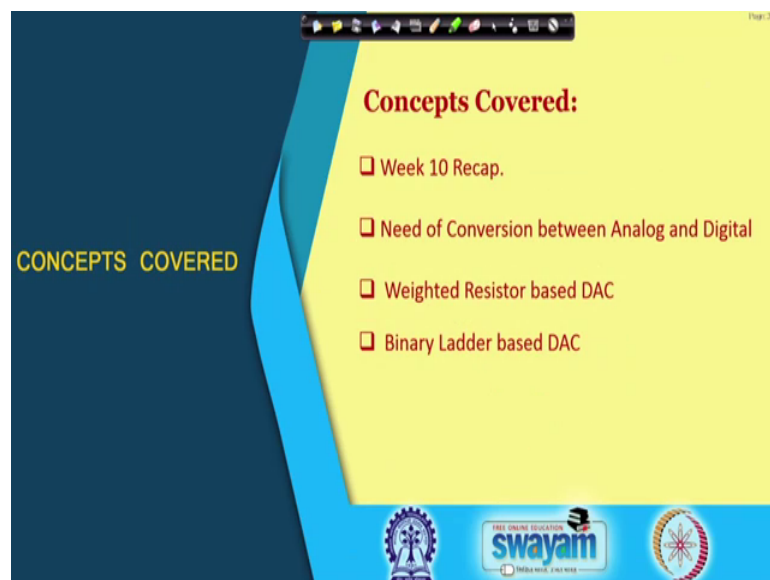


Digital Electronic Circuits
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Lecture – 51
Digital to Analog Conversion - I

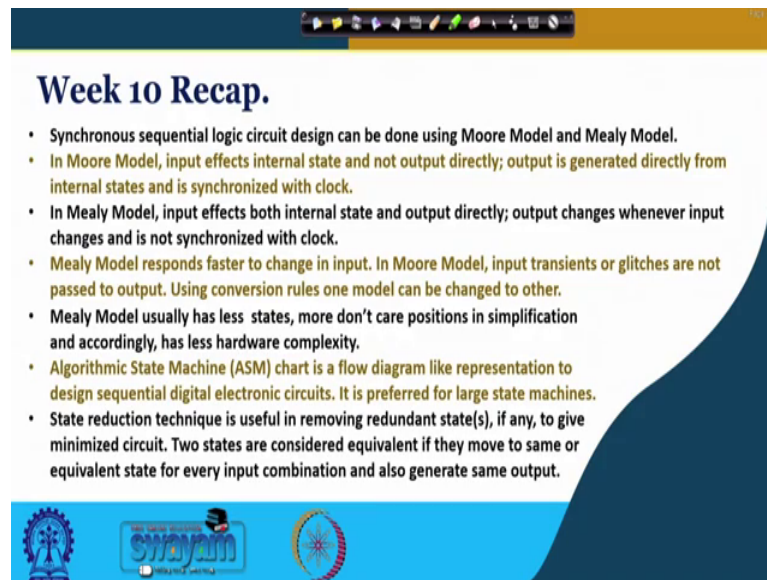
Hello everybody, we are in week 11 of this particular course. In this we will look at Digital to Analog Conversion and Analog to Digital Conversion. So, in today's class we shall take up digital analog digital to analog conversion.

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And before that we shall have a quick recap of what we discussed in the previous week, then need of conversion between analog and digital and 2 techniques for digital to analog conversion; so, that we shall see.

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Week 10 Recap.

- Synchronous sequential logic circuit design can be done using Moore Model and Mealy Model.
- In Moore Model, input effects internal state and not output directly; output is generated directly from internal states and is synchronized with clock.
- In Mealy Model, input effects both internal state and output directly; output changes whenever input changes and is not synchronized with clock.
- Mealy Model responds faster to change in input. In Moore Model, input transients or glitches are not passed to output. Using conversion rules one model can be changed to other.
- Mealy Model usually has less states, more don't care positions in simplification and accordingly, has less hardware complexity.
- Algorithmic State Machine (ASM) chart is a flow diagram like representation to design sequential digital electronic circuits. It is preferred for large state machines.
- State reduction technique is useful in removing redundant state(s), if any, to give minimized circuit. Two states are considered equivalent if they move to same or equivalent state for every input combination and also generate same output.

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Very quickly what we saw in week 10 is how we use Mealy model and Moore model to design synchronous sequential logic circuit. And we had a comparison of these two different modeling techniques. So, in Moore model we had seen that input effects the internal state and output is generated from those states only. So, input does not directly go to the output logic generation.

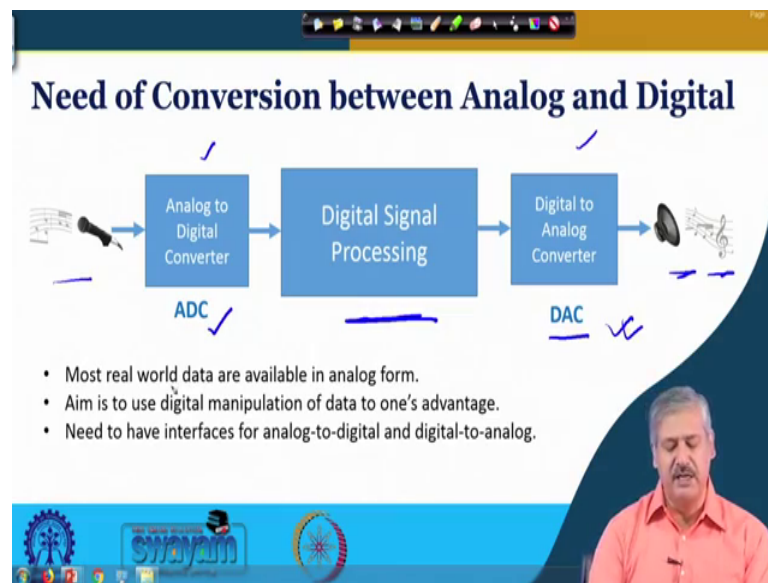
So, in Mealy model the internal states as well as input together act and to generate the output of the particular circuit. So, for which we have got certain advantages and disadvantages of both. So, in Mealy model, we can get the output a bit quicker, more number of do not care states, do not care states in the corner map based minimization. And it will be less hardware and in Moore model any tangents in the input circuit is not input signal, is not passed to the output directly.

So, once the tangent stabilized then the clocking happens and then the output is generated from the internal states. So, these are certain things that we had seen and we knew how to convert one model to another. So, we saw the techniques. So, accordingly we can employ them and depending on our requirement, we can use one or the other ok.

So, you also saw algorithmic state machine chart based design techniques, which is a flow diagram based method, it is preferred for larger state machines, because state transition diagram is found in adequate or very complex to read when the number of

these variable number of states number of inputs increase ok. And also we saw that state reduction techniques, the usefulness of it and how it can be used to minimize a given synchronous logic circuit and by which we can get a mode you know a simpler circuit ok. So, this is in brief what we discussed in the last week.

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Now, we go to a very important thing about this digital manipulation of signal. So, the most of the real life signal, that we encounter are in are analog in nature. Analog means continuously varying with time and we had already seen that these digital manipulation is of advantages and more about it you will study in some future courses or parallel you are studying in signals and systems or digital signal processing right.

So, what is important is that, we should be in a position to convert analog data to digital ok, analog signal to digital signal. So, for which we need to have a something called Analog to Digital Converter. In brief it is called the abbreviation it is called ADC right. So, consider a sound signal audio signal right.

So, you have captured it through microphone and then analog to digital converter is converting it to a digital stream right. And then you are doing some manipulation over here. So, some frequencies are boosted, some frequencies are you know at innovated and all you are, it is good that you know to have a digital processing technique because of its advantages right. And after that you want to play it in a speaker right, where this speaker will continuously you know change its position and generate the sound wave right.

So, for that we need to generate a continuous signal continuous time signal right. So, you need a digital to analog converter over there right. So, this is the kind of thing that we expect when we are trying to manipulate an analog signal in a digital platform right. So, at two ends we will be having analog to digital I mean in one end analog to digital converter and another end digital to analog converter ok. So, this is the interface circuit right. So, in this week we shall look into them right.

So, we begin with digital to analog conversion this part later we shall take up ADC, because in ADC within ADC somewhere a concept of DAC is already there right. So, it is better that we start from DAC right.

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Weighted Resistor

From KCL, ✓

$$\frac{V_0 - V_A}{R_0} + \frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} = 0$$

$$V_A = \frac{V_0/R_0 + V_1/R_1 + V_2/R_2}{1/R_0 + 1/R_1 + 1/R_2}$$

$$V_A = \frac{V_0/R_0 + V_1/(R_0/2) + V_2/(R_0/4)}{1/R_0 + 1/(R_0/2) + 1/(R_0/4)}$$

$$V_A = \frac{1}{7}(V_0 + 2V_1 + 4V_2)$$

Neglecting current through very high resistance R_f ✓

Bit	Weight
2^0	1/7
2^1	2/7
2^2	4/7
Sum	7/7

$R_2 = \frac{R_0}{4}$ ✓ $R_1 = \frac{R_0}{2}$ ✓

$R_f \gg R_0$ ✓

Analog output

Now, let us see how we can get a digital to analog conversion done. So, remember for a digital to analog conversion the input is digital right and corresponding analog signal is to be generated. So, input is digital means what? Input will be in the form of a you know binary digit say if it is a 4 bit then 1 0 1 0 or 0 0 1 1 or so, if it is a 3 digit 0 1 1 1 0 0 some such thing and output should be a voltage which corresponds to that particular this input digital input combination digital signal ok. So, if it is a voltage otherwise it could be a cadent depending on some continuous time manifestation of the input signal any equivalent manifestation ok.

So, let us look into one circuit which is based on weighted resistor right. So, what you see here; what you see here is a circuit where, this is the circuit under consideration. So,

this is your R_{naught} , R_1 , R_2 right. And this is your the voltage at this node right and this R_L load resistance is very very large, in comparison to the resistances that you have there in this different branches ok.

And to begin with let us not bother about this part ok, 2 to the power 0 etcetera let us just consider these are 3 voltages V_{naught} V_1 V_2 ok. So, this particular circuit just like this how will it operate? So, if we apply KCL at this particular node right since current is very large over here I mean resistance is very large over here. So, the current is very small, so, you can neglect that part right. So, that is what we have mentioned here. So, $V_{naught} - V_A$ by R_{naught} is the current through this $V_1 - V_A$ by R_1 is the current through this and $V_2 - V_A$ by R_2 is the current through this right. So, from KCL it should be equal to 0, is it fine?

Now, if you take all this V_A by R_{naught} V_A by R_1 V_A by R_2 to 1 side and define, then this is the question that you get right. And in this particular equation, if you consider that your R_1 is R_{naught} by 2 ok, R_2 is R_{naught} by 4. So, it is say it is called R weighted resistor ok. So, resistor values are like this right. So, it is R_{naught} divided by some integer power of 2.

So, this is what you get R_{naught} by 2 R_{naught} by 4 and then when you cancel out R_{naught} ok, then what you get here is 1 upon 7 V_{naught} plus 2 V_n plus 4 V_2 is it fine. So, this V_{naught} and this is 2 times V_1 , this is the 4 times V_2 . So, to indicate that we have mentioned this is 2 to the power 0 2 to the power 1 is 2 2 to the power 2 is 4 and you can think of you know extending it beyond that right.

So, the weight final the V_A value you get the weight of V_{naught} , in that is what 1 upon 7 whatever the voltage is there it is 1 upon 7 weight of V_1 is 2 upon 7 , 2 divided by 7 weight of V_2 is 2 to the power 2 that is 4 by 7 ok. And if you sum it up it will you will get 7 . So, this the individual weights, is it clear the basic circuit right.

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Output Combinations

$V_A = \frac{1}{7}(V_0 + 2V_1 + 4V_2)$
 $V_A = \frac{1}{7}(7 + 0 + 0) = 1\text{ V}$
 LSB weight = $1/7$
 $V_A = \frac{1}{7}(7 + 0 + 4 \times 7) = 5\text{ V}$

Digital input			Analog output
0	0	0	+0 V
0	0	1	+1 V
0	1	0	+2 V
0	1	1	+3 V
1	0	0	+4 V
1	0	1	+5 V
1	1	0	+6 V
1	1	1	+7 V

0: 0 V
1: +7 V

Now, if you look at these voltages V_0 , V_1 , V_2 , either we put plus 7 volt or 0 volt because these are digital input right either it is high or low. So, you consider high for 7 volt and low for 0 volt right. So, this is one such case 0 0 1 right, then what will happen V_0 is 7 volt right, this is your V_0 , V_1 and V_2 right. And this is 0 0 0 the output will be 1 volt right and if it is 1 0 1 1 0 1. So, this was 0 0 1 this is 1 0 1 right.

So, this is 7 volt, this is 0 volt, this is $V_2 = 0$ and this is $V_2 = V_1 = 0$, V_2 is 7 so, 4 into 7. So, what you get here it is 5 volt right. So, this is the way the output voltage depending on the input combination will be calculated. And if you have all the input combinations digital input combination from 0 0 0 to 1 1 1 ok, you had at the input side, then the corresponding analog output will be 0 volt 1 volt to 7 volt is not it.

And the list these LSB weights the voltage that you can calculate I mean which is also the resolution of it. So, this is 0 volt and this is 1 volt. So, this is 1 volt is what you see as the voltage that it can you know move from one value to another is it clear right.

(Refer Slide Time: 11:55)

Weighted Resistor and n -bit DAC

Extending for n -bit ($n = 0, 1, 2, \dots, n-1$)

$$V_A = \frac{1}{2^n - 1}(V_0 + 2V_1 + 4V_2 + 8V_3 + \dots + 2^{n-1}V_{n-1})$$

$$\text{LSB weight} = \frac{1}{2^n - 1}$$

Limitations:

- Precision resistor required
- MSB resistor is to handle much more current than LSB resistor (For 8-bit: 128 times more)

$V_A = \frac{1}{15}(V_0 + 2V_1 + 4V_2 + 8V_3)$

LSB weight = 1/15

Now, if we extend it to 4 bit, if you extend it to 4 bit what happens? So, this is R naught this is R naught by 2 this is R naught by 4 and you can imagine the next value will be in the weighted resistor based method, it is R naught by 8 right and again if you apply KCL just if you know go on doing that.

Now, it will be the value will be 1 upon 15 plus V naught plus 2 V 1 plus 4 V 2 plus 8 V 3 right. So, this position is to 2 to the power 0 2 to the power 1 2 to the power 2 and 2 to the power 3. These are the corresponding you know binary weights for the digital data that is coming right. And the LSB weight earlier it was 1 upon 7 for the 3 bit case, now 4 bit case it is 1 upon 15 that is whatever the V naught value it will be multiplied by 1 upon 15 right, this is fine.

So, we can extend it to a n bit case and in that case the output voltage over here analog output that you see, for a particular combination of the digital input will be given by this one right. So, this is V naught and this is you know the end part will be your this V n minus 1 for n bit because it starting from 0. So, 0 to n minus 1 right and LSB weight will be 2 to the power n minus 1 is it fine.

So, this is the way we can convert a digital input coming as a big stream to a corresponding analog voltage is it clear right, there will be more associated circuitry and all for practical use. So, that part we shall take up in next class. So, the first part is what we understand how we can convert through a weighted resistor based method.

Now, there are certain limitations that you can visualize for this particular method ok. For which we shall move to another method which is you know found more useful. So, first of all this depends on the weights of the resistors. So, this is we require precision resistor. So, this is one requirement and the second one is the MSB resistor, this one you can see it is value is R naught by 8 and this is R naught ok.

So, how much current is taken it is? So, this is 7 volt and this is 7 volt. So, this is 1 upon 8 right. So, the current is as much as many times lower I mean higher than this one right. So, for MSB, if it is a 4 bit case, it is 8 times more if it is 8 bit case right. So, it will be 2 to the power 7 because it is a n minus 1 2 to the power n minus 1. So, 128 times more current will be flowing through the MSB ok, MSB resistor right.

So, the loading of it the you know associated issues like heat generation and all is becoming more and more you know troublesome, when the number of bits increase in this particular method ok. This is a simple method, but this is one limitation that we find ok. And today we are talking about larger number of bits used in DAC. So, in that case we need to look at an alternative circuit. So, for smaller number of bits is fine ok.

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Binary Ladder

Consider, only V_0 is non-zero. Using Thevenin's Theorem for the cut shown,

$$V_{Th} = V_0 \frac{2R}{2R+2R} = \frac{V_0}{2}$$

$$R_{Th} = 2R || 2R = R$$

Extending to next cut,

Extending further,

LSB weight = $1/16$

$V_A = \frac{V_0}{16}$

So, for the alternate circuit what we have is called binary ladder ok. This is very very you know useful circuit. So, the binary ladder first we see this structure and then analyse the circuit and then we shall move ahead. So, what you see this also you can see this is a $2R$ then R $2R$ R $2R$ R this is though it has it has been arranged ok. So, there is no such

thing like R naught by $2R$ naught by $4R$ naught by 8 and so on and so forth I mean becomes some difficult. So, it is all of you know particular type either $2R$ or R and it is terminating here with $2R$ is it fine.

So, this side further one is V naught then this is $V_1 V_2 V_3$ earlier we started from this side was V naught you remember that ok. So, this is (Refer Time: 16:23) differences. Now, how we analyse this circuit for which we use what is called Thevenin's Theorem right. So, in Thevenin's theorem, we calculate Thevenin's voltage and Thevenin's resistance right.

So, here for this particular circuit we consider there is a cut over here. And then we see that the circuit is seen from this side to their right hand side from the left hand side to the right hand side. So, this particular block over here we are trying to find the Thevenin equivalent ok. So, for this V naught so, V_{Th} will be V naught into this is $2R$ by $2R$ plus $2R$ right, this is the resistance this is resistance this is open circuit this is cut here right, we know the how the Thevenin theorem work ok.

So, this is V naught by 2 fine and what is the Thevenin equivalent resistance so, $2R$ in $2R$ in parallel. So, this is R so, this particular block, this particular block can be you know written in this manner with a equivalent circuit obtained from Thevenin equivalent. So, V naught by 2 and this is R is it fine ok. So, this you need to understand from the basics of electrical circuit where Thevenin's Theorem was taught ok.

Now, you look at this larger block this particular block ok. So, you consider all other voltages are not present (Refer Time: 17:57) is there later on we shall include them. So, this V naught by 2 and this is R and R if we consider a cut over here right, then this R and R right $2R$ and this $2R$ in parallel. So, again in a parallel voltage is the Thevenin voltage Thevenin resistance is R .

And now, V naught by 2 and this is V naught by 2 into $2R$ by $2R$ plus $2R$. So, it will become V naught by 4 is it fine. So, this is this particular block now comes over here like this right. So, again you consider a cut over here and you will find that this is going over here like this in this particular block right.

And finally, if you further you know move forward. So, you will be having plus minus this is your down ok and this is your R this is your V naught by 16 and this is your is it

fine. So, this is what you are going to get. So, the V over here that is available to the outside world is V naught by 16 and the output resistance is R, is it ok? So, the V naught at the output over here is coming as V naught by 16, is it clear?

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Weighted Sum

Extending and from principle of superposition,

$$V_A = \frac{V_0}{16} + \frac{V_1}{8} + \frac{V_2}{4} + \frac{V_3}{2}$$

$$V_A = \frac{1}{16}(V_0 + 2V_1 + 4V_2 + 8V_3)$$

Now, let us look at what happens to the situation when V 1 is present and others are not present ok. So, this is this case ok. So, in this case this 2 R and 2 R are in parallel right and becomes R. So, this is R and R 2 R and this is 2 R and if you take a cut over here, it is similar to what we had seen before only the number of stages to the right hand side is now less one less ok.

So, here first it is becoming V n V 1 by 2 and R then V 1 by 4 R and finally, it will be V 1 by 8 and for this also the output resistance will be R is it ok. So, V 1 contributes as V 1 by 8 in the final thing and this is V naught by 16 and if you extend for all the other voltage input and use principle of superposition you have these output voltage as V naught by 16 V 1 by 8 V 2 by 4 V 3 by 2. And if you add them up then it is 1 upon 16 V naught plus 2 V 1 plus 4 V 2 plus 8 V 3 is not it.

So, will see the 2 to the power 0 comes over here 2 to the power 1 2 to the power 2 and 2 to the power 3 right. So, these are the corresponding binary weights and corresponding analog output will be here this way right, earlier it was 2 to the power n minus 1, now it is 2 to the power n. So, this is for n is equal to 4 that is what we see over here.

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Binary Ladder and DAC

Bit position	Binary weight	Output voltage
MSB	1/2	V/2
2d MSB	1/4	V/4
3d MSB	1/8	V/8
4th MSB	1/16	V/16
⋮	⋮	⋮
Nth MSB	1/2 ^N	V/2 ^N

Consider, 5-bit ladder
 0: 0 V
 1: 10 V
 LSB: $\frac{10}{2^5} = 0.3125 V$
 Full scale voltage:
 $\frac{10(1 + 2 + 4 + 8 + 16)}{2^5}$
 = 9.6875 V

With 2R termination, full scale o/p voltage = $9.6875 \frac{2R}{(R+2R)}$
 = 6.4583V
 Current drawn from each digital source for R = 1KΩ is 10V/3KΩ = 3.33 mA

• Output impedance always R, regardless of the number of bits.
 • Terminating ladder with 2R impedance, looking into any branch from any node, impedance is 2R.
 • Each digital source sees input impedance as 3R. (equal loading)

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \dots + V_{n-1} 2^{n-1}}{2^n}$$

Now, we can extend it for n bit right. So, if we extend it for n bit then, we have for these binary weights corresponding to MSB will be a 1 by 2, second MSB third MSB 1 by 8 and nth MSB or the LSB will be 1 upon 2 to the power n right. And corresponding output voltages are V by 2 V by 4 etcetera etcetera and if you have add them up you get the analog output, is it ok.

And if we consider a 5 bit ladder just for an example and you consider 0 as 0 volt the digital binary input that is there and 1 is 10 logic low is 0 volt logic high is 5 you know 10 volt corresponding the binary covalent 0 and 1 ok, then the LSB will be 10 by 2 to the power 5. So, 0.3125 volt right and the full scale voltage right, when all the bits are 1. So, this is 1 plus 2 plus 4 plus 8 plus 16 right your putting those values divided by 2 to the power 5.

So, it is 9.6875 volt it is not 10 volt it is 9.6875 volt ok. So, few interesting thing about this ladder based DAC right. So, in this case output impedance is always R regardless of the number of bits ok. And if you here we have seen that the termination was with that part we have not discussed.

So, if it is terminated with 2 R ok, then looking into any branch; looking into any branch means in the ladder from any node right, the impedance is seen has 2 R. So, that is what you can analyse and see and each digital source. So, this is R and the 2 R. So, it will see a impedance as 3 R so, for the digital source. So, R and 2 R together it is 3 R right.

So, each one of them will be having equal loading right. And if it is not want almost equal loading I mean not much of the difference not like what we had seen in the case of weighted based weighted resistor based method, where it is the MSB was for a 8 bit case 120 times 8 more current you know the resistance was carrying 128 times more current ok.

So, these are certain advantages and instead of 9.6875 ok, if you terminate with $2R$ instead of this very high resistance, if you terminate with $2R$ then the output voltage will be $9.6875 \frac{2R}{2R + R}$ ok. So, this is 6.4583 volt ok. So, this you will note for the sake off you know your understanding if instead of a very high resistance ok. A some other value is used for termination, then what how you what will be the corresponding voltage, is it fine.

And then the corresponding current will be in that case you know 3.3 3 milli ampere for each one of them for another value. So, it will be you know close to that value it is not varying too much from one digital input source to another this is a good point about this method ok.

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Conclusion:

- For digital manipulation of analog signal, analog to digital conversion (ADC) is needed.
- To get back the processed digital signal in analog form, digital to analog conversion (DAC) is needed.
- Weighted resistor based n -bit DAC has LSB weight $\frac{1}{2^{n-1}}$. KCL is useful to analyse such circuit.
- DAC requires precision resistors. In it, MSB resistor handles 2^{n-1} times more current than LSB resistor.
- Binary ladder based n -bit DAC has LSB weight $\frac{1}{2^n}$. Thevenin's Theorem is useful to analyse such circuit.
- Binary ladder based DAC has constant output impedance irrespective of number of bits. It can have equal loading for each input.

So, with this we come to the conclusion of the first part of the DAC discussion. So, what you have seen is that for digital manipulation of analog signal, analog to digital conversion is needed and to get back the processed digital signal digitally processed signal, which is after processing is in digital form and you have to get back it into analog from then digital to analog conversion is needed ok. And we had seen 2 methods in weighted resistor based method in with digital to analog converter DAC has LSB weight of 1 upon 2 to the power n minus 1 and for analyzing that such circuit Kirchhoff's current law KCL is useful ok.

And for DAC used DAC using precision registers ok, the you know for this weighted registered based DAC the precision registers are required and MSB register handles 2 to the power n minus 1 times more current than LSB register this we have already seen. And binary ladder based das DAC has got width for the LSB as 1 upon 2 to the power n and Thevenin Theorem is useful to analyse such circuit and it has a constant output impedance with respective of number of bits, then it can have equal loading for each input is digital input which is a useful feature. So, with this we conclude this particular lecture.

Thank you.