Digital Electronic Circuits
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Lecture - 05
CMOS Logic

Hello everybody, we discus today CMOS Logic. In the last class, we discussed TTL Transistor Logic based circuits, ok.

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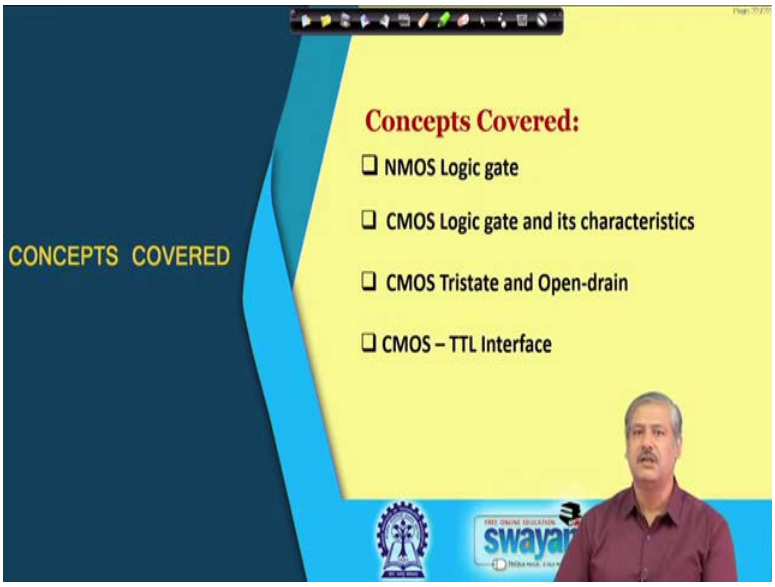

And we'll cover CMOS logic of course, and it is various configurations like tri-state and open drain and when it is used together with TTL in a circuit; how to interface, but we shall begin with a brief discussion on NMOS logic.

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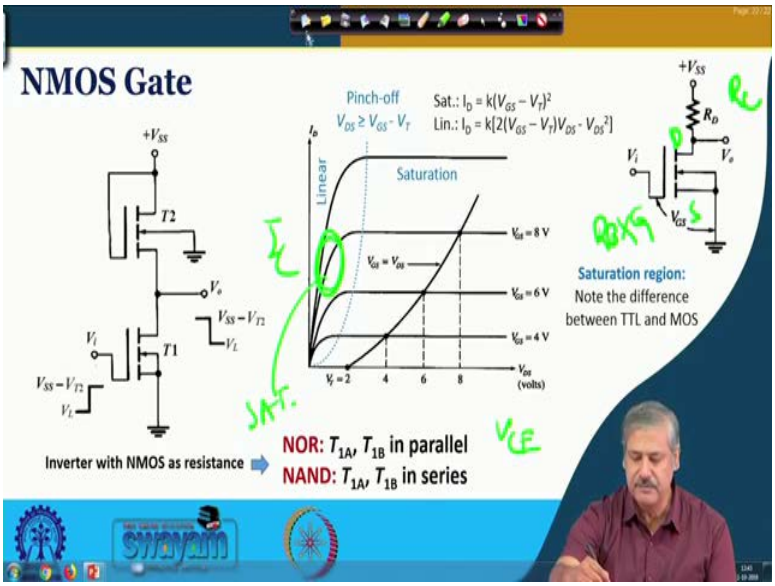

So, a MOS device you know is a field effect device which offers very high input impedance because its input is connected to an insulator - oxide layer, but it can be used as a inverter just like what the transistor based BJT based inverter that we had used before ok, without the - with the exception of that R_B is not required.

So, this is similar to what we had in earlier case R_C, but R_B is not required because it is - it is connected to an insulator - ok, its input impedance is very high- right. And, and this is an n-channel enhancement mode, the MOSFET that we are using here – alright, n-channel is used for the electron has got higher mobility; enhancement - that means, when a particular voltage is applied that is called threshold volt, a layer is, n-channel is formed and as long as the voltage remains more than that, the channel is there and the current flows and if it is less than the threshold voltage, the channel is not formed and the current will not flow ok.

So, V_i needs to be greater than threshold voltage or this V_{GS} needs to be greater than the threshold voltage and at that time, if we increase the – increase, this is your drain, this is your gate and, this is your source if we keep increasing the drain-to-source voltage right, the current will increase linearly in the beginning, but after that there is an effect called pinch-off effect when this V_{DS} is equal to V_{GS} minus V_T - ok. At that time, because of the pinch-off effect - beyond that, V_{DS} is going beyond V_{GS} minus V_T, the I_D, the current - the drain current will remain constant.\

Pinch-off: $V_{DS} \geq V_{GS} - V_T$

This drain current remaining constant here is termed as saturation which is different from the saturation region we had discussed in case of bipolar junction transistor where an equivalent I_C versus V_{CE} curve, we had seen. So, in the I_C versus V_{CE} curve that we had seen, in case of bipolar junction transistor, this region was the saturation region there if you remember - ok.

When the collector-emitter V_{CE} voltage was 0.2 volt or 0.1 volt of that sort, both B-C junction and B-E junction were in forward bias; however, in this particular case, in this particular case, this region is called saturation region.

So, this difference is to be noted not to get confused and this region when the V_{GS} is greater than V_T and the current increases with increased value of V_{DS} that is called linear region or called triode region and we have got two different equations; this is one equation which is there in the saturation region. So, the saturation region is similar to active region in our earlier discussion.

Saturation: $I_D = k(V_{GS} - V_T)^2$

Linear: $I_D = k[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$

And this equation we shall use later, keep note - take note of this in CMOS discussion and this is the equation when it occurs for linear region. And what people have done - they in the NMOS based logic development, this resistance manufacturing - because now the resistances are very high. So, this high resistance manufacturing - it takes lot of space. So, instead of that a NMOS driver based - NMOS transistor based load with gate-source, gate and drain connected in this manner which offers approximately linear - when this V_{GS} and VDS are, you know, constant.

So, you can see the - you know the current variation with the voltage is approximately linear. So, that is given, that is used as - instead of an actual resistor as a load which offers less amount of space, requires less amount of space. And for the NOR logic and NAND logic development using NMOS gate, you are having this particular inverter similar to what we had done in case of a RTL circuit or electrical switch based circuit a - for NOR

there will another transistor will come in parallel and for NAND, another transistor will come in series.

So, this is the standard thing that we had followed the similar thing is done for NMOS based logic gate development also. But, one issue that we here take note of here, is that when this transistor is on, T1 is on, the resistors must be sufficiently small compared to resistance 2, I mean which is resistance offered by the transistor 2; otherwise the output will not be considered sufficiently low, ok.

So, if it is you know, if both of them are same then what will happen, the output will be 0.5 of a 50 percent of V_{SS} which is not sufficiently low - we want to make it as low as possible, right. So, this T1 resistance will be sufficiently small compared to resistance offered by T2 that we take note of - ok.

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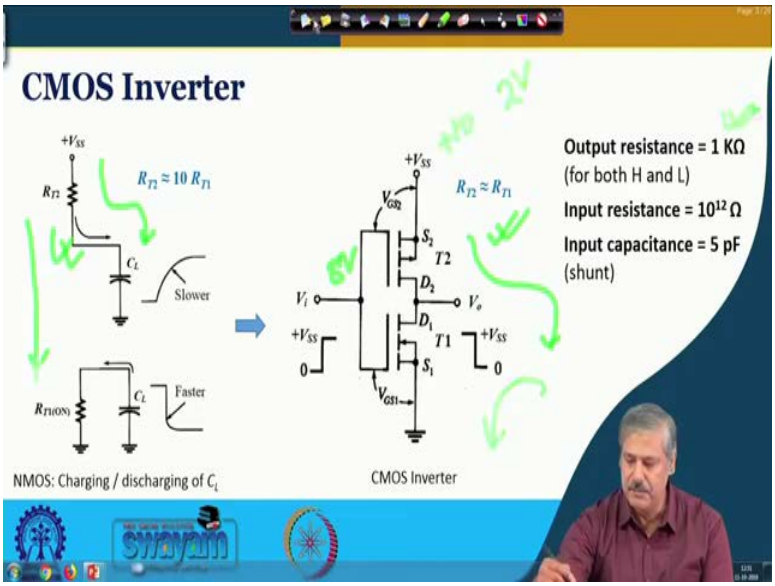

Because of which in the NMOS based circuit, we are having an issue that the output where the capacitor plays a very important role the at the output junction, charging and discharging of it because the current it the next stage will take is very low of the order of picoampere or so.

So, this charging of the capacitor by this particular resistance which is relatively high takes more time than the discharging of it. So, which limits the speed, which brings an element

of asymmetry. So, from a NMOS based logic inverter circuit, we have moved to CMOS base circuit where the particular part is replaced by a PMOS, ok.

So, how PMOS works? While in NMOS when we look at the working of the NMOS, so, basically you are forming a, placing a positive voltage above a threshold voltage which attracts electrons and the n-channel is formed and the current conducts. In case of PMOS what will happen, we want to form a channel made of holes, made up of holes.

So, a negative voltage, relatively negative voltage needs to be applied. So, if the source and substrate of it is connected to a positive supply say 10 volt over here- right; at the threshold voltage for this PMOS is 2 volt, then 8 volt or less would be required at this side at the input side, then only the PMOS channel will be formed and it will conduct - right.

So, when it is at low which is of course, much, much less than this 8 volt. So, channel is formed, so PMOS is on right and when it is at low then of course, it is less than 2 volts, so the NMOS will be off and the other case when it is 10 volt – right; so, when it is 10 volt, so, this is also, this is 10 volt this is 10 volt. So, it is not sufficiently negative, this particular junction - right. So, no p-channel is formed, but it is sufficiently - this particular is sufficiently positive above the threshold voltage, so n-channel will be formed.

So, at any given point of time we have got either a PMOS or NMOS on and only during - in a transition or the switching, both of them can become on, ok. So, because of which and this PMOS on - the PMOS is made in such a manner that the though the mobility of hole is less - that the output resistance is symmetrical for both, of both the cases about of the order of say 1 kilo ohm and the charging and discharging is faster compared to what we had seen before. The other important thing here - there is the, you know, when it is either 0 or 1, no power consumption is there along this path. Only during switching some power you know, consumption will be there and, also for during switching - when this output capacitor is getting charged or discharged - getting discharged. So, during that process some power consumption will be there, but during static condition - unlike in this particular case when it was on right, when it was on - ok. So, there was a current you know, flowing so that situation does not arise here and input resistance of such a CMOS is very high 1- 0 to the power, of the order, 12 ohm and capacitance is of the order of 5 picofarad, this capacitance which will come in a form of a shunt.

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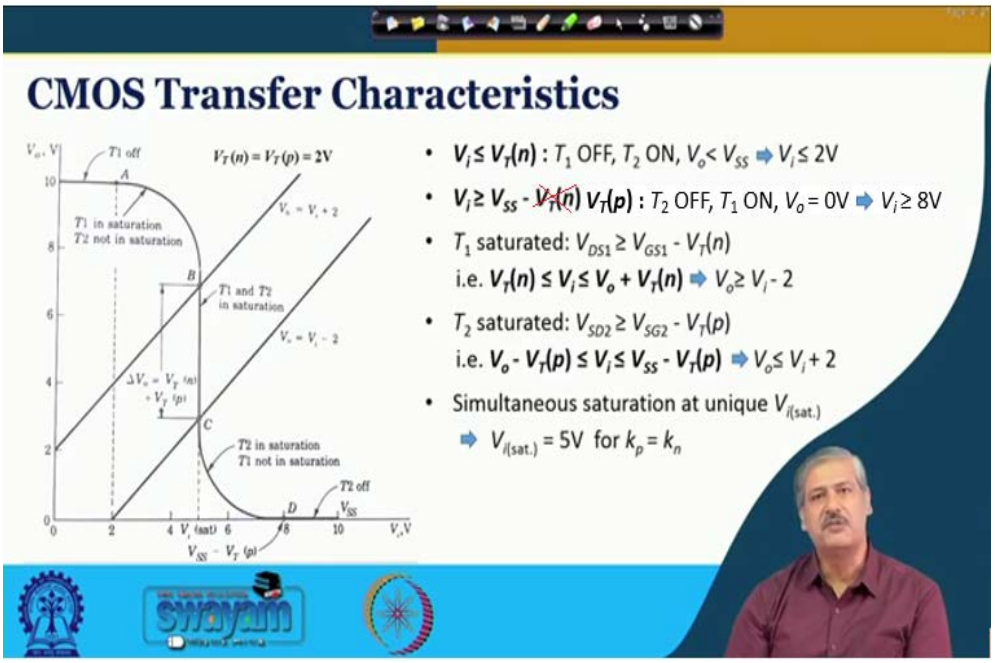

With this, we go to CMOS transfer characteristics and if we look at the CMOS transfer characteristics, this is the V_i versus V_o plot and it has got 5 distinct zones. So, the first zone that we look at is the case when the input voltage is less than the threshold voltage of the NMOS, ok. So, when the input voltage is less than the threshold voltage of the NMOS. So, what is happening at that time? The T1 the NMOS is off and at that time of course, this is sufficiently small right.

- $V_i \leq V_T(n)$: T_1 OFF, T_2 ON, $V_o < V_{SS}$ $V_i \leq 2V$
- $V_i \geq V_{SS} - V_T(p)$: T_2 OFF, T_1 ON, $V_o = 0V$ $V_i \geq 8V$
- T_1 saturated: $V_{DS1} \geq V_{GS1} - V_T(n)$ i.e. $V_T(n) \leq V_i \leq V_o + V_T(n)$ $V_o \geq V_i - 2$
- T_2 saturated: $V_{SD2} \geq V_{SG2} - V_T(p)$ i.e. $V_o - V_T(p) \leq V_i \leq V_{SS} - V_T(p)$ $V_o \leq V_i + 2$
- Simultaneous saturation at unique $V_{i(sat.)}$ i.e. $V_{i(sat.)} = 5V$ for $k_p = k_n$

So, if it is 0 volt or 2 volts. So, 10 minus 0 volt or 2 volt it is sufficiently small and it was channel is positive channel is formed. So, for which T2 remains on - ok. So, this is what you see over here. Next, the other case when the input voltage is more than that 8 volt that we had talked about, more than 8 volt; that means, the p-channel - it does not get then properly formed - it is below the threshold voltage. So, when V_i is greater than 8 volt - ok.

So, V_i is greater than 8 volt (Slide correction: $V_i \geq V_{SS} - V_T(p)$) - what is happening? T2 is off, but at that time definitely the n-channel has got the voltage which is more than the threshold voltage. So, for which T1 will remain on. So, these are the two cases, two extreme cases we have seen and you have already noted earlier, in case of that NMOS logic inverter discussion, that the pinch-off occurs when V_{DS} is equal to V_{GS} minus V_T we remember that for the NMOS.

So, whenever V_{DS} is greater than V_{GS} minus V_T, all right - that will be the saturation region then. So, this particular case, the when you map to this - the corresponding voltages right. So, this is happening when the V_o – right, V_o t is your V_{DS} and this V_{GS} is your V_i and 2 volt is your - the threshold voltage that we have considered for the NMOS also for the PMOS.

So, when this V_o is greater than V_i minus 2, the saturation for T1 occurs - ok. So, V_o is equal to V_i minus 2 is this line and V_o is greater than V_i minus 2 is this zone - ok. So, in this zone, in this zone, what we see that T1 is in saturation, T1 is in saturation and if we look at the corresponding thing for T2 when T2 will remain in saturation, just similar thing, but applied to PMOS. So, V_o less than V_i plus 2 - when it will be remaining in saturation, so this is the other case not sorry not of course, up to the you know this the threshold voltage up to this point. So, this will be the case when the T2 will remain in saturation. So, both T1 and T1, T2 remain in saturation in this zone and the rest of the zones are defined in this manner T1 in saturation, but T2 will not be in saturation; T2 in saturation, but T1 in not in saturation ok, this is the other two.

So, when T1 and T2 both are in saturation and we apply the equation that we have shown before. So, we get a unique solution for the voltage when both of them are in saturation and if you know - use these particular values, so we get that for 5 volt for the transistor parameters of both of them called k_p and k_n will be in this being same - which signifies, which implies that there is an abrupt jump at this particular voltage 5 volt, in the inverter characteristics. In actual practice, it will be little bit tapered - it will not be an abrupt jump like this.

So, this is how the CMOS transfer characteristics - it works and from that we can define V_{IL}, V_{OH}, - right; V_{OL}, V_{IH} all those things can be defined; for example, V_{IL} in this particular case definitely, we can consider up to say 2 volt or even little bit more than that

ok. So, similarly the V_{IH} is you can see that is relatively higher, which is an important thing to be noted. So, V_{IH} is more than 6 volt in this particular case that is that would be of you know for us to you know certainly consider - ok.

So, this is the kind of thing which is happening for this particular values that we have considered - right and accordingly, the manufacturers will tell you for different supply voltages, you remember the CMOS works over a very large range of supply voltages. From 3 to 18 volt compared to near about 5 volt for TTL based logic gates.

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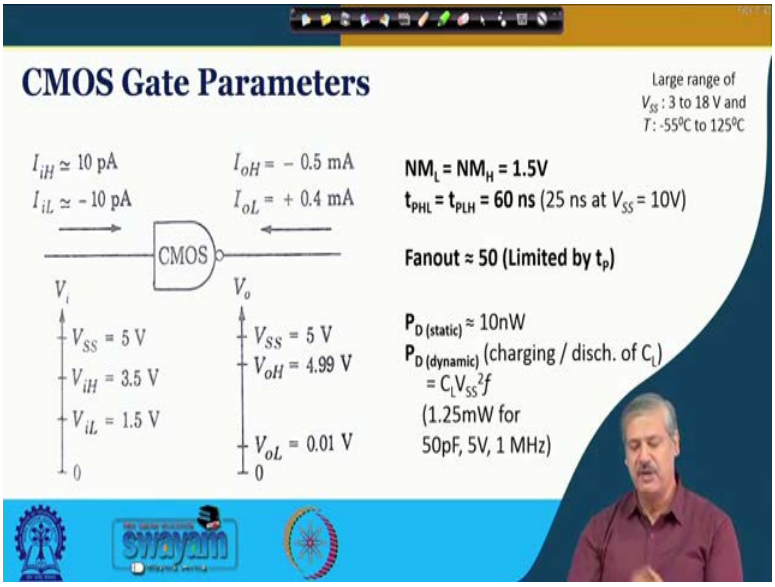

So, one particular example for a 5 volt supply case is the - different kind of parameters that you get. So, as we said the supply voltage is say, 5 volt. Then, corresponding V_{IH} is 3.5 volt - 3.5 volt that is what is considered, if it is 10 volt you know almost equivalent to that is 7 volt, I mean, that region. So, 8 volt is the case when the other region that we are entering into, the fifth region that we entered and V_{IL} is 1.5 volt that has been considered, V_{SS} is 5 volt V_{OH} is again almost equal to 5 volt - ok.

When this is for V_T is equal to 1.5 volt and if we go back -so, this is your, the corresponding V_{OH} the 10 volt - it is the almost 4.99 volt it has been considered and corresponding V_T is 1.5 volt. So, these are the different things if you can compare from the previous diagram for a different kind of V_{SS} and V_T – ok, so - which is coming from the manufacturers a specification and the other important thing to be noted here are the current level. The current levels are very small. So, the input current is 10 pico ampere and a minus 10 pico

ampere. So, basically the two cases when it is high or low and the corresponding meaning we all understand that it is going into is positive and going away is negative and similarly the I_{OH} and I_{OL} - the amount of current it can deliver or it can sink.

So, these are the two important parameters for us to take note of. And, accordingly the noise margins are calculated by the standard formula and for another important parameter is the speed, that is the propagation delay for output going from high to low or low to high which we can see is relatively higher compared to TTL and of course, if the supply voltage increases the speed becomes faster - ok.

So, that is another important point that we take note of. Fanout is not limited by the current it can deliver which we saw in case of TTL, but amount of propagation delay it can handle. Static power consumption is very low this is another important characteristics and dynamic power you know consumption is one important consideration here which is one part is there that half C V-square, right - during charging and discharging the similar power consumption is there the same half C V-square.

$$P_{D\,(dynamic)}\ (\text{charging / disch. of } C_L) = C_L V_{SS}^2 f$$

So, together it is C V-square that you can see and as many times it is getting charged in, charged and discharged in 1 second - given by the frequency of operation - right. So, together you get the dynamic power consumption because of the output capacitor is getting charged or discharged and this power that is getting you know consumed during the transition period that brief time that you have seen when both of them are active. So, that being very abrupt and so we can neglect that. So, roughly it is guided by this power that you see over here and with the higher high frequency it becomes - it comes in the range of milli watt and becomes compatible to TTL that is we take note of here, fine.

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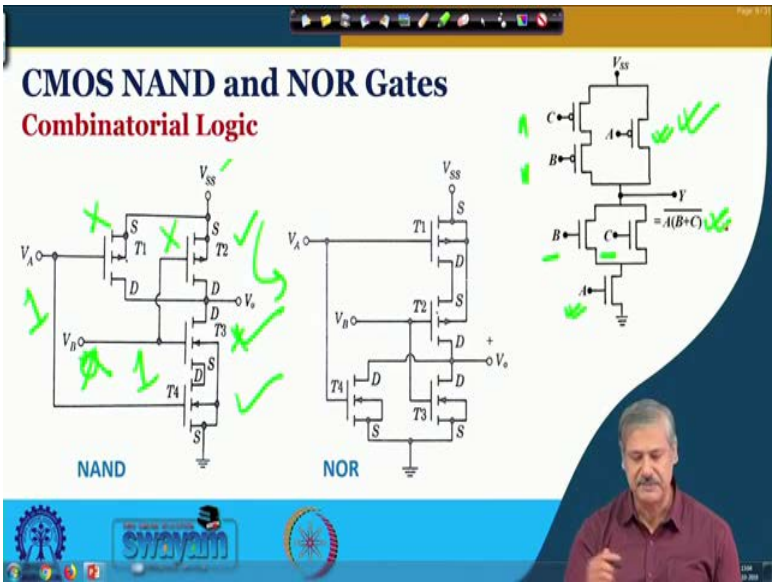

So, we go to - this is one beautiful thing about this MOS based gates - ok. So, when we look at development of NAND gate or NOR gate or you know combinatorial logic - we would not read need resistive elements and other things that is - that was there in a BJT based you know circuit development.

So, in NAND gate development CMOS we need for every NMOS another corresponding PMOS to get the advantage of the CMOS circuitry. So, NAND gate development, we have two NMOS in series and the corresponding PMOSs are in parallel - ok. So, any one of them is low, any of the any one of them is low what is happening 0 so VA is 0.

So, this is in series. So, this path will not be there this path is block. So, this is blocked by this one right when say this is 0 this is 0, but at that time the corresponding V_B. So, this is 0 means this is now, this the PMOS on is on right. So, the output is getting the V_{SS} over here through this - ok. So, the output will be high is it clear so, any one of them being 0.

So, there is a parallel path here at the output providing the voltage and the current, the power supply and in the series any one of them is blocking it - one of them is blocking it ok. So, that is how what happens so, when it is both of them are 0 and when both of them are 1. So, this is 1 and this is 1 high.

So, this is on, this is on right and this is off as well as this off it is how the PMOS will work. So, this is connected to the available to the ground is available over here ok. So,

logic low voltage is available - is it clear? So, that is how the NAND works. NOR is similar - so, these two will be now in parallel and the PMOS will be in series – right; and extending it further we can develop many kind of combinatorial logic by different combination of this.

So, this is also something by which people are, you know, which is - drawing becomes a bit easier. So, this presence of bubble over here actually signifies PMOS. So, this is a symbol of a PMOS in that fashion and this is the symbol of an NMOS absence of this ok. So, these two are in parallel and corresponding these two are in series, this is in series with the other one.

So, the whole of it the corresponding - what corresponds to B and C, what corresponds to B and C in PMOS – right; so, that will be in parallel with what is there as A over here. So, that is how the combinations are formed. And, this particular combination – right; so, this is B plus C ANDed with A right and there is that inverter.

So, that is how you get the logic and many such combinatorial logic can be developed by simple interconnection of this which is much easier compared to what you had seen in case of other logic family that we had discussed - ok.

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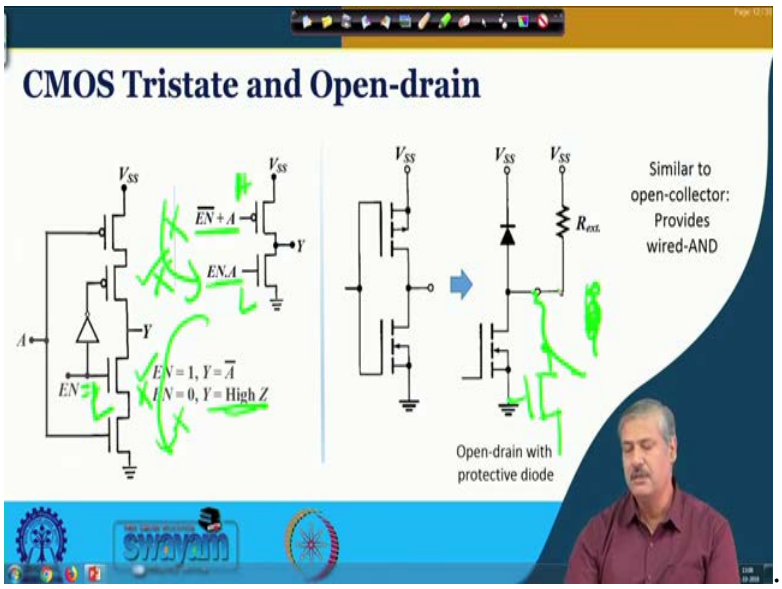

Now, if we take this a bit further. So, in the left hand side what you see is a circuit – right, where the NMOS an NMOS over here is in series with 2 PMOS that you see, they are not in parallel.

If they are in parallel, then they would have been a NAND logic forming, the other thing that you see here at this input between them there is an inverter present - ok. So, what is it what does it do actually? So, in the inverter, this input EN is 1 – ok; so, this NMOS is on and this is inverter means this is low - ok, if this is high this is low, this low means this PMOS is also on at that time - ok.

So, the output will at that time will totally depend on whatever is the input - ok. So, when EN is equal to high, so this is on this is also on and output follows the input if there is an inverter logic - so it will be the inversion of it. But when input EN is low, what is happening? This is you know, off and this is also off because it is at that time this is high - for a PMOS makes it off, right. So, both of them are off.

So, irrespective of the presence of A, the output is neither high nor low, neither you can drive that is not nor it can sink that is not possible ok. So, this is the condition we say is tri-stated which is neither high nor low and it offers high impedance, it is electrically offering very high impedance.

So, similar thing can occur if we have a circuit like this the previous stage is enable bar plus A; that means, enable complimented OR A and the NMOS is given by enable ANDed with A we will see when enable is 0 - ok, then this is 0, right and this is 1. So, the output will be this will be high and this will be low which will ensure that both of them are off. So, output is electrically isolated offering high impedance and only when enable is high – right, it is A which decides the output, A could be many other things from the previous stages.

So, these are the tri-stated configuration using CMOS and this is open-drain. So, open drain - how it works - similar to open collector. So, only thing, only issue is that this PMOS now when is replaced by the external resistance, the pull-up resistance there is a protective diode which is used in this particular case. In CMOS circuits, this protective diodes are there in input stages as well to avoid surges because the static voltage is a very problematic thing in CMOS based circuit. And, this one - another stage, another stage is over here

which is when it is connected - another such say wired-AND, you know another such circuit which is you know connected over here - ok.

So, then the logic together is providing wired-AND similar to open collector. So, this is what we take note of from this particular discussion.

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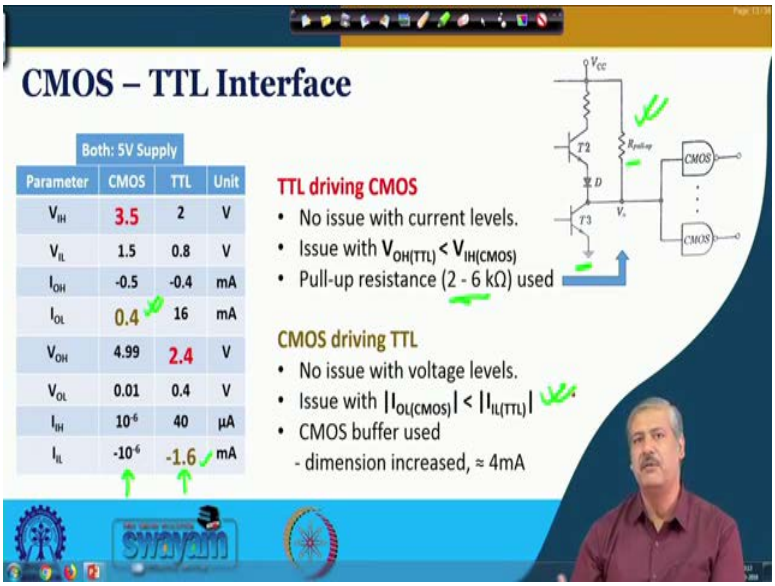

Finally, at last part of our discussion - CMOS circuits are there, TTL circuits are there, could be cases when for less power consumption more packing density we are preferring say, CMOS right and higher speed and associated benefits we are thinking of using TTL and then we want to in connect these two parts for getting both the benefits. So, then we need CMOS and TTL interface - right. And, to get a CMOS and TTL interface, when both of them are using say 5 volt supply, the corresponding parameters for input V_{IH}, V_{IL}, I_{OH} and all.

So, this is what I have taken from the transfer characteristics that we just discussed - right and TTL we have - I have taken from the earlier lecture we had. So, these are the two columns where the different parameters have been put forward.

So, when TTL drives to CMOS. So, TTL drives CMOS, when you compare you find that no issue with the current level because the CMOS because very less current of the order of pico ampere and voltage levels are also fine. Except only one case where the $V_{OH(TTL)}$

right - $V_{OH(TTL)}$ which is of the order of say 2.6 volt in our earlier discussion we have seen from the transfer characteristics with loading it can go up to say 2.4 volt or so.

This is your V_{OH} that is the output high and, but the input voltage that is required by CMOS for the input to be considered high is 3.5 volt for 5 volt cases - right and 10 volt cases, we have seen above 7.5 - 8 in that range ok. So, we are comparing because both need to have being you know, same power supply 5 volt for the compatibility. So, 5 volt is what we are considering here.

So, this is higher right. So, that is what is only the problem otherwise there is no issue in connecting CMOS load to TTL and for that what people use how to - how it is overcome! It is overcome by having this is the TTL stage, this is output stage ok. So, having a separate pull-up resistance, external pull-up resistance that you see over here – right, which actually increases this voltage level more than what it was in - what you can get in normal TTL cases - ok.

So, the voltage will be V_{CC} minus whatever IR drop, voltage drop is occurring here which will be more than the required 3.5 volt and this voltage - the resistance it has been seen to get voltage higher than this 3.5 volt is in the order of this 2 to 6 kilo ohm, this kind of resistance would do - ok.

So, this is what is required and when CMOS drives TTL right. So, CMOS is the say TTL is the load side. So, again if you compare the voltage levels and all we will find that there is no issues with the voltage levels. So, the issue is there, the current it can sink - ok. So, the current it can sink in the case I_{OL} CMOS.

So, this is the current it can sink 0.4 - ok. So, it is sinking. So, that is why it is told positive and I_{IL} when input is at logic load right the current it is coming out of the input transistor of the CMOS is of - this minus 1.6 milli ampere. So, this is much more - right. So, if you just connect it. So, this is going to give problem.

So, to overcome that, what is used is a CMOS buffer only. After the CMOS gate, another CMOS gate will be put with appropriate dimensions - larger area or so, which will enable more current to get sunk - ok. So, by which in some standard IC, is made by manufacturers- so, Texas Instruments and others, so, it has been seen that the current that can be sunk is of the order of 4 milli ampere which can take 2 standard TTL or so and if it is a low

powered TTL more such gates can be connected. So, this is how the interface has to take place - issues I have mentioned and it the issues are coming from comparing the transistor parameters - for the gate parameters for these two cases.

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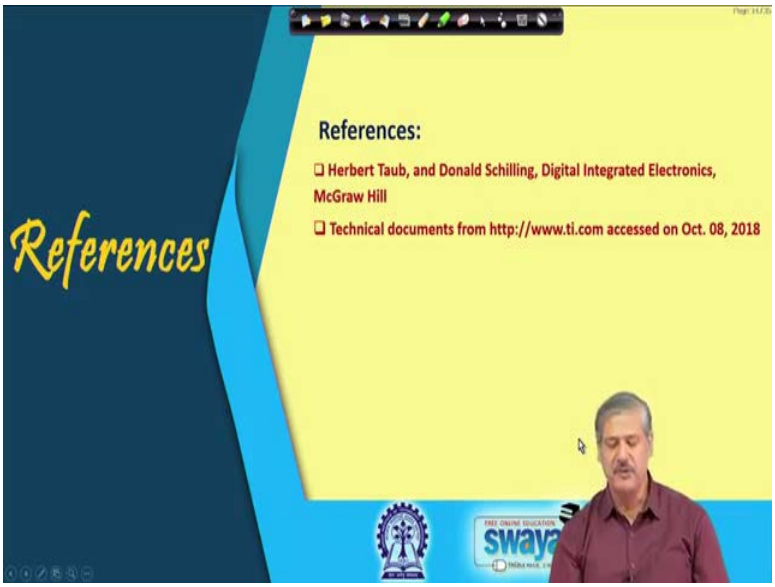

So, references are mostly taken from the first one and some technical documents.

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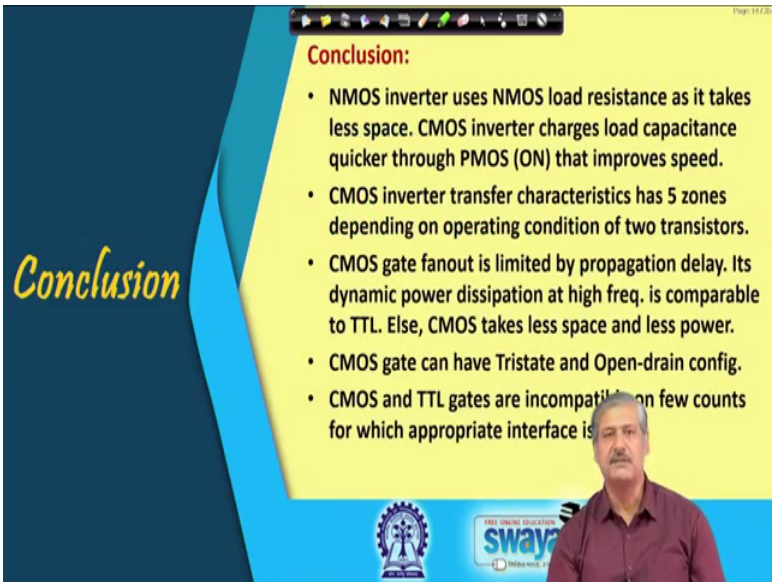

And to conclude what we have seen that NMOS inverters can be used, but NMOS load resistance is preferred for less space and CMOS inverters are useful in the sense that the charging and discharging are quicker and also it takes the static power - there is no static

power consumption and if you look at the transfer characteristics, there are 5 zones depending on operating condition of the two transistors whether they are in conducting or non-conducting, if it is conducting whether it is a linear region or saturation region.

The fanout is not limited by amount of current, but the propagation delay - amount of propagation delay we can tolerate and - because more such things connected, more such capacitances will come in parallel. Dynamic power dissipation is the important consideration and it becomes a bit TTL comparable at higher frequency and it can have tristate and open drain configuration and TTL and CMOS gates are incompatible on few counts, not all the counts and that can be appropriately taken care of when TTL and CMOS gates are to be interfaced with one another.

So, with this we end the week 1, the first module because of the time flag and other things certain things we have touched in a manner for which greater discussion and the references can be referred to or supplementary materials can be also considered.

Thank you.