Digital and Electronic Circuits
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Lecture – 43
Cascading: mod-2, 3, 5 to Mod 6, 10, 1000 Counter

Hello everybody. In the last two classes, we had discussed synchronous and asynchronous counters, up and down counters with modulo number-8 and we had seen how it works even for modulo number 16 right. And we can of course understand that how it will work for modulo number 4 also ok, though the basic circuit that we had discussed for 8 and one example we had seen for 16 right.

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So, this is where the you know the modulo number was on in the integer power of 2. So, in today's class, we shall look at some other modulo number like modulo 3 counter, modulo 5 counter and then we shall look at the effect of cascading.

I mean if we cascade one counter with the another counter, we can get an a modulo number which is if you just multiply them, then whatever the value, so that modulo number will come up ok. So, we shall look at such arrangement ok.

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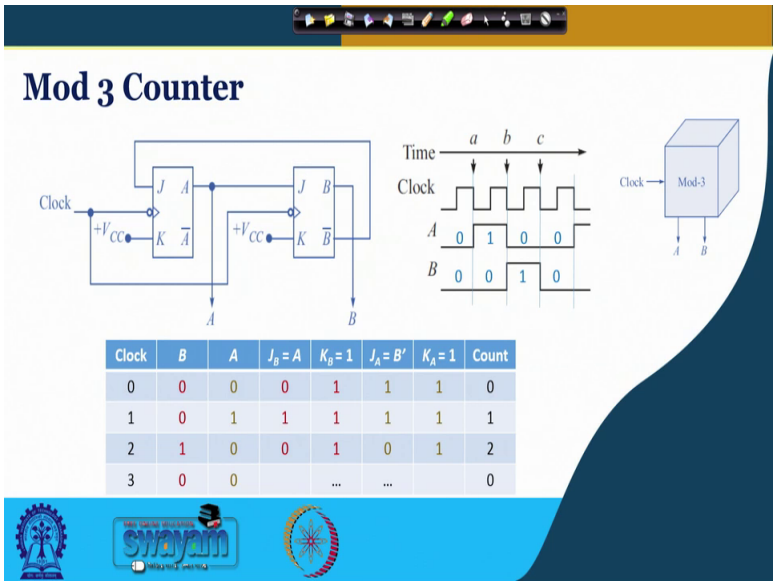

Clock	B	A	$J_B = A$	$K_B = 1$	$J_A = B'$	$K_A = 1$	Count
0	0	0	0	1	1	1	0
1	0	1	1	1	1	1	1
2	1	0	0	1	0	1	2
3	0	0		...	...		0

So, we begin with mod-3 counter ok. So, let us see the circuit of one mod-3 counter right, so it is made up of JK flip-flop right. And it is synchronous the clock is fed here right. And in this B bar is fed here as J input of A flip-flop ok. And A output is going as J input of B flip-flop all right. And K input for both the flip-flops are connected to logic high ok, very simple circuit the you can see all right.

Now, let us see how this circuit behaves; how this circuit behaves ok? So, initialised with 0 0, so this is the clock right. So, 0 0 then at that time your J B, K B and K A is always 1, this is permanently connected to one all right. So, J B is A, so A is 0 means, J B is 0 right. And what about J A? J A is B bar, B is 0 all right. So, this is 1 ok. J A is B bar all right, it is feedback like this ok, so this is 1.

So, after the clock trigger, what will happen? So, this is 0 1 right J B, so it will remain at 0, and this is 1 1, it will toggle from 0, it will come to 1, is it clear. From 0 0, we have come to 0 1. We are analysing a sequential circuit right. Now, when it is like this, so J B now, because A has become 1 right, so J B is 1, K B is always 1, J A since B is still 0, B is still 0, it remains at 1 and this is 1 right.

So, next clock trigger, both the flip-flop toggles. So, 0 becomes 1 and 1 becomes 0 right, this is the case. After that what happens, J B is A means, the 0, this 0 comes here and J A is B bar, so B is 1, so it is 0. So, this is 0 1 and this is 0 1 ok. So, it will after clock trigger

what will happen, so both of them will get 0. So, we are having 0 0, 0 1, 1 0, 0 0 ok, this is visible in the timing diagram also.

So, once it goes to 0 0, the cycle will continue. Cycle will repeat, after 0 at 0 0. After 0 0 0 1 will come and 1 0 will come ok. So, this is the mod-3 counter that you can see. And in this case; in this case if you take the output from flip-flop B ok, so every 3 clock pulses, it will remain high for one clock period is not it.

So, the regarding, the decoding logic and all, this B flip-flop output directly gives you the output that a count of 3 has taken place and it will remain I for 1 clock cycle right. So, with not need any separate circuit for that ok, is it clear. So, if we put this thing as a mod-3, you know block like this right with in which we know that this is the circuit, this is the way the circuit behaves ok. So, 0, 1, 2, again 0, 1, 2, this is way the count goes on.

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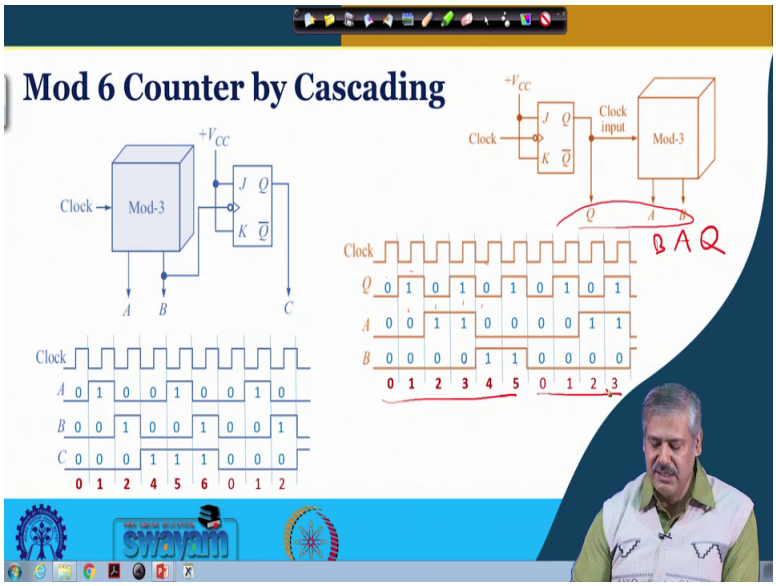

If that is the case, then let us see if we connect a mod-3 and mod-2, mod-2 you all know right 2, 4, 8, 16 right. So, mod-2 means only one flip-flop at its output, it is divided by 2 right, so that is mod-2 counter.

So, if mod-3 and mod 2 put together, what happens ok? So, there are two arrangements, what in the first arrangement, first we have putting the mod-3 ok. And the B flip-flop which is going high and remaining high only for 1 clock period for every 3 clock pulses

ok, so that is the that B output is fed as clock to the next flip-flop that is the mod-2 counter right.

So, in this case, what happens? In this case, this is your A and B, which is changing as 0 0, 0 1, 1 0 right. After that again 0 0 from the previous discussion on the previous slide right 0 0, 0 1, 1 0, right a count of 3 has taken place again 0 0, 0 1, 1 0, again 0 0, 0 1 ok, 1 0, because count of 3 has taken place, so it is repeating right.

Now, every time B goes from high to low. So, B goes from high to low over here, B goes from high to low here, B goes from high to low over here. So, this Q which is written as C here ok, it toggles ok. So, it toggles means, so C was 0 initialised with 0, so it becomes 1. So, it will remain 1, till it gets next negative edge of B right over here. Then again it will be become 0 and then it will continue is it fine.

Now, if you look at this 3 flip-flop output together C, B, A ok, the unique states they define for this clock pulses that is fed over here ok, then what are those unique states? So, put together you can see 0 0 0, 0 0 1, 0 1 0, 1 0 0, 1 0 1, 1 1 0, then again 0 0 0, 0 0 1 comes right is it fine. This what you see, if you read it along this line C, B, A this way right.

So, you have got 1, 2, 3, 4, 5, 6 6 unit states unique states, after which it repeats. So, what a what does it mean, it is a mod 6 counter right, according to the definition of modulo number of the counter. See it is a mod 6 counter and what are the counting states 0, 1, 2, 4, 5, 6 again 0, 1, 2, 4, 5, 6. So, this is the way it will continue, is it fine.

Now, for a mod 6 counter given the mod-3 counter was giving you 0, 1, 2 and then again 0 right, you may think that can we get a mod 6 counter, which is 0, 1, 2, 3, 4, 5, so 6 unit states the count value, then again it becomes 0 ok. So, this arrangement does not give you, the previous arrangement see it gives you 0, 1, 2, then 4, 5, 6 ok, 3 is missing right. There are 6 unique unit unique states, but it is missing.

Now, if you put the mod-2 counter, before the mod-3 counter, then let us see what happens ok. Since, we have already defined A and B, mod-3 counter here as A and B, so we are just keeping it that Q right. Otherwise, you write C also, but to avoid, so in this case it is you know the order is different it is A, B, C. So, it will be B, A,Q ok, so, this is the MSB to this is your MSB ok, and this is your LSB.

The clock is fed here the one, it will change faster is compared to the others actually is your LSB right. So, and the MSB changes slower, so B will be the one like this. So, coming back to these discussion mod-2, before mod-3. So, this Q changes in every clock negative edge right this negative edges, it is changing 0 1, 0 1, it is toggling right. Now, for this mod-3 counter for a forget about these clock time being. So, this is the clock, this Q is now fed as clock here, at it is negative edge, it will behave like a mod-3 counter right. So, it will give you, so this is one full clock cycle for this particular mod-3 counter.

This is another full clock cycle, this is another full clock cycle. So, 0, 0 1, 0 0, 0 1, 1 0, again 0 0, 0 1, 1 0, this is the way it will continue right. So, one clock cycle full cycle for Q which is fed here as clock is 2 clock cycle over there, so that is why, you can see 0 0 is therefore 2 clock cycles. (Refer Time: 10:08) 1 1 again for 2 clock cycles like this ok, because it this Q is a d divided by 2 ok, in terms of the frequency compared to clock right.

Now, if you do the reading from B, A, Q, as I said MSB is your B and A is this Q. So, 0 0 0, 0 0 1, 0 1 0, 0 1 1, 1 0 0, 1 0 1 and then again 0 0 0 is coming ok, so that is the way you have to read the data, then you can see 0, 1, 2, 3, 4, 5 again 0, 1, 2 right. So, it is up counter without any skipping any counting value right. So, this is the way, you can get mod 6 counter by cascading mod-3. After that mod-2 and also mod-2, after mod that after mod-3 ok and the counting states value will be like this in each of the cases.

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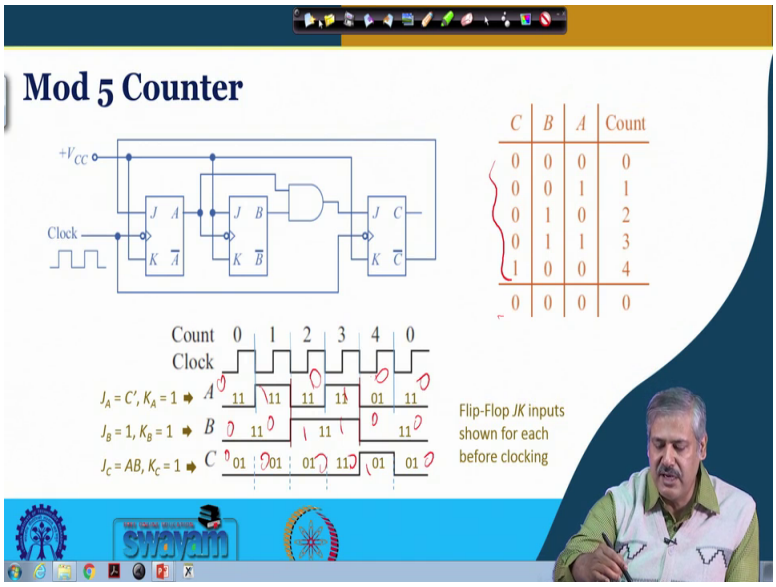

Now, let us look at mod-5 counter one arrangement, again there could be many different way, it can be made. So, there could be other than JK flip-flop other circuit as well right, even with the JK flip-flop there could be different arrangements. So, this is one arrangement ok.

So, in this what you can see that K A, K B, K C right, all of them are permanently connected to V C C right. J A is connected to C bar; J is connected to C bar, you can see right. J B is also connected to 1 right, but J B is fed by A ok. How that happens, how that effects and all that we shall see in the timing diagram ok.

And J C is fed by A and B, A and B fine. So, this is the initial circuit that we see. And then we shall examine, how it behaves like a mod-5 counter right. So, here the A flip-flop will toggle ok, whenever these the inputs are 1 and 1, so that is the case in the beginning, when this C is equal to 1, I mean initialized with all 0 0 0 ok, this all are 0, so this is 1 right.

So, what I have written here, this in this notation. So, these are the J and K ok and flip-flop JK inputs are shown for each before clocking. so this one is there right and this is permanently connected ok. So, then A will toggle right, so A will toggle means, A will become from 0, it will become 1 right. Now, when a goes from 0 to 1, this flip-flop does not get the trigger. This flip-flop will get the trigger, whenever A goes from 1 to 0 at the negative edge of it, because it is an negative edge clock negative edge trigger right.

So, you can see for B flip-flop, there is no trigger flip-flop B flip-flop trigger is for these brown marks ok. These brown you know lines that is there which is associated with the negative edge of flip-flop A output flip-flop A output right. So, B flip-flop at that time will remain at 1 1 only input will remain at 1 1 only and the value will remain 0 for this clock cycle as well, because it was not got any clock trigger.

What happens to C right, C it is input is A B A and B, so the input is 0 right and K C is 1. So, this is always 1, so this is 0 1, so the out value will remain 0, this fine. So, after 1 clock pulse right what we can see, the values are 0 0 1. So, this is 1, this is 0 and this is 0 right. So, then this is one fed back here, so this will again toggle.

So, from 1 it will become 0 right, so that is what has happened ok. And when it toggles, these gets a negative edge, so B becomes from 0, it will becomes 1, so that is what you

have seen what you see over here ok. So, this is 0, this is 1 and for this flip-flop, the input is still 0 1 for which this is 0 ok.

Next again since C is still 0, so A will again toggle that is what has happened, so it has become 1 right. And at the unless the negative edge of clock come, so A come B will not change. So, B is remaining at 1 all right. And C before that it is only 0 and 1, because this is this a was 0, so it is remaining at 0. Now, at this point of time, what you can see that A is 1 and B is 1, so, this J A is getting 1 1.

So, then the next clock trigger what happens, next clock trigger the C becomes C is always getting the clock all right becomes 1 right. And before clocking of course C bar was 1, so A has toggled right. And there is a negative edge, so for which it has also toggled for which it is become 0 B has become 0.

Now, at this point of time since a C has become 1, so C bar is 0, you can see the input of flip-flop A is 0 1, so it will these output will remain 0 ok. And these output is also 0, because it is no negative edge ok. And at that time A and B, both of here this end input for which it is 0 and this is 1. So, this next the output C 0, so, we are coming back to 0 0 0 right.

So, now if you look at the timing diagram and now these values counting states. So, this is 0 0 0 right, 0 0 1, 0 1 0, 0 1 1, 1 0 0 and then again 0 0 0 ok. So, this is what you can see over here right. Again it comes back to 0 0 0, so what is it 5 counting states, and it is sequential increasing ok. So, it is a mod-5 counter clear right. So, as I said there can be other arrangement also, this is one arrangement.

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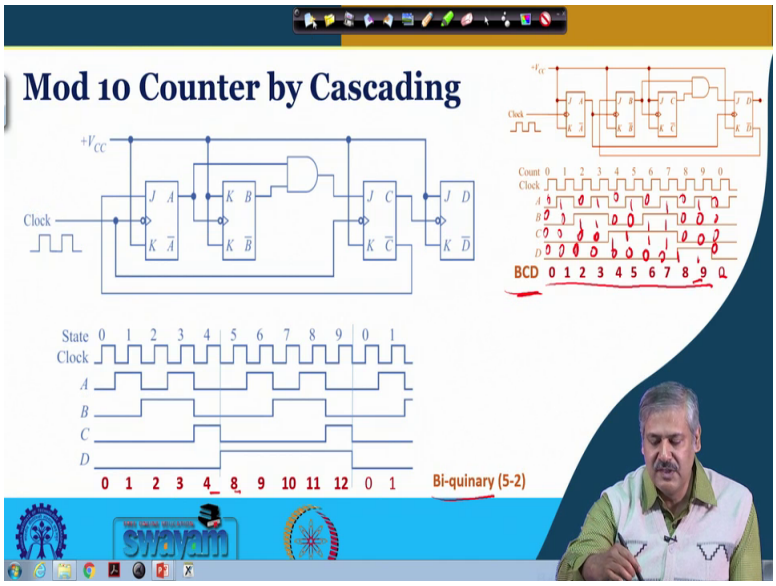

Now, what we expect to see the cascading, and getting mod-10 counter and like what we saw for mod 6 counter, where mod-3 and mod-2 were put together one after another. So, here mod-5 and mod-2 will put together one after another and we shall get mod-10 count that is what we expect right. And again there could be two arrangement mod-5 first, mod-2 later and mod-2 first, mod-5 later. So, these are two possible arrangements. So, we shall examine them.

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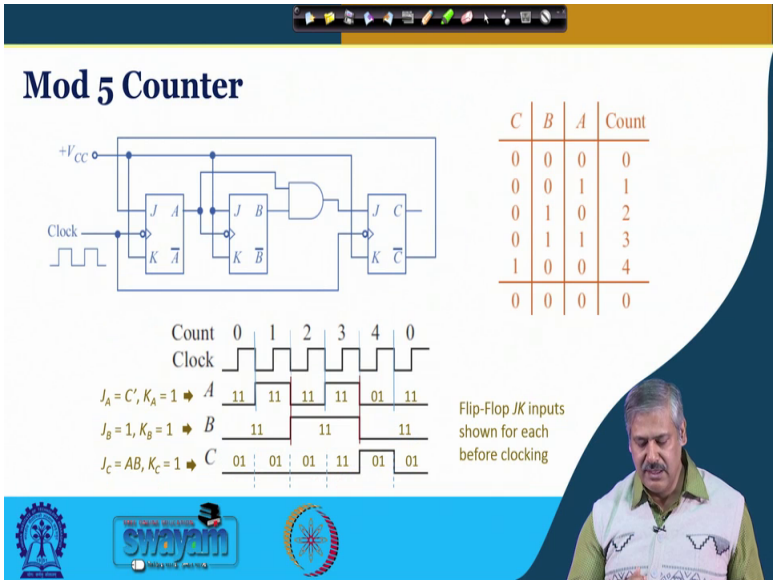

And before that, we also take a note that here C output is remaining at high for one clock period, in this particular arrangement ok. And so this can directly give you, this signalling that a count of 4 that is from 0 to 4 this has taken place 1 0 0 state has occurred right.

So, coming back so mod-5 followed by mod-2 ok. So, in this case the A, B, C, this the first one, this three are mod-5 counter, so 0 0 0, 0 0 1, 0 1 0, 0 1 1, 1 0 0 ok, then our again 0 0 0 is coming and so on and so forth right.

And at the negative edge of C; C is fed as clock here, it will toggle, flip-flop D will toggle ok, so that is what is happening at the negative edge of C, you can see that D has changed value. So, this is the negative edge of C. So, from 0, it was initialized with 0, it has become 1. Again the negative edge of C will come here. After the A, B, C, the mod-5 counter has gone through 5 clock cycles right 5 clock edges. So, again at that time it is coming from 0 1 to 0 and this is the way it continues ok.

Now, if you look at this state values, so 0 0 0 together that means, you are reading D, C, B, A together ok. So, this is in every case you put the 0 0, then after that 1, so this is 0 0 1, then this is 1 and it this way it will continue.

So, the first 6 5 values you can see 0, 1, 2, 3, 4, after that what has come 1 three 0's, 1 0 0 0 1 ok. So, 1 3 0 is nothing but 8 and this is 9 right. So, these are unique ten states 0, 1, 2, 3, 4, 8, 9, 10, 11, 12 unique 10 states right. But, the count value if you convert from binary to decimal and you know in that manner. So, these are 0, 1, 2, 3, 4, 8, 9, 10, 11, 12, again 0, 1, 2, 3, 4, 8, 9, 10, 11, 12, so this is the way, it will continue ok. But, this is a mod 10 counter because of 10 unique states that are there right.

And again if we for a you know mod-10 counter, the we would expect that number will be 0 to 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, the binary coded decimal are represented ok. For that what we need to do, similar to what we are done for mod 6 counter. So, we shall place the mod-2 counter first ok, followed by mod-5 counter ok.

So, now this mod-2 counter, we are naming it as A ok. And this we are naming at this mod-5 counter as BCD right and so this A is changing at every clock trigger right. And after that this A is effectively feeding as clock sorry this is not this one, if there was another like here. So, feeding as clock to the this 3 flip-flop BCD ok, the mod-5 counter,

and at this clock edge it will change from you know 0, 1, 2, 3, 4, 5 ok. So, this is the way it will go on right.

So, now if you look at the state values, so 0 0 0 0, then 0 0 0 1, 0 0 0 1 0 ok, 0 0 1 1, 0 1 0 0 ok, then 0 1 0 1, then 0 1 1 0, 0 1 1 1, then 1 0 0 0, 1 0 0 1 and finally 0 0 0 0. So, 1 0 0 1 means 9, after that again 0 has come ok. See you got 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, and then 0, 1, 2, again it repeats. So, this is mod-10 counter, but where the numbers are sequentially increasing and there is no such jump like from 4 to 8. So, this is called BCD counter, and this is called bi-quinary counter 5-2 counter ok so, 5 2 right.

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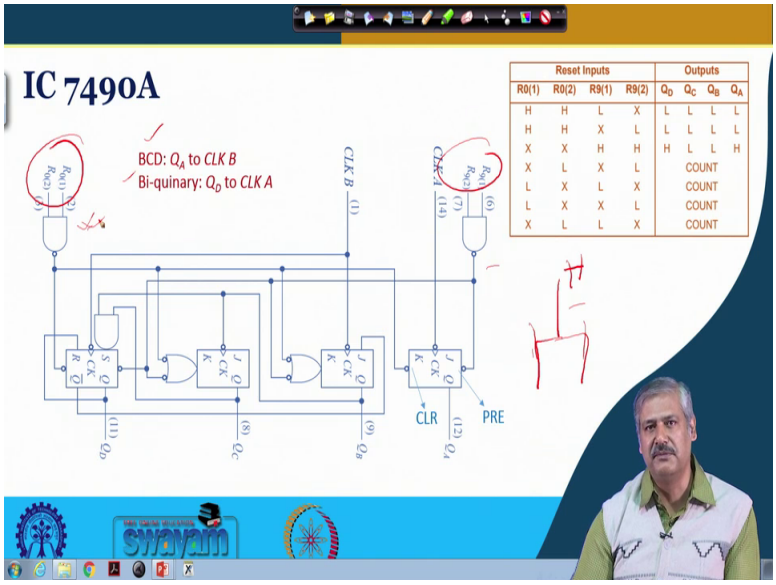

So, would like to see one IC 7490 ok, where we have a mod-10 counter implemented ok. So, IC 7490 A is one such IC right. And this IC has got a mod-5 counter over here right, and a mod-2 counter right. And you can see there are 2 clocks, this is one clock and this is another clock. This clock is associated with mod-2 counter and this clock is associated with mod-5 counter right.

Now, when you want to make it work like A, so we can make it work like individual mod-5 and individual mod-2 counter. So, for mod-2 give input here, output here, mod-5 we give input here, and we take the output from Q D right. All three of them is giving the counting states, but that a count of 5 as taken place the final signalling, if you required you know in certain sense that decoding of 1 0 0, we can take it from here right.

So, but if you want to work them work it as a mod-10 counter, we have to cascade one after another right. So, the cascading can be done, again one of the two ways that we have mentioned. So, if we want a BCD counter made out of it, so mod-2 counter should be first. And then mod 5 counter will be following.

So, at that time clock will be fed here right, the external clock which is getting counted or external event that triggered of which is getting counted. And this Q A need to be connected over here ok, then the circuit will behave like a mod-10 counter BCD counter right. And instead if we want Bi-quinary counter, then the clock will be fed here the external clock will be fed hereand this Q D will be connected to clock A is it fine right.

Now, comes there are 2 other inputs, 2 sets of other input you can say, this is R 0 1 and R 0 2 right, so when any one of them is low ok. So, this proper count is happening, I shall discuss with later. So, when a both of them are high, then this output is low, this output is low and it will be cleared all of them will be clear ok. So, the all the output will become low ok, so when both of them are high; irrespective of what is happening over here right.

Now, when irrespective of what is happening means, one of them remaining low ok, please understand that. So, when both of them are high ok, if one of them this R 9; R 9 means it is setting 9, so that I will come later. So, one of this input is remaining low, irrespective of what is happening to the other input, the output will be all this things will be asynchronously cleared right.

And when this two are high, this two are high, irrespective of what is happening at this places right. So, this particular 4 flip-flops will be loaded with 9 high, low, low, high, Q D to Q C using pre-set and clear. So, all of them has got a pre-set and clear input right is this two are not triggered, because there be only getting the clear value 0. So, these two flip-flop has got both pre-set and clear ok. So, this will be having your what is that called 9 will get loaded right.

And when any one of them are low, then for both the cases, the normal count will happen based on the clocking arrangement that we are having either BCD or bi-quinary. If we are looking for mod-10 counter, otherwise normal mod-5 or mod-2 counter, it will work is it fine ok.

Again we shall discuss in next class or subsequent classes that why, these two inputs and an internal logic gate has been put in this manner at that time, it will be clear. So, right now if we just need to clear it, you can connect one way and we can you know feed it to both of them and we make it high, it will become clear ok. Later on we will see how why how this two input and this internal logic gate will helpful in subsequent classes.

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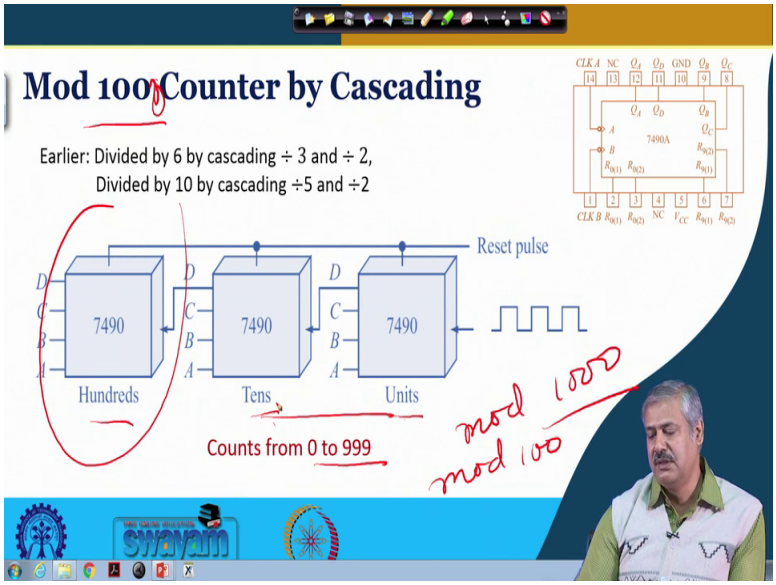

Finally, we can extend the way we were cascading in circuits to get higher modular number from 6 to 10. From now by connecting modulo 10 counter in cascade like this 7, 4, 9, 0 three of them, one after another ok. What we can get, we can get a modulo 100 sorry not 100, this is 1000 ok, please take a note of this modulo 1000 counter 0 to 999 ok, the count is possible right.

So, whenever this changes by 10, it gets a clock, I mean every time changes, there will be a negative edge available and similarly over here and similarly over here, so that way we can get a mod modulo 1000 counter available by cascading right. If we cascade two of this thing, not this one is say there, so it will get modulo 100 10 and 10 right is it fine.

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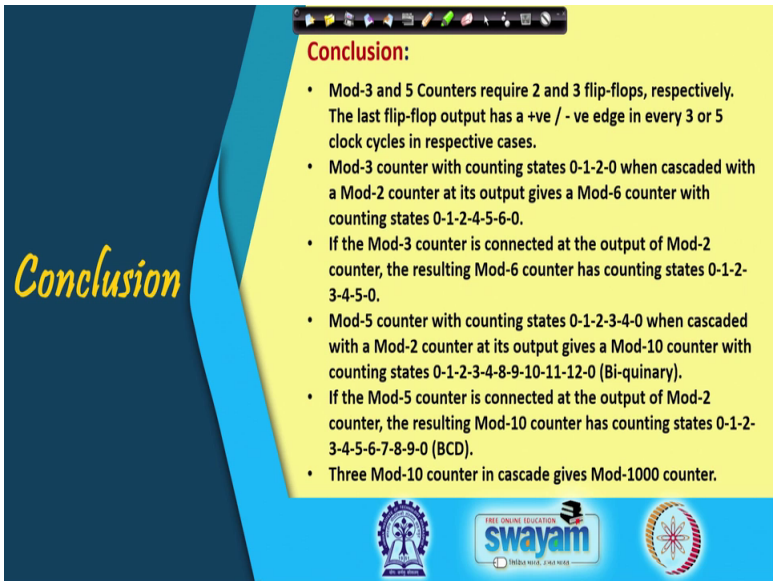

So, with this we conclude today's class, mod-3 and mod-5 counters we have seen required 2 and 3 flip-flops. And the way we have designed them is 0, 1, 2, 0, 4 mod-3 counter and when we have we are cascading it, we can get depending on whether mod-3 is there, before mod-2 or mod-2 is there, before mod-3, we can get 0-1-2-4-5-6-0 or 0-1-2-3-4-5-0.

Similarly, for mod-5 counter, we have the states counting states 0-1-2-3-4 in our in that circuit that you have seen. And when mod-5 and mod-2, we are putting them one after another the cascading cascaded circuit depending on mod-5 is before or mod-2 before, we have got bi-quinary arrangement or a BCD arrangement BDC count happening ok. And 3 mod-10 counter in cascade gives mod-1000 counter ok.

Thank you.