Digital Electronic Circuits
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Lecture - 04
Transistor Transistor Logic (TTL)

Hello everybody. Today we shall discuss more of Transistor-Transistor Logic.

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And we'll cover TTL transfer characteristics and different operating parameters, TTL open collector configuration, how it is used, TTL Tristate, and Schottky TTL.

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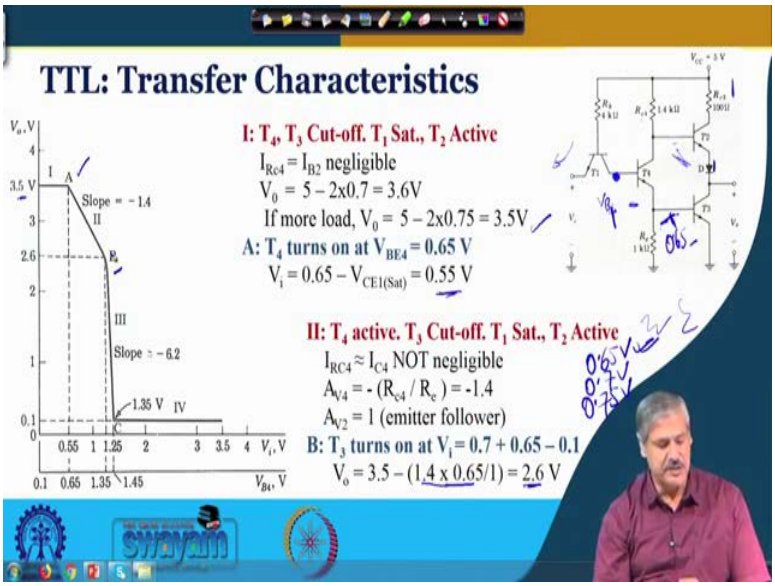

In the last class we got introduced to TTL, and there we ended by saying that a phase splitter - this is the phase splitter that we see is important when we talk about the TTL, when we talk about TTL activity, and the totem pole output configuration. So, this is what, how we ended in the last class.

And in this class we shall elaborate more on that. So, this is the phase splitter and also we mentioned that this resistance cannot be made 0. So, this was there in the last class, we made a note of it. So, in this particular thing we look at the inverted characteristics, this is the inverted characteristics. There are 4 distinct zones, ok. So, we shall discuss each one of them turn by turn, and the first thing when we, what we start with is the case when the input voltage is 0, ok. So, this V_i is 0, there is a difference to V_{B4}, this particular voltage - this is V_{B4}, that we shall discuss little later. So, this is your V_B, V_{B4}, ok.

So, when here is 0 - what is happening? Current is going in this direction, current is going in this direction - right. And this transistor, the base current is very small the collector current is also accordingly small. So, this transistor will be having more of I_E, ok. So, it will be firmly in saturation - right. And when it is in saturation - current is going in this direction, so this transistor does not get enough current to be on so this T4 is off, in cut-off. And when T4 is off, no current is flowing through this. So, T3 is also in cut-off, ok. So, these are the two things that we can see, T1 is of course in saturation.

What happens at the time to T2? T2 at that time is on, and the current that is flowing pastd this T2 depends of course on the load because T3 is off - whatever current is flowing past here, it depends on the load current, ok. For a typical load, the current over here is the base current which is reasonably small. So, I_B and R_{C4} - this drop is small. So, accordingly the output voltage will be drop across this diode, and drop across this transistor, this base-emitter junction, ok.

$$I_{Rc4} = I_{B2} \text{ negligible}$$

$$V_0 = 5 - 2x0.7 = 3.6V$$

$$\text{If more load, } V_0 = 5 - 2x0.75 = 3.5V$$

$$\text{A: } T_4 \text{ turns on at } V_{BE4} = 0.65 \text{ V}$$

$$V_i = 0.65 - V_{CE1(Sat)} = 0.55 \text{ V}$$

So, typically, it is 5 minus 2 into 0.7 - 3.6 volt. For a large amount of current, if it is drawn by the load both of them can go into saturation. So, at that time these two drops will be 0.75 volt or so. In this particular discussion, this part of the discussion, we consider that the transistor when it just begins to be on, the base-emitter junction voltage is 0.65 volt – ok, just it starts operating; becomes active at 0.7 volt - when it is active and, when it is in saturation it is 0.75 volt. So, this is how we look at this base-emitter voltages for an approximate calculation of this transistor inverter characteristics, ok.

So, for that particular case, we have 5 minus 2 into 0.75, 3.5 volt will be available at the output when a load is connected and which is drawing larger amount of current. So, accordingly, find this point 3.5 volt at 0 volt what here in the transfer characteristic clear, ok.

Now, as the input voltage is increased, ok, - so, slowly, slowly, current might get diverted in this direction, ok. Now, when this V_{B4} is 0.65 volt just at this particular point, ok. So, what will happen - this T4 will turn on, this base-emitter junction will turn on, base-emitter on, this is what we have considered, ok. So, at that time 0.65 volt and this is the collector saturation drop that is 0.1 volt. So, at 0.55 volt of V_i what we see that T4 is just turns on. So, this is one big point A over here that we see in the characteristics - clear, ok.

So, now, we go to region II. So, this is the region II. So, in the region II, what has happened? T4 has become active, ok, so current as started flowing through this. So, I_{E4} and R_e this drop is there, ok, but this drop is not sufficient to turn this T3 on, it is still less than 0.65 volt, ok. So, what will happen at that time? Only this one will be on and T3 is then cut-off that is what is region two over here, ok. And at that time, at that time of course, since this has started conducting these drop is not negligible anymore these I_{Rc} - this drop across this R_{c4} is not negligible anymore, ok.

$$I_{RC4} \approx I_{C4} \text{ NOT negligible}$$

$$A_{V4} = - (R_{c4} / R_e) = -1.4$$

$$A_{V2} = 1 \text{ (emitter follower)}$$

$$\text{B: } T_3 \text{ turns on at } V_i = 0.7 + 0.65 – 0.1$$

$$V_o = 3.5 – (1.4 \text{ x } 0.65/1) = 2.6 \text{ V}$$

So, at that time, if you will look at the gain across this voltage gain across this T4, ok, so from our basic transistor amplifier principle - the gain is minus R_{c4} by R_e, that is the gain that we shall see in a configuration like this alright. And the gain that we can calculate this is 1.4 kilo ohm and this is 1 kilo ohm, all right. So, as we keep incrementally increasing it this particular transistor will offer a gain of minus 1.4 which you see this slope by which it is reducing. How long will it reduce? Ok, like this till this starts operating. When will it start operating? When this voltage is 0.65 volt. Plus minus.

When this is 0.65 volt, how much current is flowing over here? So, 0.65 volt divided by 1 kilo ohm, right. So, that is the current, and that multiplied by 1.4 is the voltage that will be the drop across this at that time, when it just starts operating. And at that time, then output voltage will be 5 volt minus 0.75, 0.75 minus this particular drop, so 3.5 minus this drop so that is the 2.6 volt. So, when it just begins to - become on, at that time this is the point that B is reached, that is your 2.6 volt and at that time the input voltage is 0.7 volt over here, and 0.65 volt over here, that is 1.35 that is V_{B4} - that is required, and minus the saturation voltage over here 0.1 volt, that is 1.25 volt, that is what you will see at this break point B, is it clear? So, this is the II zone - how it can be defined, ok.

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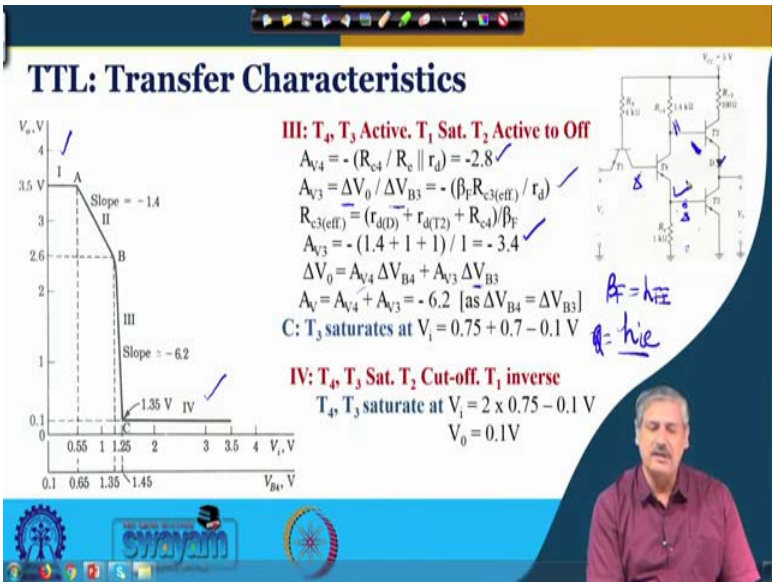

Now, we look at zone III, ok. So, in zone III, T4 and T3 both are active, ok. So, you are looking at this particular place. So, both of them are active. So, the resistance across this base emitter junction, which in h parameter term, which is defined as h_{ie} which you have defined here as r_d, resistance at base-emitter junction can be considered - as a diode resistance in that equivalence, ok. Otherwise those who are familiar with h parameter representation this is nothing but the h_{ie} in the h parameter - to put a representation.

$$A_{V4} = - (R_{c4} / R_e \parallel r_d) = -2.8$$

$$A_{V3} = \Delta V_0 / \Delta V_{B3} = - (\beta_F R_{c3(eff.)} / r_d)$$

$$R_{c3(eff.)} = (r_{d(D)} + r_{d(T2)} + R_{c4})/\beta_F$$

$$A_{V3} = - (1.4 + 1 + 1) / 1 = - 3.4$$

$$\Delta V_0 = A_{V4} \Delta V_{B4} + A_{V3} \Delta V_{B3}$$

$$A_V = A_{V4} + A_{V3} = - 6.2 \ \ [\text{as } \Delta V_{B4} = \Delta V_{B3}]$$

$$\text{C: } T_3 \text{ saturates at } V_i = 0.75 + 0.7 – 0.1 \text{ V}$$

So, this resistance will come in parallel with r_d, and because of which this gain will become R_e parallel r_d in the denominator, and R_{c4} in the numerator, ok. And r_d is of the order of 1 kilo ohm similar to this. Of course, the more current flows, we know the current versus

voltage curve, by which at higher current, the r_d value will come down. So, this will not remain exactly at this particular value, but gradually this denominator will become less, but for our calculation, approximate calculation, this is sufficient. So, 1 kilo ohm, 1 kilo ohm in parallel - that is 0.5 kilo ohm and we get the gain of minus 2.8 from this part, for this part of the gain, ok.

Now, when this one is conducting - is in active region, this is also providing a voltage gain, ok. So, these voltage gain is at the output with respect to voltage changes that is occurring at the base of T3. And, this can be calculated as the beta forward - that is again, this is your r_d, beta forward is nothing but that h parameter term h_{fe}, - h_{fe} or we know the current gain, that is the beta in the forward direction - forward active mode of the transistor, ok. So, at that time what is happening? So, these beta forward and the collector resistance at this for this particular transistor and the base-emitter across this - the resistor that is there, which is h_{ie} or r_d over here the way we have represented it, clear! So, this is the A_{V3}.

Now, this R_{c3}, effective R_{c3}, how do you calculate? You calculate as the resistance in - this resistance - diode resistance, this resistance - over this base emitter junction resistance, as well as this R_{c4} divided by the beta forward - is the effective collector side resistance for this calculation, which happens to be minus and if you just substitute the values - minus 3.4, ok. And the gain over here in this cascaded stage is gain forward coming from here change in delta V_{B4}, and change coming from this right – and, this delta V_{B4} and delta V_{B3} - the change over here and the change over here are same because of the emitter follower - that kind of you see - whatever change will occur the same change will occurr over here. So, effective gain is summation of these two and we get an approximate slope of minus 6.2 which of course, increases towards - when more and more currents are flowing, flowing through it, ok.

So, this is how the third zone occurs and the T3 saturates at, this particular transistor saturates at when this reaches a voltage 0.75 volt, ok. So, this is 0.75 volt, this is this saturates before T4 0.75 0.7, and at the input side minus 0.1 that is the voltage that you will see which is 1.35 volt over here, ok. Is it clear? This is the 1.35 volt that you see from the input side from V_{B4} side it is 1.45, ok. So, this is the point C, that is how it is defined.

So, V_i is still getting increased - what will happen? Now, T4 will go also into saturation and that is the voltage that kind voltage will be 2 into 0.75 minus 0.1, that will be the V_i at

that time and corresponding V_o will be 0.1 volt. And if you keep increasing the voltage then what will happen? This transistor will be working - this will be sending current in this direction, it will work in the reverse direction. This emitter will work as a collector and this collector will work as an emitter and the current will be going in the other direction – right; and for that the inverse beta will be very small value, ok.

$$T_4, T_3 \text{ saturate at } V_i = 2 \times 0.75 - 0.1 \text{ V}$$

$$V_0 = 0.1V$$

So, if you now look at the whole of it the normal stable operations - this is the region I and region IV, ok. And in this region I and region IV what we see - how this T4 conducts. So, in region I, we have already seen that T4 is off, when T4 is off this is high in terms of, you know, making this transistor on and this one is low, that is in region I. And the other stable condition is region IV; and at that time what is happening in the that particular condition; in region IV so this is in saturation, right. So, this time this is low in terms of making this on these two transistors on, and this is high in terms of making this transistor on, ok. So, this transistor is on. So, 0.75 volt, 0.2 volt here, 0.95 which is not sufficient to drive both this transistor, and the diode together on, so this transistor will be off, ok.

So, in that sense, in that perspective, they are - when one is low another is high on when one is high the next, the other one is low. So, they are remain out of phase in that sense, that is why it is called phase-splitter. And we have already noted in this particular zone briefly, this T2 and T3 both of them are active, for which there is a path from 5 volt to ground when both the transistors are, and diode is on. And there, the resistance over here, we need to make it some finite value, we cannot make it a 0 because, otherwise large amount of current will, you know, flow and power dissipation will be there, ok.

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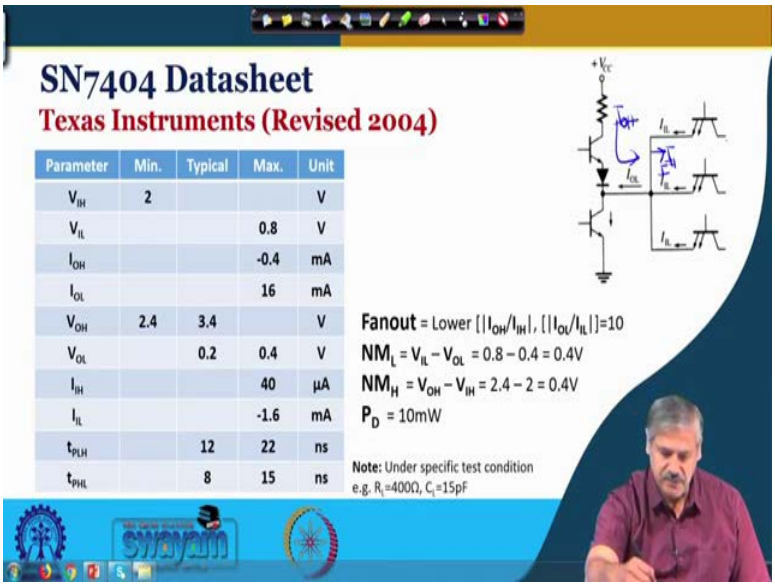

Now, we look at the - one practical, so I said that parameter was an estimated value. So, if you look at any standard manufacturers datasheet we shall see that how the TTL gate inverter 74 say, 04, what are the different parameters how that is been specified, ok.

So, we are already familiar with the terms like V_{IH}, V_{IL} and so on. V_{IH} is the minimum voltage at the input side which is considered as high, ok. Any voltage above that is considered as high - that is, no issue with that, ok. So, if we look back this previous one, so V_{IH} according to the manufacturer for different - considering the typical loading and all; so the value is considered for the minimum case is 2 volt, ok. So, at the input side when it is 2 volt and above right it is considered safely as - input is considered as high; that means, it will give, generate output which is low, ok.

Similarly V_{IL} input - maximum value of the input voltage which is treated as low, any voltage less than that will be treated as low. So, if you look back at this value. So, 0.8 is somewhere here, 0.8 is somewhere here, right. So, sorry, 0.8 is somewhere here. So, at that time the output is somewhere here, ok. So, any voltage less than that is treated as logic low, ok.

Similarly, V_{OH}, V_{OL} - all these terms we have defined before and these are the corresponding values that the manufacturer will give you, and from there what we can do we can arrive at the noise margin-low and noise margin-high as per the definition that we have discussed in the very first class, and in subsequent classes, and from that we can see

for the TTL the values are 0.4 volt and 0.4 volt, ok. This is according to manufacturer's datasheet.

$$NM_L = V_{IL} - V_{OL} = 0.8 - 0.4 = 0.4V$$

$$NM_H = V_{OH} - V_{IH} = 2.4 - 2 = 0.4V$$

In addition you can see the corresponding current values, for these different cases and one such calculation were we can one such thing that we can see for find out calculation here, is the case where you can see this is the totem pole output and similar gates have been connected at the output, ok. So, the I_{OL} all right, now when we talk about this you know these sign of the current, so any current that is going into is consider positive and going out off is considered as negative. So, I_{OH} is the current that you can see right which is which is considered positive. So, let us start with I_{OL} only because in these example I_{OL} is there. So, I_{OL} when the output is low the current that is being sunk in. So, current being sunk in I_{OL} is 16 milliampere.

So, that is the maximum current it can sink, ok. So, that is and - this is getting into, that is why it is positive, all right. So, this is the 16 milliampere and for the load side similar circuit that is there. So, I_{IL} which is coming out of it, what is the corresponding value according to the specification given by this? That is minus 1.6, it is because it is coming out of it, and it is getting into, right.

So, how many such then load gets can be serviced by this? So, this is I_{OL} by I_{IL}, all right. And the other case happens when this is off and this is on and the current is driven in this direction and this is in inverse mode. We know that this is going in this direction - inverse mode – so, that time the current that is at the load side, that is your I_{IH} is of the order of 40 microampere - the current that is going when this transistor is operating in inverse mode that is the beta I_B of T4, ok.

And corresponding I_{OH} which is coming from here that is I_{OH} in that case – right, for corresponding I_{IH}, ok. So, what is the value? That is given as minus 0.4 milliampere, ok. So, again it is going out so that is the say that is why the sense is negative sign is negative. So, how many such gate can be serviced? So, again you take the ratio all right and the finite will be lowered of these two numbers, and in happened to be case that the way the

circuit has been designed by the manufacturer it is 10 in both the cases, and for this particular gate, the power dissipation is of the order of 10 milli watt.

$$\text{Fanout} = \text{Lower}\ [|I_{OH}/I_{IH}|, [|I_{OL}/I_{IL}|] = 10$$

The other important parameter is the propagation delay. So, propagation delay high low to high, ok. The value you see 12 nanosecond and 22 nanosecond - it depends on the loading, ok, more such loads, more such capacitors will be coming in parallel and more time will be required, ok. And the other reason for which low-to-high is more compared to high-to-low - that we have discussed before - that the time it takes to bring it out of the saturation, which is more in case of the transistor getting driven into saturations from saturation to cut off - the charge redistribution that is required. In t_P high to low is the case when you have got the case, which is relatively low, and this is measured under some specific condition, ok.

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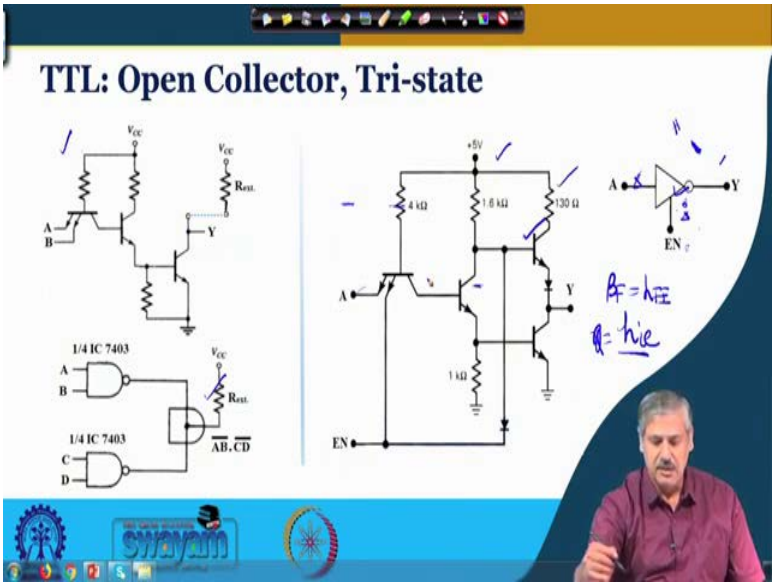

Now, TTL open collector - how does it work? So, in the TTL open collector, the last stage in the totem pole you do not have any resistance, ok. So, this remains open. So, to make it work we need to connect an external resistance to it, ok. So, this is the external resistance through it. So, this is called pull-up resistance also, ok.

Now, by varying this resistance we can vary the amount of current and if you are connecting say, a light emitting diode over here which requires more current and

corresponding resistance values can be decided here - to make it glow. So, that is one good thing about it.

The other aspect of this open collector configuration is that if you connect two such gates. So, this is a one gate right, and there is another gate and you are connecting just ANDing these two outputs. So, together if you just analyze you see that they will give a wired-AND connection. So, these two another such gates is there right and you just connect it over here it will give you a wired-AND connection which is also useful in some cases. So, this is one important thing about open collector configuration.

There is another use of TTL, the thing that we discussed earlier in terms of tri-state, ok. So, in Tristate; that means, the output is neither able to drive current, nor able to sink current, ok. So, that is called the tri-stated kind of thing, ok. So, neither high, nor low - it is kind of electrically isolated. So, when this enable is low logic low - 0 volt or so, what will happen? In this particular case you see for any of these cases, any of these cases this particular transistor will be - this current will be drawn in this direction. So, this transistor will be off, ok. So, this transistor is off. So, at that time this can become high - in earlier, in normal operation - right, but because of this diode the you know, which clamps the voltage to 0.7 volt and 0 volt over here which is not sufficient to make both of them on for which this transistor is also. So, both of them are off. So, in enable is 0, both of them are off in the totem pole output. Only when it is high, then it serves the normal operation of an inverter, ok. So, this is the tri stated TTL which is also useful in many circuit.

So, we shall look at - you know TTL NAND gates, you have already seen, alright.

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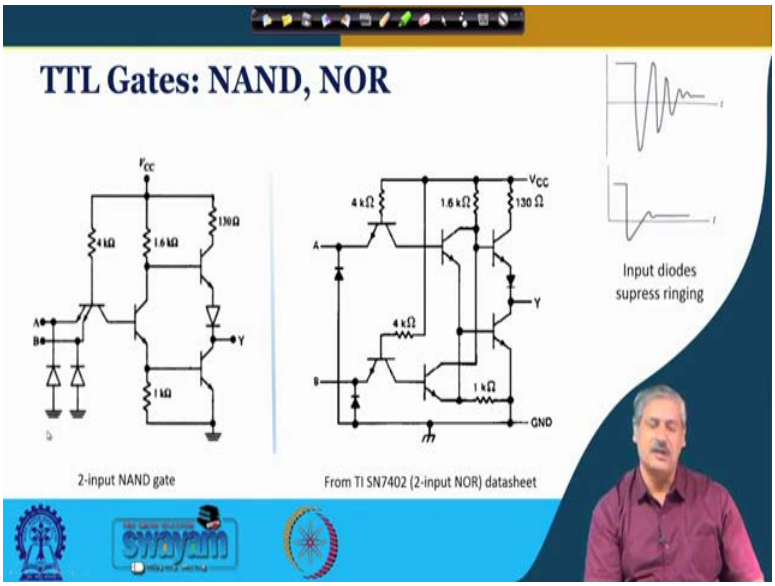

So, TTL NOR gate - if you look at the manufacturers specification. So, I have taken from a Texas instrument say, SN7402 technical document. So, what you will see here? These two input stages are in parallel and these two phase splitters are in parallel, and the totem pole part is common. And NAND gate of course, this is a multimeter NAND gate. So, this is how the TTL NAND gates and NOR gates are prepared, and the operation is known.

And you will see in these cases there is an input diode over here which actually prevents ringing due to you know transmission line transmission issues - termination issues. What can happen? When you are taking it from high to say low right, so it may not there may be a ringing. So, these diodes actually when it go sufficiently low this particular thing. So, it conducts and it takes away the energy. So, this is another important thing that we need to know in the as a practical case.

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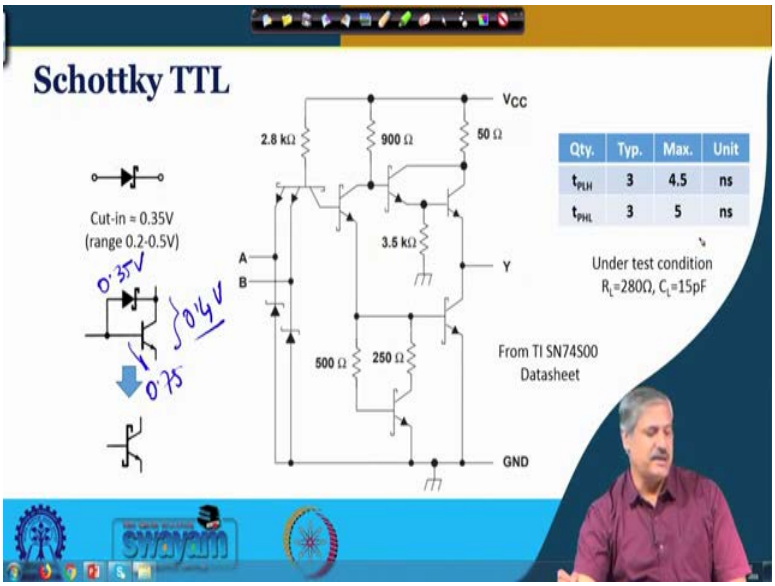

And the last topic that I would like to just mention here in today's class is the use of Schottky diode in the TTL configuration, ok. Schottky diode you know is a metal-semiconductor junction and it can provide a cut-in voltage in the range of 0.2 to 0.5 volt. So, this is clamp, this is used between base and collector of a transistor, and this transistor because of this, this voltage is clamped to say, 0.35 volt if you take - if you manufacture in that manner and this is your 0.75 volt. So, this is 0.4 volt or so, which prevents it getting into saturation, so as to say, ok.

So, just stop short of saturation which is useful in the sense that it helps in bringing it out of the saturation, the time - the switching speed increases. So, that is one important thing where all the transistor that are supposed to saturate right that are changed using a Schottky diode, ok. So, this is 74S00, again taken from the data sheet. So, you see this, transistors are changed by Schottky diode, ok.

In addition, over here what you see, is that earlier there was only a resistance, from this T 4 now there is an active pull-down. So, this helps in taking the charge from this base-emitter junction when it is coming out of saturation, I mean, whatever level it goes into the saturation. And the other thing over here what you see is a Darlington pair configuration over here and you do not need a diode over here, because there are two such things. So, it also helps in providing larger amount of current. So, this configuration over here together with the Schottky clamped transistors used - as a whole, increases the switching speed,

and the switching speed that we are get here is of the order of 3 to 4.5 nano second depending on the test condition and that is very useful for enhancing the transition speed.

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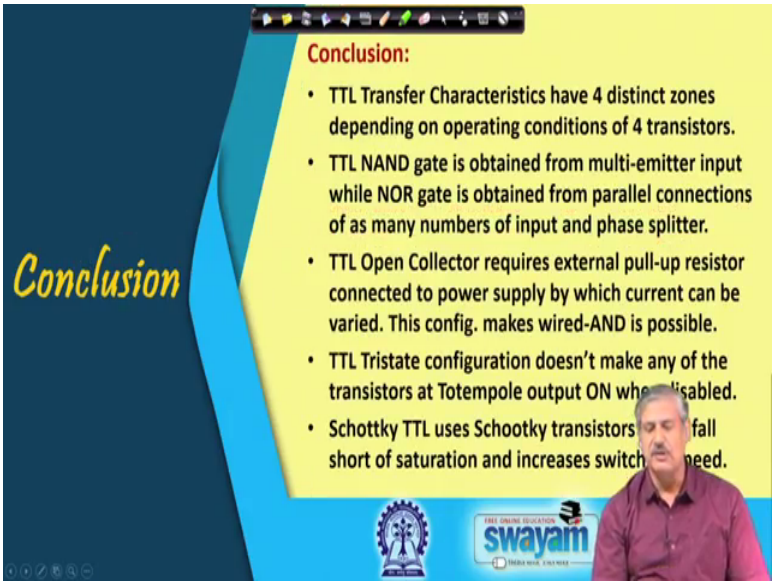

So, finally to conclude, so what you have seen today? TTL transfer characteristics - 4 distinct zones how it works and its different operating parameters. We have seen that TTL NAND gate is obtained from multi emitter input, while NOR gate is obtained by parallel of the input transistors and the phase splitters. Open collector configuration we have seen that it requires an external pull-up resistance, and it can be also used for wired-AND configuration. TTL Tristate, we have seen that when it is disabled, none of the output none output transistors in the totem pole configuration is on. And Schottky TTL, does not allow the transistor go into the situation. It just stops short of saturation which enhances the switching speed.

Thank you.