Digital Electronic Circuits
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Lecture – 35
Conversion of Flip – Flops and Flip – Flop Timing Parameters

Hello everybody. We have been discussing flip-flops. So, we have seen its truth table, characteristic equation, excitation table, and also representation through timing diagram in an analysis problem. So, in today's class, we shall discuss Conversion of Flip-Flops, and Flip-Flop Timing Parameters.

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In course of that, we shall also account ourselves with synthesis of sequential logic circuit. We shall gently introduce ourselves to that more complex sequential circuit design, we shall do later ok.

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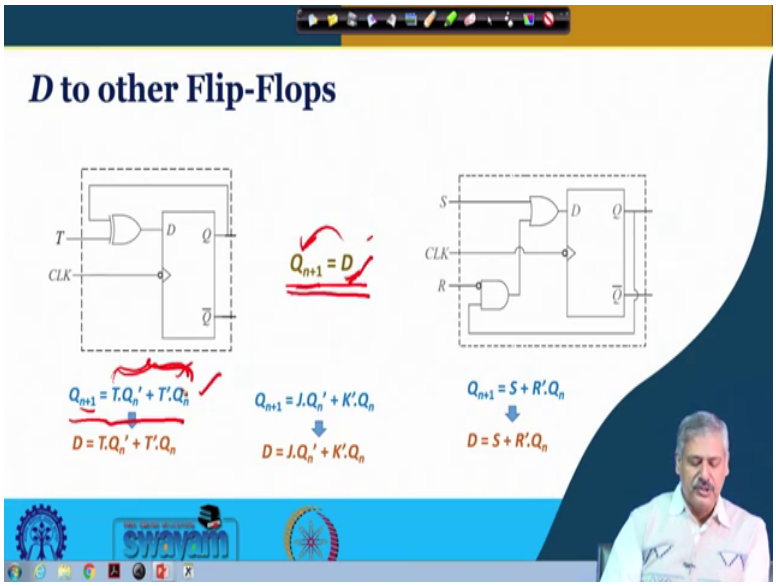

So, here when you are talking about conversion of flip-flops, so what actually we are looking at is a case a situation, where a circuit has been designed with a particular kind of flip-flop ok. And in your resource in your stock or library, you find that a different kind of flip-flop is available with you ok.

So, one option is to redesign the entire thing using the flip-flop that is available with you or thinking of a conversion mechanism by which the given flip-flop, the available flip-flop can be made to what like a different flip-flop ok. So, if we are looking at D flip-flop is available with you ok, and you are looking for a T flip-flop made out of it ok. So, one such circuit we have seen in the analysis class in the previous class, but let us look at a formalized method.

So, one way of doing it is that we know the characteristic equation of D flip-flop is Q n plus 1 is equal to D. So, whatever is presented at D input with the clock trigger, it goes to the output that we already are we are familiar ok. So, if we are talking about conversion of D flip-flop to T flip flop, so we know the T flip-flop equation characteristic equation to be Q n plus 1 is equal to T Q n prime or that is plus T prime Q Q n ok, this is already you we know.

So, if we look at this equation Q n plus 1 is equal to this, and Q n plus 1 is equal to D right. Then if this input T Q n prime plus T prime Q n, we feed as D ok. Then the D flip-

flop next clock instant, it will go here at Q I mean at the output of Q n plus 1 right. So, this Q n plus 1 will take the value of D. If D is defined as this one, is it clear ok.

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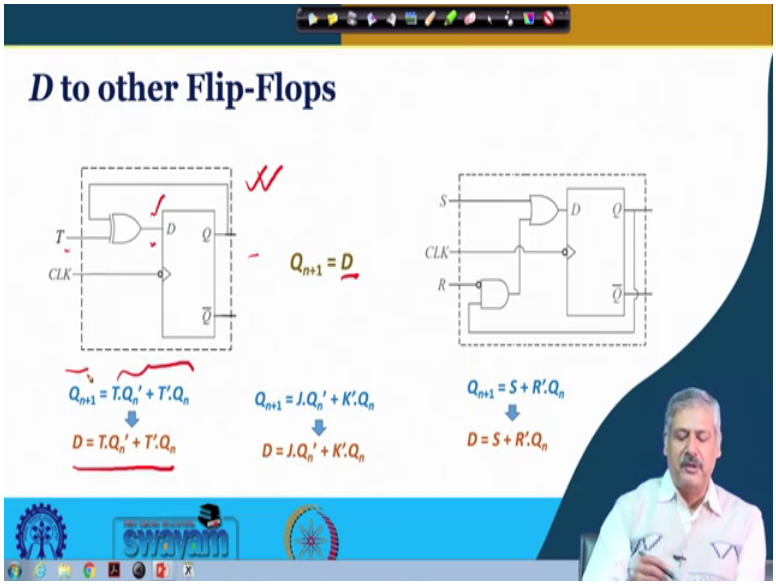

So, simply we can write D as T Q n prime plus T prime Q n ok. And that in the logic circuit this is a computer logic circuit right, so we can get by designing it. So, this is your T input, and this is just an XOR ring. So, basically Q and Q and getting XOR, and it is being available here as D input. And when the clock trigger comes, whatever is here it will go there ok. So, whatever is here that is this will go there. So, this is very simple for converting D flip-flop to T flip-flop ok.

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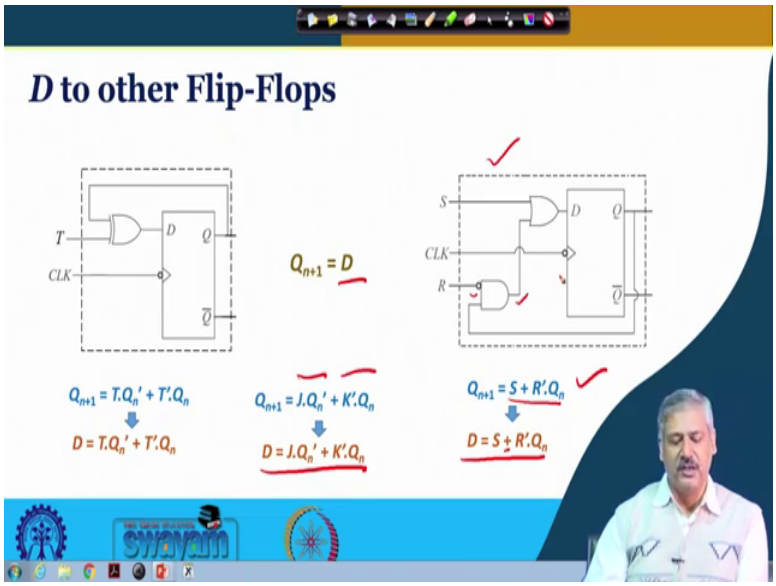

So, this can be extended to JK flip-flop as well. So, JK flip-flop equation is similar, but it is J Q n prime plus K (Refer Time: 04:13) prime Q n ok. So, we will take D as this one ok, and then we shall just make it combinatorial circuit, and accordingly we will get it right. And similarly, for D flip-flop getting converted to SR flip-flop ok. So, the equation is Q n plus 1 is S plus R prime Q n. So, we can write S as D as S plus plus is here or we know that, so R prime Q n ok.

So, the circuit will be here is goes here with it is getting (Refer Time: 04:52) R there is a inverter a NOT gate ok, and Q n is coming from here all right. And this is ended, and together it goes here right. So, this block this block entire thing can replace the SR flip-flop, wherever it is required in your design in your circuit its clear.

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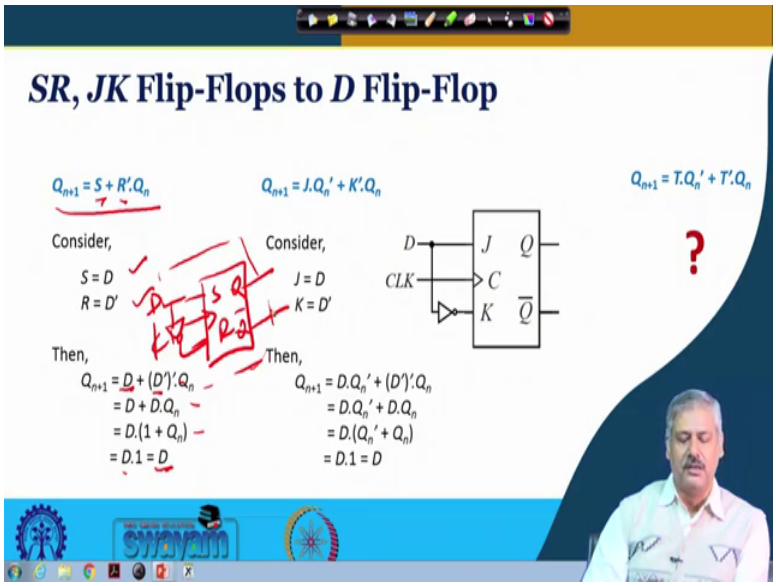

Now, if we are looking at converting other flip-flop to D flip-flop right. So, if we are looking at SR flip-flop getting converted to D, we have seen before. Otherwise, also we can figure it out from their equations the characteristic equation. This is Q n plus 1 is equal to S plus R prime Q n. And if we consider S as D, and R as D prime which we are done before, but we can put it in the characteristic equation.

And in this equation S is put as D, and R as D prime ok. Then we go through the steps, we can see that Q n plus 1 is becoming D, if that is what is done ok. So, this Q n plus 1 is D is basically your this D flip-flop equation. So, SR flip-flop all right S and R, this is your clock right. So, here you put a inverter and you connect, so this is D. So, this whole block this whole block this is Q, this is Q bar. This whole block will behave like a D flip-flop ok.

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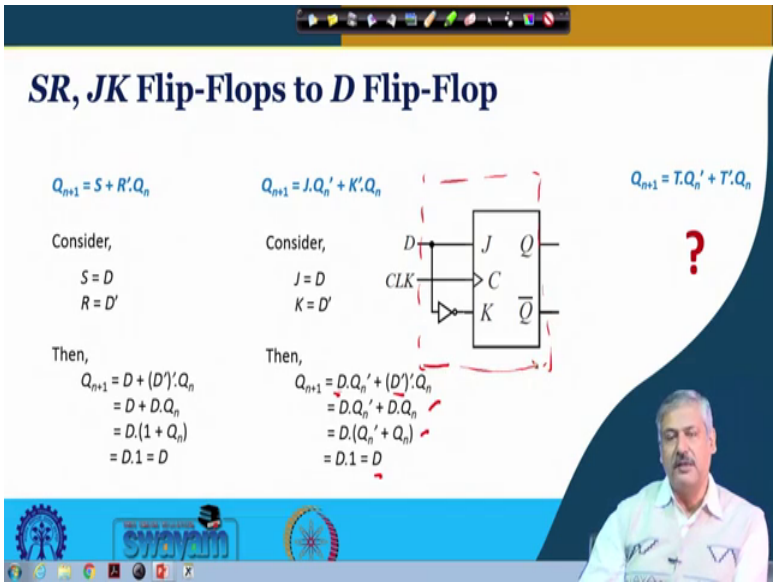

Now, same thing if you follow for you know J JK flip-flop, again you put a D and you know J as D, and K as D bar all right. So, you can see J as K D and K as D bar, and then you go through the simplification steps. So, you see that it is ultimately becoming D ended with Q n prime or Q n, which is D only. So, you can get the D flip-flop, just by connecting an inverter between J and K, and taking the J output as D output. So, the entire block over here behaves like a D flip-flop ok.

Now, if we are looking at converting T flip-flop to a D flip-flop ok. So, now if we look at the equation, whether we can put a inverter and all, and we can get it, we can see that the solution is not as trivial as it had been the case before. So, if we you know look very closely, and go through algebraic manipulation we can arrive at something ok.

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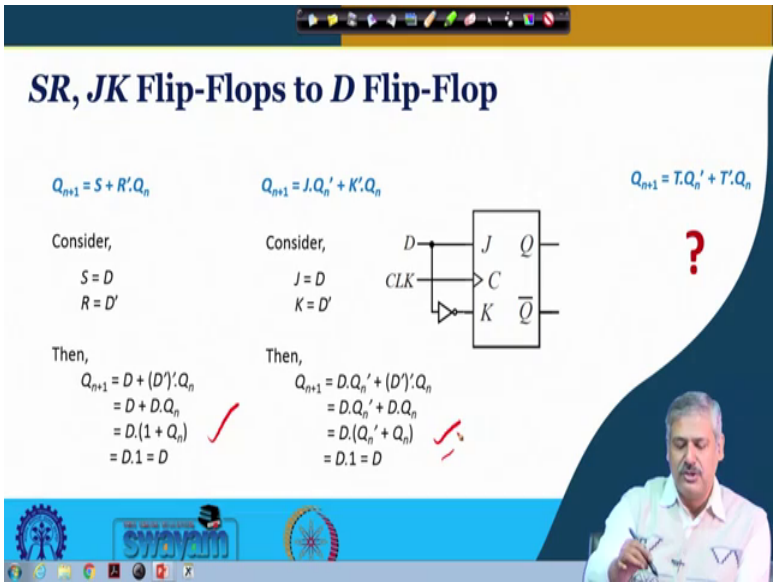

But, we can look at a method which is a generalized method, which we will work for every such conversion or every such synthesis kind of thing, which will work equally well for what we have shown here. Here we get got by comparing the equation, and by applying some knowledge about this Boolean algebra ok. So, otherwise also we can follow a standard synthesis method by which we can arrive at this solution.

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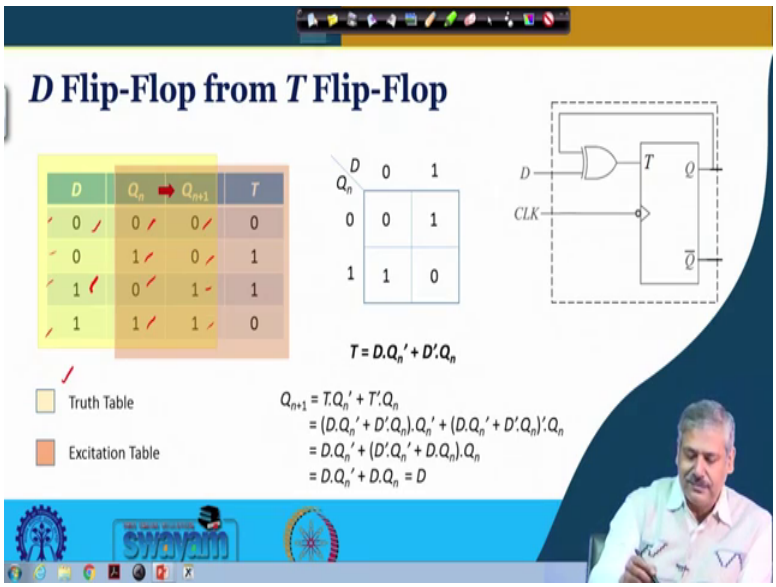

So, let us look at this problem of getting a D flip-flop out of T through a synthesis example, you know synthesis of logic circuit example not going through a algebraic

manipulation process ok. So, to do that, so let us see how we can go ahead. So, here what we are doing you see we have a table here right, which has got four columns. And here we have got of course these five rows, where data is four rows, where data is put ok.

And so the first part of it you see the one in this color all right yellowish color, you see that it is D flip-flop truth table ok. The flip-flop that we want truth table of that would be written, so that is this generalized you know method we are talking about. So, it will apply for a any other case, we shall take we can look at another example of course in the next slide. So, here we are talking about D flip-flop, so D flip-flop truth table is here. So, 0 all right if Q n is 0, the output will be 0; Q n is 1, output will be 0 that is the with D flip-flop works. So, if D is 1 both for Q n is equal to 0 and 1, output will be 1 this is right.

Now, we look at the T flip-flop right. So, this is the D flip-flop that is the way to work. So, at the time at the T flip-flop input, because inside there is a T flip-flop as a whole the block T flip-flop plus some additional circuitry, it behaves like a D flip-flop. So, inside whatever T flip-flop we have put, what should be the input in these cases four cases that we have seen in the D flip-flop truth table ok, so that we figure out.

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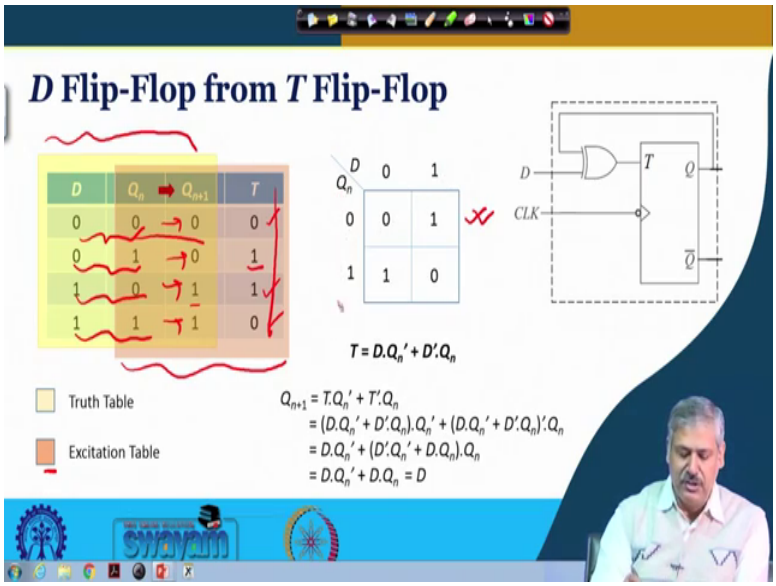

So, we see that in the first case when D is equal to 0, and Q n is equal to 0 ok, then the transition takes place from 0 to 0 ok, Q n plus 1 become 0 for this combination right So,

for this particular transition 0 to 0 right, what should be the input at T flip-flop. So, we look at T flip-flop excitation table, so that says it should be 0.

When this is 0, 1 this combination, and next value is 0, it toggles ok. So, for T flip-flop the input should be 1. For this combination 1 and 0, next value is 1, so that is again 0 to 1 T flip-flop toggles, that is input should be 1. And the fourth combination, when 1 and 1, then the transition takes place here is 1. So, 1 to 1 T flip-flop should be 0, is it fine. So, this side we are getting from excitation table putting this color, and this side we are getting from truth table right. So, we have put them in one common table ok.

So, now we understand that for this combination D and Q n that is external input and current state, what should be the T flip-flop current input ok. So, to get equation out of this to get a equation out of this what we can put, we can get a get it through a Karnaugh map I mean simply, so D is over here that is 0 and 1, and Q n is 0 and 1.

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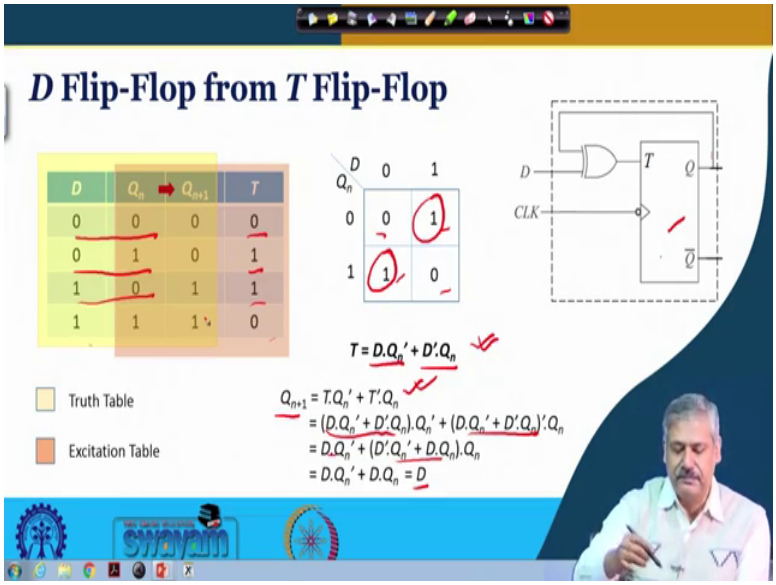

Now, we look at the cases, so 0, 0 T is 0, 0 1 ok. T is 1, this is the 1, 1 0, this is 1. So, this is 1, and 1 1, this is 0 right. Now, what we find that this can be gained obtained only by through two such you know products terms, so D Q n prime plus D bar Q n ok, this is what it becomes so T becomes actually D XOR Q n D XOR Q n right.

So, you could have obtained it by as I said the you know through an algebraic manipulation and all. And knowing how XOR function works, XOR of you know XOR

of same function with the same XOR of one function with the same function is giving you 0 right. And 0 with another variable will be the variable itself ok, one with 1 XOR with the variable is complement of the variable, and 0 XOR with the variable is the variable itself.

So, essentially what we are getting here is XOR of XOR, and then the variable ok, so that if you are knowledgeable about the XOR operations and all. Otherwise, as I said generally speaking, we can get it for sure by a standard method like this ok. And we can verify, so Q n plus 1 over here, we have got in this manner. We know the basic equation of Q n plus 1 sorry that is T Q n prime plus T prime Q n for this particular flip-flop right.

And then we substitute T as what we have got Q n and D XOR right, so that is this relationship and over here ok. Then we do go through you know steps right, then we can see that it is nothing but D ok. So, Q n plus 1 eventually becomes D right. So, this is the way we can see that it is the T flip-flop, and this is D flip-flop. So, this is a simple you know synthesis problem this steps we know that truth table, and then this is what is required for the input to be all those cases, and that is obtained through um excitation table ok.

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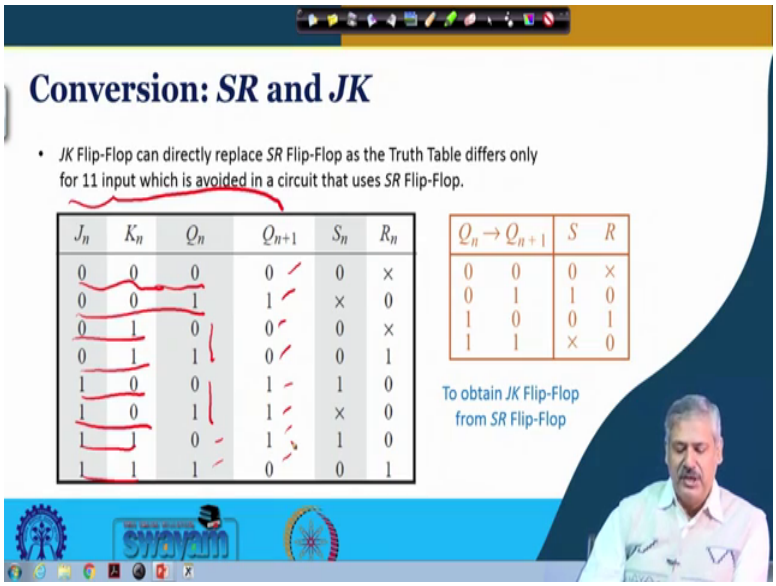

J_n	K_n	Q_n	Q_{n+1}	S_n	R_n
0	0	0	0	0	×
0	0	1	1	×	0
0	1	0	0	0	×
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	×	0
1	1	0	1	1	0
1	1	1	0	0	1

$Q_n \rightarrow Q_{n+1}$		S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Now, let us look at another example ok, where we have JK flip-flop required from SR flip-flop ok. So, given a SR flip-flop two you know two input and we require a JK flip-flop. We can do it for any other type that is one type to another, so let us look at this one

right. So, in this case what we have over here. In the first place as we have mentioned so, JK flip-flop truth table is it ok. So, the one that we want to be made that truth table will be put that is there in the left hand side right. So, 0, 0 and if this is the case input is 0, 0, 0, 0, 0 and Q n is 0 right. Then next value will be 0 only, and input is 0, 0. And this is one next value is 1, because 0, 0 the previous value is written ok.

So, 0, 1 irrespective of what is Q n, this is 0, 0. 1, 0 irrespective of Q n, this is 1, 1. And when it is 1, 1, it toggles ok. So, 0 becomes 1, 1 becomes 0. So, this we are already familiar. Now, each in each of these cases now, for the SR flip flip-flop that is been used for the design at its input, what should be present that we figure it out ok.

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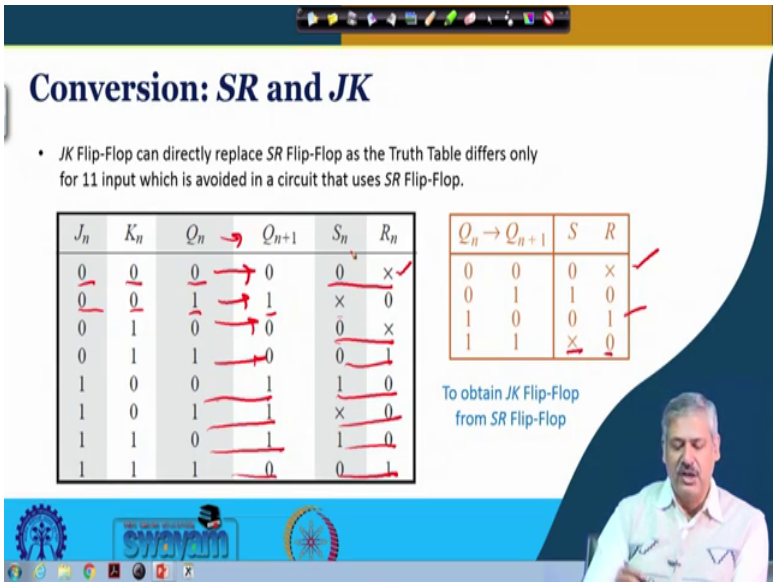

So, here we see a 0 to 0 transition ok. If J n is 0, K n is 0, Q n is 0 at that time ok, what should be present at S and R. Since it is a 0 to 0 transition from SR flip-flop excitation table, we can write it should be 0 cross that means either 0, 0 or 0, 1 any one of them is ok. So, this is what should be present clear. So, if it is 0, 0, instead of 0, if it was 1 ok, then what would been the case the transition, it would have move to 1. So, what should have been present at SR flip-flop input at that time, it should have been X and 0 that is from the SR flip-flop excitation table right.

So, for this combination 0 1 0 JK Q n, then at that time 0 to 0 transition, again 0 X 0 cross ok, 1 to 0, we need 1 to 0 is 0, 1 right 0, 1. So, again 0 to 1 ok, so this is 1, 0 1 to 1

cross 0; 0 to 1, 1, 0. And 1 to 0, 0 1 is it fine. So, this for these particular transition we require this ok.

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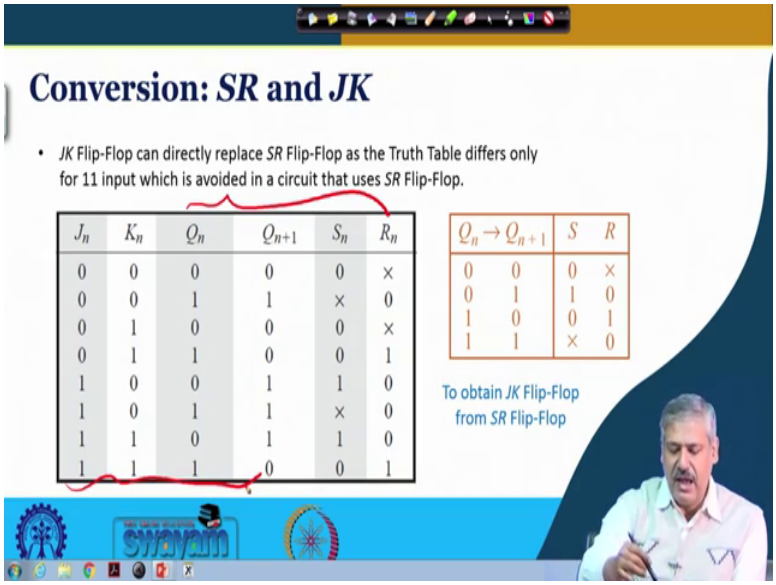

So, we can now understand that this part is the SR flip-flop excitation table, which is deciding the entries right. And these part JK flip-flop truth table are deciding the entries. So, this is this JK flip-flop truth table itself is it ok. Now, with this table in hand ok, we now move to next step.

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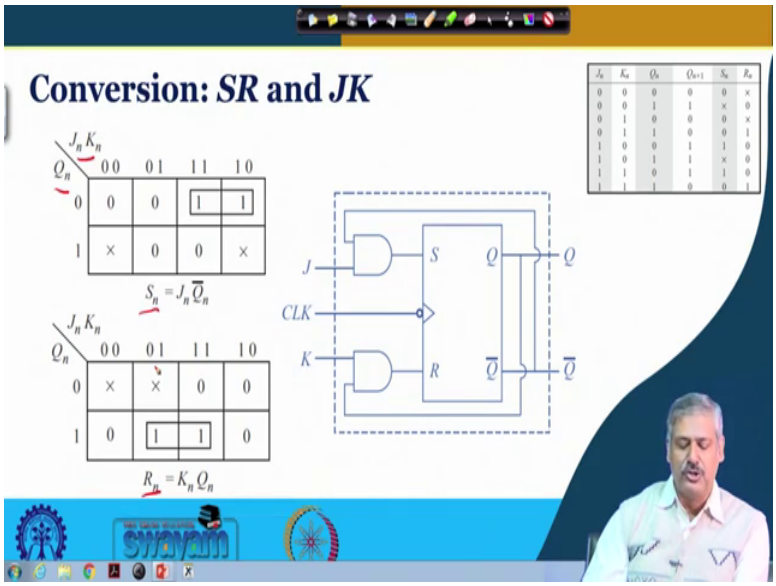

So, next step would be that representing each of these input each of these input S n and R n at a given time in as a function of J n K n and Q n ok. So, the current state current inputs that is coming from external externally, because we are trying to convert it to a JK flip-flop ok, so that is what we are having as current input. And at that time what should be presented at SR flip-flop input, so that we required change in the output Q n required Q n plus 1 value appears at the output is it fine.

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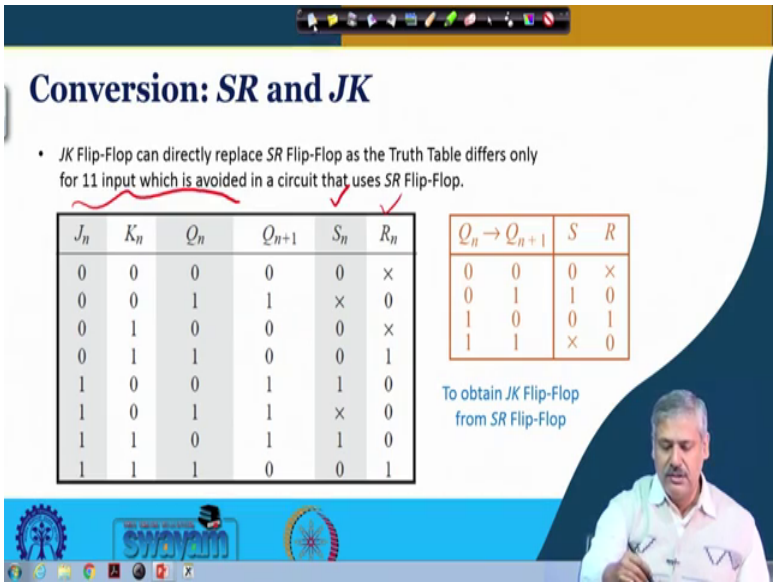

J_n	K_n	Q_n	Q_{n+1}	S_n	R_n
0	0	0	0	0	×
0	0	1	1	×	0
0	1	0	0	0	×
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	×	0
1	1	0	1	1	0
1	1	1	0	0	1

$Q_n \rightarrow Q_{n+1}$		S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

So, from that truth table the truth table, that we had just seen do a mapping from this part J n K n Q n ok and S n and then J n K n Q n as R n. So, two such Karnaugh map will be there two such relationship will be available ok. So, in one case this is what we get right 0 0 1 1 cross 0 0 X right, this we can see from so 0 0 0, you can see for J n K n Q n, it is 0 S n.

So, you can see it is S n right. Here 0 0 Q n is 1 this is X ok. So, you can see this is X 0 0 1, this is X. Next is next is 0 and 0 right, you can see 0 0. Next is 1 1 you can see ok, so this is the way 1 X right, and then 1 0. So, 1 X, and this is 1 0, because this is 1 0, and this is 1 1 that is the way Karnaugh map is written right, so 0 X 0 0 1 X 1 0.

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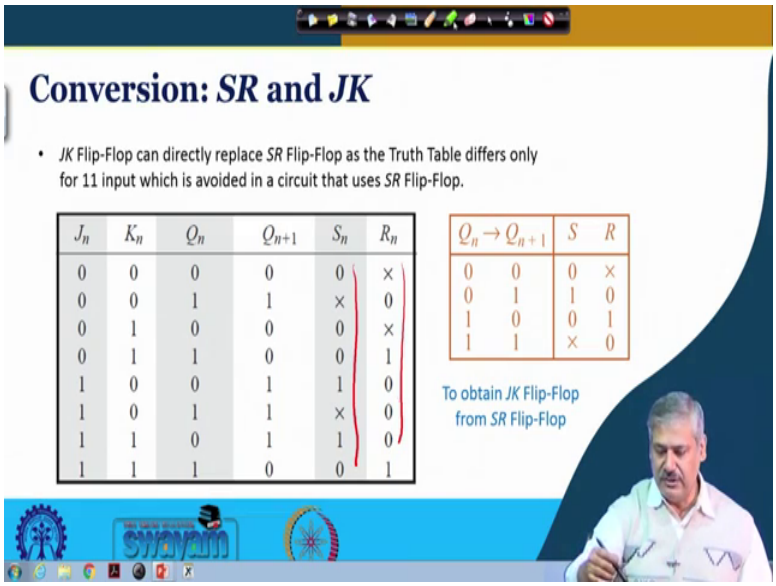

So, this is what you can see this is what you can see over here 0 X 0 0 1 X 1 0 ok. So, similarly for the R n value, you can see the mapping is presented X 0 X 1 0 1 0 0 ok.

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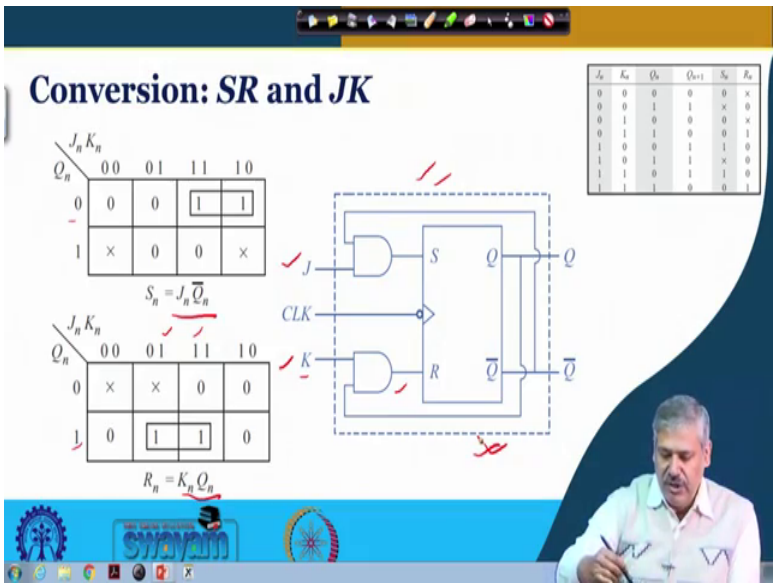

So, now to have a minimized expression for this right; so, we can see that one group is required here, so that is coming as J n remaining constant with value 1, and Q n with value 0, so J n Q n bar. So, as an we can simply write it this way, because we need to cover only the once that is the largest group possible. And for R n, we can see that it is K n remaining value with 1 and Q n with value 1, so it is K n Q n ok.

So, now we can get the circuit as we have we see over here. So, this is your basic SR flip-flop, this is your Q and Q bar right which is generated internally in the SR SR flip-flop. So, J and K are the external input ok. So, in one case J is ended with Q n bar right the connection is taken, and fed as S. And in the other case K is ended with Q n, and fed as R ok. And this whole box which you see with the dotted box is your is final circuit final converted circuit fine.

So, any flip-flop that you require which is from the characteristic equation or truth table, you can you know directly cannot convert ok, you can go through this synthesis process, first you write the truth table. And then for the changes that is happening at Q n and Q n plus 1 for a specific input, you write the input that is required for the flip-flop being used from the store or library. And then you use the excitation table through Karnaugh map or any other minimization process you get the combinatorial circuit may, and then finally you implement it right fine.

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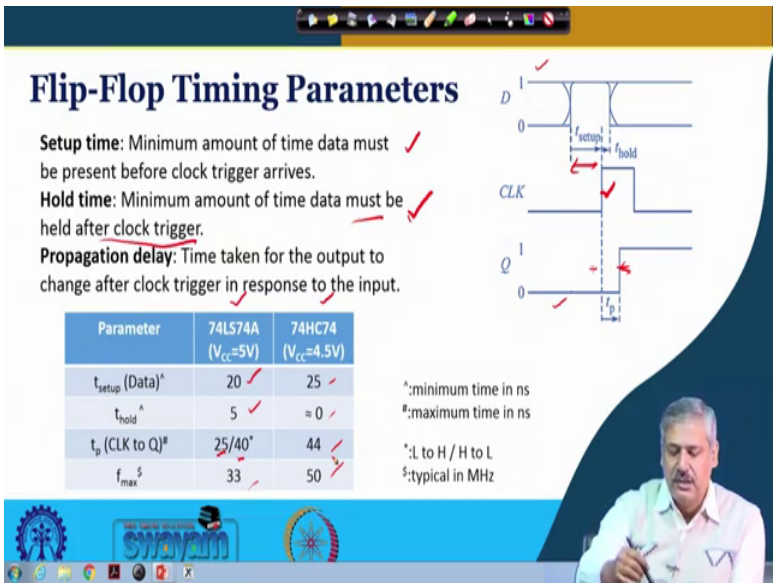

To end this particular lecture, we just would like to get you know introduced to another important concept is that of flip-flop timing parameters its significance ok. So, as I said the timing diagram is the key to exhibit how the things happen workout with respect to time, which is not very clear from the truth table, excitation table or other form of you know representation. So, we take help of this timing diagram to discuss to understand the

importance of these timing parameters. So, there are quite of few, but we just take up three important once.

So, one is called setup time ok. So, this is minimum amount of time data must be present before the clock trigger arrives ok. So, the clock trigger comes, so if it is a say positive S trigger, you know kind of thing the it has arrived ok. So, whenever it reaches positive, it is you know susceptible to change. So, before that some minimum amount of time, data's must be held at a stable value. So, this is called setup time ok. If it does not then, the output cannot be guaranteed manufacturer cannot guaranty the output ok. So, this is one aspect.

And the other thing which comes in association with it is called the hold time ok. So, this minimum amount of time data must be held after clock trigger ok. So, clock trigger has happened, you are not supposed to immediately withdraw the data. So, it must be held for some time ok. The minimum time that is required you, if you hold it for more time there is no issue, but certain minimum time it should be held that is called hold time ok, so that is to ensure or guarantee appropriate output of the flip-flop appropriate you know state change in the flip-flop ok.

And the other thing that is there is called propagation delay right; so, time taken for the output to change after clock trigger in response to the input. So, basically it goes through different you know logic gates, and there could be various basic components like you know stray capacitances, resistances, so charging, discharging. So, all those issues are there, because the basic gates we have already learned.

So, if you put together all of them ok, so the amount of time that is required for the for example here D was one so D is after clock trigger becoming initially it was 0 becoming 1. So, the delay associated is called propagation delay ok. These three terms you take note of. And if you go through the data sheet, you will see many other such you know terms are there timing related which are important ok, but that may occur in certain instances of time not regularly as it is happening for the setup and hold time and propagation delay.

For example, if you present a asynchronous clear right or asynchronous preset, so after certain amount of time, only it will be reflected it will the output will get cleared or it will get preset. So, there is a delay associated with it, but your it is happening whenever

it is required not you know regularly. So, those delays, and those parameters, those terms are also available in the data sheet, if you look at it you can see that there ok.

So, to get an idea about what are the practical values some of the you know IC's or circuits that are used. So, we take the D flip-flop one from TTL family ok, another from CIMOS family. So, you see that in TTL family the setup time is these are all in nanosecond ok. So, minimum time 20 nanosecond, hold time is you know 55 nanoseconds. So, 7474 74 LS 74 A ok. So, if it is again L means low power, so higher resistance values ok. So, if it is only short key S for short key that we know we have seen it in the logic family.

So, then the resistance values will be standard one. So, for which you will see the time will be relatively less. So, these are you know just the order that you get it, but for different families with different realization, we will be having variation around it ok. And this propagation delay, so low to high 25 nanosecond ok. And this is 40 nanosecond is high to low ok; this is the maximum delay that can happen.

And typical frequency of operation because of these delays and all; so that is 33 megahertz ok. And in these case this CIMOS thing, so you can see the setup time is like this hold time is approximately 0. In some literature, you will find it is written 0.5 nanosecond. So, this is the propagation delay, it has not been separated in the data sheet low to high, high to low and it max has been mentioned as 50 megahertz ok.

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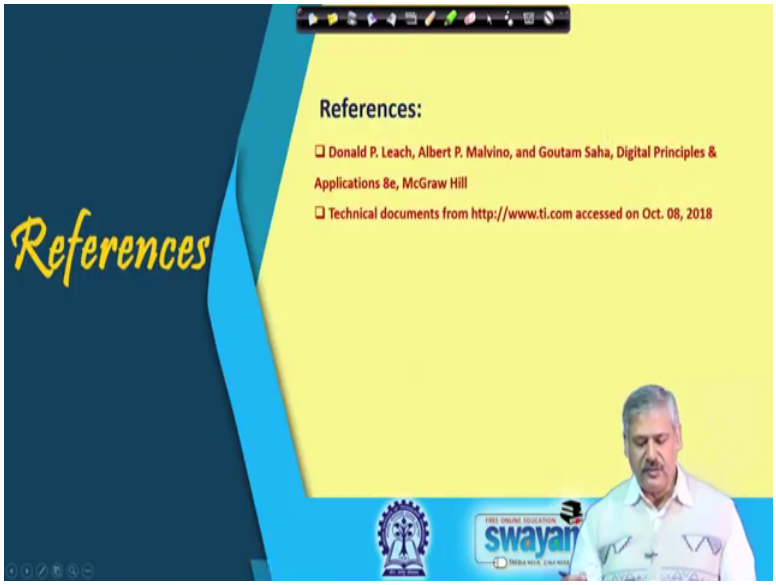

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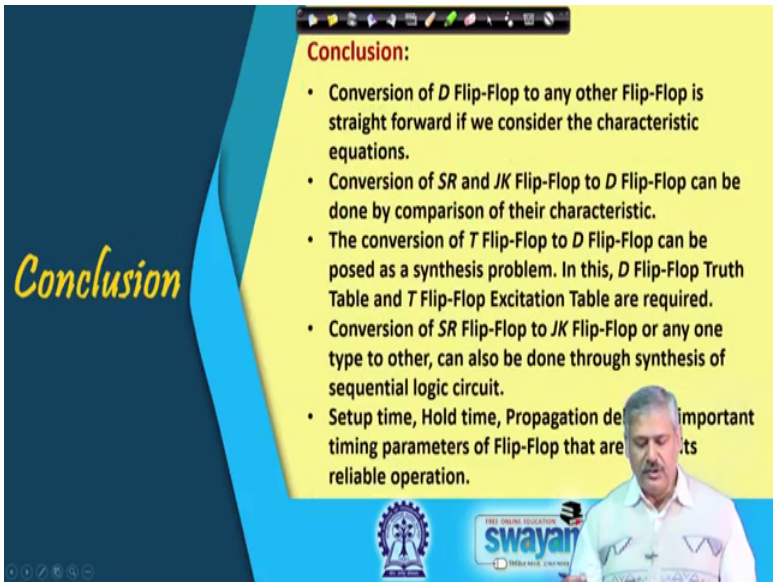

So, to summarize, conversion of D flip-flop to any other flip-flop is straight forward, if we consider the characteristic equation. Conversion of SR and JK flip-flop to D flip-flop can be done by comparison of their characteristics. The conversion of T flip-flop to D flip-flop can be posed as a synthesis problem. In this, D flip-flop truth table, and T flip-flop excitation table are required. And similarly, SR flip-flop can be converted to JK flip-flop again though a synthesis problem ok. And setup time, hold time, propagation delay are important timing parameters a for their reliable operation we need to take note of them, and use the flip-flop triggering accordingly.

Thank you.