Digital Electronic Circuits
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Lecture - 34
Analysis of Sequential Logic Circuit

Hello everybody. In this class we shall discuss how to Analyse a Sequential Logic Circuit ok. So, this is the first discussion on this, so we shall introduce the topic softly. So, we shall not take a very complex circuit. In future classes we shall have discussion on more complex circuit. So, we have seen various representation of flip-flop in the previous class.

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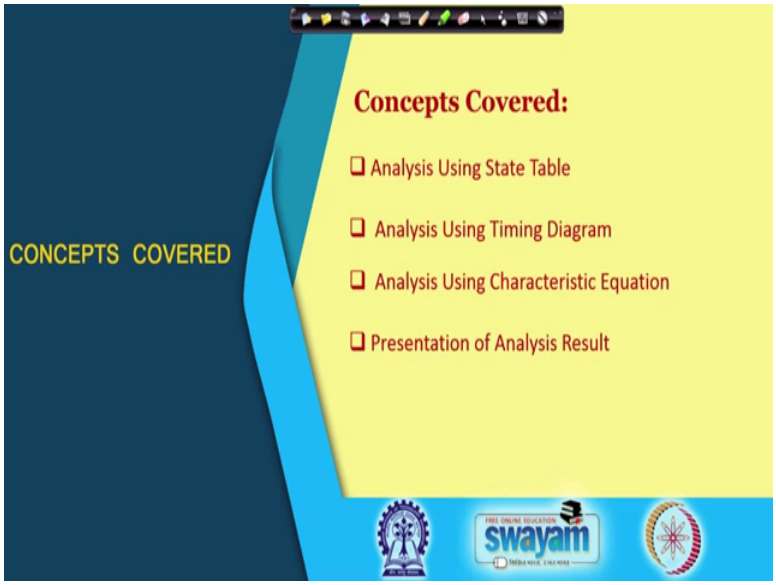

And we shall make use of some of those representation in the analysis ok.

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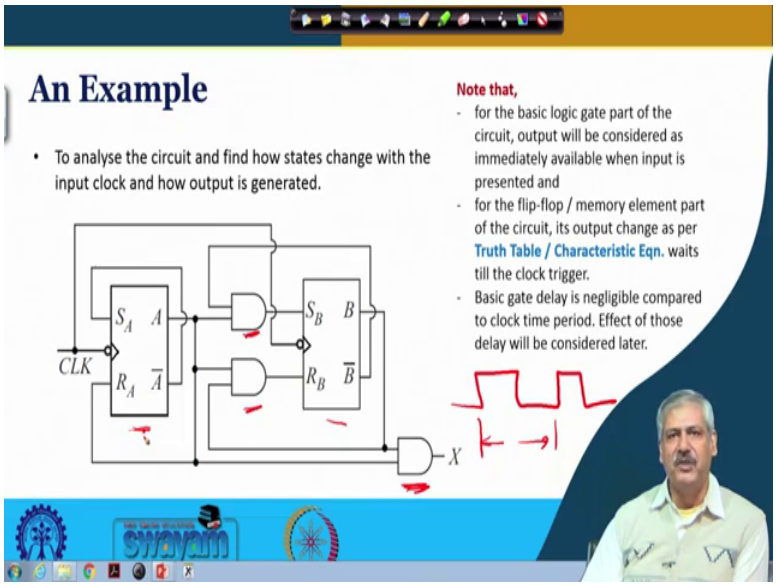

So, we start with an example and through solving this for example we shall learn the associated technique ok. So, the example that we have taken up you can see is a SR flip-flop best example, right. So, this is a SR flip-flop, this is another SR flip-flop, so you have named it as A and B ok. So, input has been designated as S A R A instead of Q and Q bar we are writing A and A bar ok. So, that we understand that this is associated with flip-flop A and similarly for flip-flop B.

And what you see the circuit has got other logic gates. This is what you are expected to see in a sequential logic circuit. It will be having combinatorial circuit element. So, called combinatorial circuit elements that is basic gates, right which does not have memory. And we shall also have these memory elements in the form of flip-flops ok. And later we shall see combination of flip-flops by which you know the resistors will be part of the sequential logic circuit and other things ok. So, other building blocks we shall discuss later.

So, there is some connection, right. So, you have to go through the analysis steps and figure out what the circuit as a whole does. And in doing it since it is analysis we shall make use of what we will see later that truth table and characteristic equation. We have not looking excitation table or state transition diagram in its analysis. So, that will be useful in synthesis part which we shall take up later ok.

Further, here we see that of course, this is a clock flip-flop, right. So, we considered the clock cycle time; clock cycle time this is the way the clock cycle is triggering, all right. So, this clock cycle time is much much more than the propagation delay of this basic gates ok. This propagation delays or of the order of nanosecond 10 nanosecond or so, ok. And in this flip-flop of course these are this frequencies could be in kilohertz Hertz or megahertz, even in all those cases this is not this delay is not comparable to whatever is the timing period.

So, if the delay is comparable what will happen that again we shall take up later. Right now in our first discussion on analysis of sequential logic circuit we are considering a scenario where this propagation delay of basic gates is substantially small. And similarly the circuit inside the basic gates the comprises of that goes into the making of this flip-flops. So, delay associated with them and delay of the flip-flop is also small ok. So, that is what we consider.

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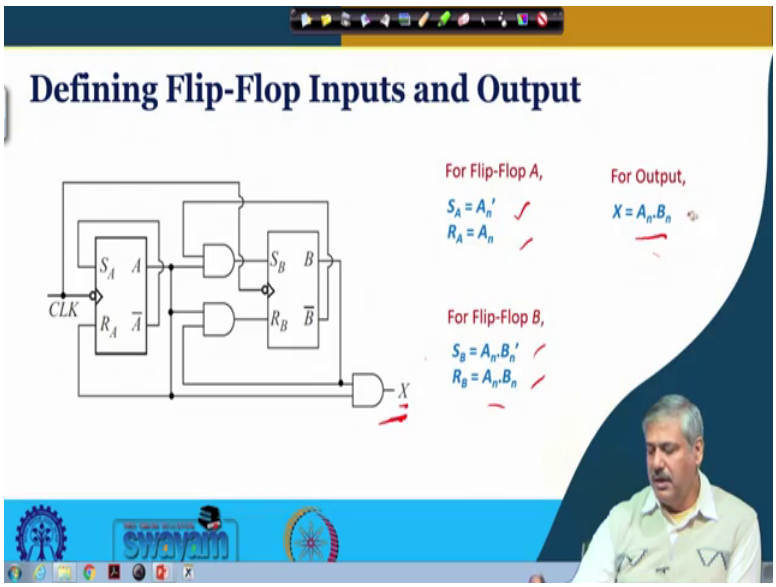

So, first we look at representation of different inputs of the flip-flop in terms of the current state value, right. And in this particular circuit there is no external inputs. So, if there was external input we would have represented in the form of using that external inputs also. So, we shall take up example where there is external input in sometime later. And also we shall do it for the output, this final output that is getting generated here, right.

So, we see what is happening for S A input. So, if you look at S A input, right this is nothing but whatever you see here A, right. So, that A the current state value is fed back, and presented as S A. Is it fine? You can figure it out. So, that is the analysis part, right you have to look at the circuit diagram and from that you can figured it out. So, S A is A n bar, right.

What about R A? So, this is what we have to see all the inputs we have to see the you know logical connection; logical relation. So, R A you can see this coming from over here. So, this is the path it is talking, right. So, R A is A n; this is fine. Now you have to look at S b. So, this is S B; what we see it is coming from a AND gate, right. So, this AND gate is one input is A and the other input is B bar, so, that is A n and B n bar. So, that is S B. And what is R B? R B is R B you can see is that fine. So, this A n this is one is there another is this is coming about here that is B n, right; so A n and B n, right.

And also you can see the final output X is B n and A n, right. So, final output could have take would have been taken from here also if it is so possible ok. Otherwise it is if it is, so drive something else and also it depends, right. But logical relation of both of them is same for this particular example for some other example it could be different, if we depending on the requirement; it could be A n B n bar or A n bar B n bar some such thing or whatever. is it clear?

Now we have understood what is S A R A, S B R B and X ok, how they are logically connected. So, that is the first step what we do in the analysis.

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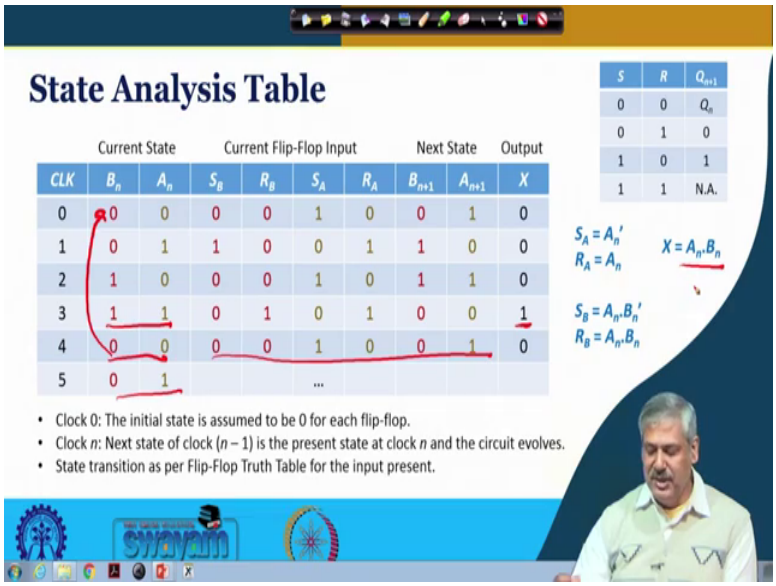

So, next we come to something which looks formidable now to begin with, but once we go through the process we will see that it is not that difficult to understand what is happening here. So, it is called state analysis table or state table. So, in this we begin with an initial state ok. We are analysing the circuit, so initial state if not otherwise mentioned; if not otherwise mentioned so you can assume it to be 0 0. That means, the current value of the flip-flop is 0 and 0; is it ok.

Otherwise it will be mentioned that it is initialized with this, clear. And how we can make sure that this is 0 0? So, the flip-flop usually will be having a synchronous clear or their input, in some of the flip-flops present input may also be there, but here is available ok. Otherwise also you can drive to the; I mean if it is so possible, by synchronous clear or present also you can come to a particular initial stage.

So, it is fairly acceptable reasonable to assume that the initial state is 0 0 if it is not otherwise mentioned ok. So, that is what we mean by clock 0. And then with clocking these circuit will move from one state to another and the corresponding output will get generated and that is what we have to investigated, is it ok. So, this is the current state this is S B R B the inputs, S A R A the inputs, this is the these are the next state, and this is the output. So, this is how the state table has been configured which is understandable, right.

So, if the current state is 0 0 and we have already seen the equation for S B R B and S A R A ok. So, what is the current input? So, if it is 0 0, both of them are 0 0 for S B you can see a A n is 0, right, so this is 0 because this is n logic and here also n is there so both of them are 0. So, if both of them are 0 for flip-flop B what will be the; so this is flip-flop B; what will be the next state, ok. So, 0 0 means previous value will be written, so B n is 0, is it clear.

So, that is what you will see. And when the your, if you look at S A and R A, it is in Hertz of A n, A n bar. So, A n is 0, so S A becomes 1, and R A becomes A n itself. So, it is 0. So, 1 0, so it will get set. So, this is 0 1; is it clear or not. The first row; only the first row ok.

So, then first clock trigger comes; so, basically B n plus 1 is clock trigger has happened, ok. So, the value will becomes 0 and 1, the flip-flop will move from 0 0 to 0 1. So, when it moves from 0 0 to 0 1, right. So at the next clock cycle inputs will get changed accordingly, because the inputs to all these things and even the output is a function of A n B n and had there been an external input. So, the is a function of that ok. So, here we are considering only these states, right.

So, for that we have to come to the second row of the state table. So, after first clock cycle first clock trigger has happened. So, we have to come to 0 1 and that 0 1 becomes the current state, through which the analysis process will continue with which the analysis process will continue.

So, if it is 0 1ok. Now again we shall look at we shall look at what is happening to this S B R B for B n and A n being 0 1 S S B is A n B n bar; right A n is now 1 and B n is 0. So, B n bar is 1, so 1 and 1 ended is 1. And what about R B? R B is A n B n. so, B n is 0, so 1 and 0. So, this is giving you 1 and this is you 0 ok. So, this is 0.

So, 1 0 means then B n plus 1 will become 1, this part is clear. What about A n sorry; what about S A R A now we look at S A R A this part we have seen, ok. So, S A R A is A n bar and A n; A n is now 1 ok. So, S A becomes n bar is 0 sorry; S A becomes 0, right because this is 1 and this is 1, right, because it is an. So, 0 1 means it will become 0. So, next state the clock trigger comes, becomes 1 0 after second clock trigger. So, this 1 0 becomes the current state ok.

And this 1 0 then again if you look at S B R B, this is an is 1 and B n is 0. So, you will see that an is 0 making it 0 and B n here also n is 0, so it is 0 0 ok. So, 0 0 means previous value will be written. So, this is at 1 ok. And what is happening to S A R A? Because is it was 0 it becomes n was 0, so S S A becomes 1 because it is invert and this is 0. So, 1 0 means it becomes 1. So, current state becomes an X state becomes 1 1.

And with 1 1 at the input ok; so, we will see again if you follow this equation 1 1 as at the input A n is 1 and B n is 1. So, B n is 1 means this is 0. So, 1 ended with 0, so this is 0 and this is 1 ended with 1 this is 1 ok. So, this is 0 1 ok. So, that makes it 0 A n plus 1. And your S B R B ; so that S A R A. So, S A R A is your this just inverse of it. So, A n is S A is 0 and this is 1, so that makes it 0 ok.

So, that is net state becomes 0 0. So, when it is 0 0 you come over here you see this is the first row. So, same thing will come over here and it will keep repeating. And in each case if you look at the output is A n B n. So, whenever the current value is 1 1 the output will be 1 1 at that time ok. For the rest of the cases it is 0; is it fine ok.

So, this is the way the state table will evolve.

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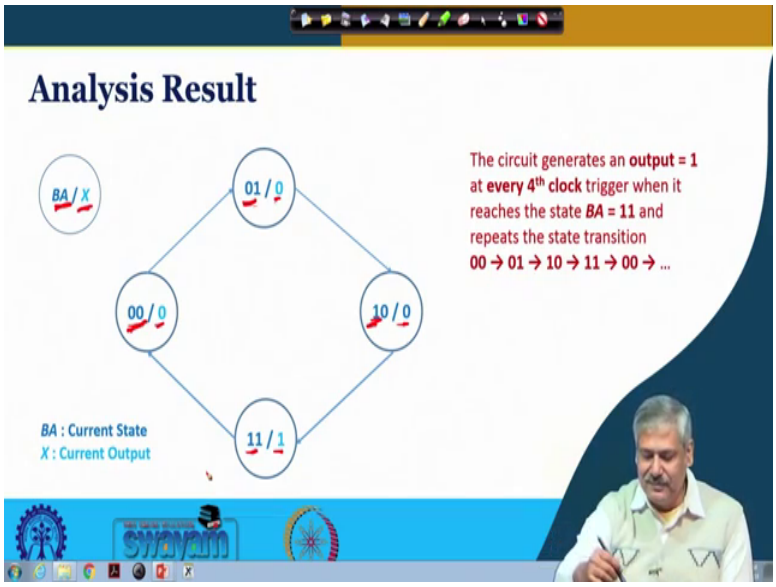

So, how will you represent the analysis result? So, you can represent through pictorially, through state transition diagram. So, in the state transition diagram what you are we are showing here is that a this is the current state and this is the output that is generated ok.

So, 0 0 is the current state, and output generated at that time is 0; that we have seen in the table, right. So, next state is 0 1. That means, the when the clock trigger comes, right and this is 0; 1 0 after that then 0 0 and this 1 1 and at that time output is 1. Next clock again it goes back to 0 0. And it keeps cycling around this 4 states, ok.

So, this is one way we can visualize what is happening in that circuit after analysis, the other one is a text description where we say the circuit generates an output 1 at every 4th clock cycle that is what you have you can see when the where it reaches the state B A is equal to 1 1 because that is the way these flip-flops where designated, and repeats these state transition 0 0 0 1 1 0 1 1, ok. So, that is the way it continuous.

So, analysis for analysis a circuit is given you analyse and you come to a state transition diagram for a pictorial description of it or it takes description to English you know statement to clearly explain what that circuit does, ok. That is there analysis result.

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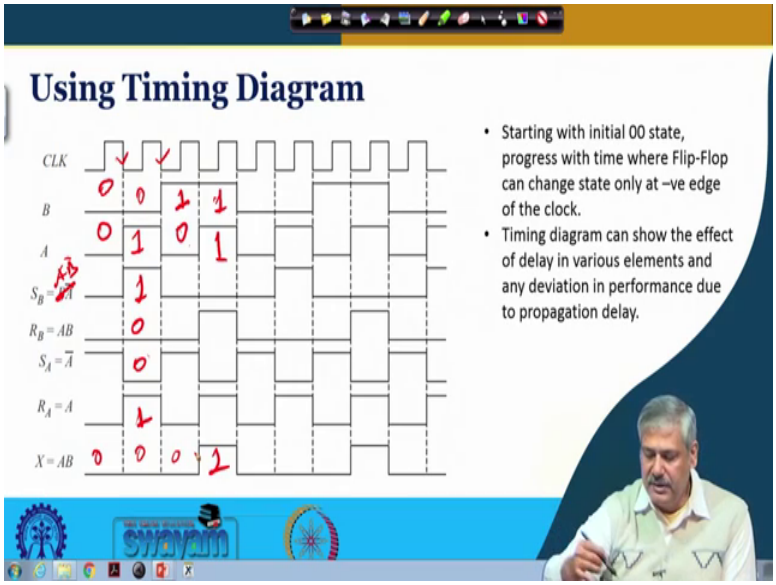

Now, in the representation of the flip-flop we said that timing diagram is very useful, but we did not take up. Now here we can see the how timing diagram comes into play.

So, for which we consider that this is the clock and it is getting triggered at negative edge of the clock, ok. So, whenever a negative edge comes the circuit can trigger, ok; I means the flip-flops can trigger, right. So, we start with initial state B and A 0 0; that is what we have considered, right. So, in B and A are 0 0 up to this time point what about the values

of S B and R B or S B was B A A prime B, so this is 0, this was A B so this is 0, right. And S A and is A bar. So, this was 1 at that time and R A is 0. Is it fine?

So, this is what we can see from the previous circuit if we sorry; here it is A n B n prime, this is S B is A B prime, ok. So, there is a mistake we have to yes look at it.

So, then what happens at this point when the clock trigger comes, when the clock trigger comes at this point, ok. So, depending on the values that are presented, so this is 0 and 0, right. So, the previous value was 0 for B, right, so S B R B is 0 0; S B R B is 0 0. So, it will continue to become 0 0. So, it gets the trigger over here, before that it is not supposed to change. That we discussed before when clock circuit is triggered circuit or gated circuit or so, ok. So, even if the input you know changes unless the clock trigger comes it is not going to change.

So, this continuous to 0 0 0, ok. How long it will continue till then edge clock edge comes, at that time it is you know it can make a change if depending on the excitation, all right. And what happens to A? A is 1 and 0. So, when the clock trigger comes A becomes from 0 it goes to one.

Now, here what I was telling that we can show the delay if it is appreciable which other representations cannot show. If the delay over here flip-flop delay is comparable to the compatible to this you know this clock period sorry; from here to here this is one clock period, from here to here this is one clock period, then we can show the delay, right here a is changing we can show it like this, that when proportionate delay. That it has become one, but after sometime and if the delay is cumulative or this delay is something by which it the circuit can man function or can give some undesirable result, that is better manifested through timing diagram with representation, but not by others, ok. This is the usefulness of timing diagram based representation. And we shall see such cases in future when you study other sequential logic circuit, clear.

So, coming back; so 0 B continues with 0 0 and A becomes 0 to 1; is it fine? And it will remain 0 to like this till the next clock edge comes, till the next clock edge comes negative is triggered, ok. So, when it is at 0 and 1 what happens to the inputs now, ok. So, again this is A B bar, ok, right. So, this becomes S B becomes A B bar. So, this becomes 1 ok, R B is A B so this is 0; S A is A bar, so this is this is a is 1 so this becomes 0 and R A is 0 R A is ah R A is 1 because it is a A is 1 now. Is it fine?

So, it is moving with the clock, right synchronous clock and it becomes 1 after that that causes the changes in S B R B S A and R A. So, small propagation delay will be there, right. But again this is negligible compared to the clock period, negligible compared to the clock period, because this logic operations as I said if it is appreciable then we can show that S B is becoming; after this has changed, like this then from that it will further small delay and it will be shown in that manner, ok. Otherwise we are neglecting that part, ok. So, 0 1, so this is 1, this is 0, this is 0 and 1.

Now, clock trigger negative edge comes. So, at that time again circuit can change. Again let me correct every time, ok. So, this is, ok. So, then what happens 1 0; sorry S B is 1 0. So, B becomes 1, right and S A is 1 0 all right. So, S A is sorry 0 1 S A R A. So, it becomes 0. So, from 0 0 it goes to 0 1 then 1 0 and then you can see that it is goes to 1 1 and then again its repeats at 0 0, ok

So, this is the way the timing diagram can be used to show how the circuit moves; I mean that is this through the analysis process. And each time you can show the output over here and based on the current input, and when both the inputs are 1 1, right you can show the output is coming 1 1 just after a small propagation delay if propagation delay is compatible. Fine, right.

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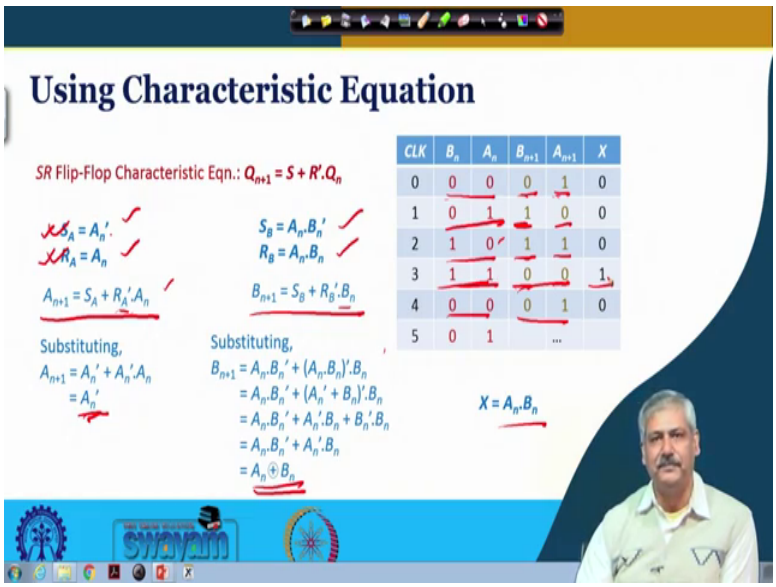

So, we can use characteristic equation also directly, since we already are familiar with characteristic equation, right to come up with the analysis result, ok. So, we have seen

that S A and R A how it gets represented. And we know the flip-flop equation of SR flip-flop. So, A n plus 1 we can write it in this manner S A plus R A prime A n, right. And when we substitute S A from here and R A from there and we just you know simplify we see that A n plus is A n bar A n prime, ok. And that we have actually seen in the previous cases, then the timing diagram also that it is just toggling output is a flip-flop is simply toggling in a every clock cycle, and that we can see from the equation also.

Similarly S B and R B we have seen, right. And we have got flip-flop equation. Now instead of Q n plus 1 1 we are writing B n plus 1; Q n we are writing B n and if we substitute and no and you know put it into a more compact form by going through the steps of minimization. So, we see A n exhort B n, we can have these state table. So, we can where this is the current state again I reset if we it is not specified you can begin with his current state, right. And then we can look at this equation, so B n plus 1 is A X or B n, right. A X or B n is 0 0. So, it is 0. And what is n plus 1 it is just inverse of it. So, this is 1.

So, 0 1 becomes the next state. So, 0 1 this XOR this becomes 1 and A n prime, so it will become just the opposite of it that we already know we have seen from this equation. Then becomes 1 0 becomes the current state XOR is 1 and A n its just gets complimented so this is 1. So, 1 1 becomes an X state. So, 1 1, right XOR 1 1 is 0 only and then 1 toggles become 0. So, next state becomes 0 0. So, 0 0 again you come back to the looping of it cycling of it. So, it is 0 1 and it continues this way, right. And when it is current state is 1 1 we can see that output is A n B n which is 1, fine.

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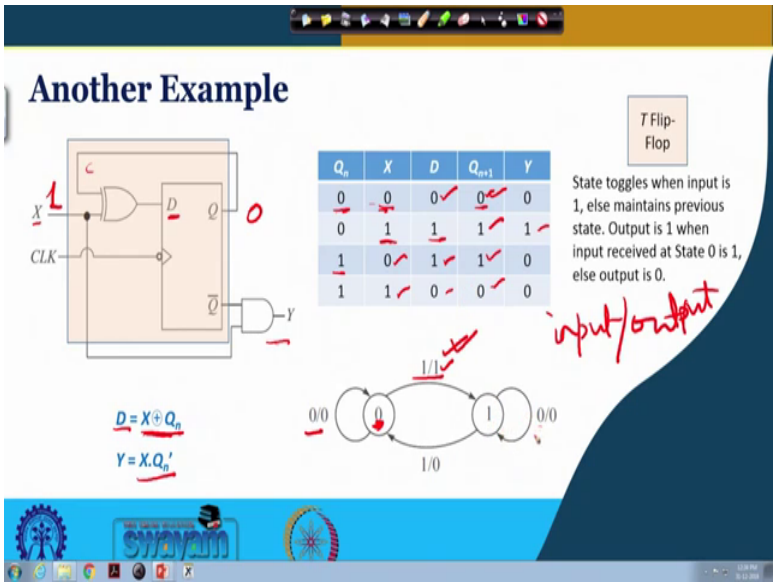

Finally, we look at one again simple example to be for the first class on analysis of thesecircuit, where there is an external input present, ok. So, here is a d flip-flop clock and then there is an external input, right. And there is a output that is getting generated in this manner. So, first step is what; getting the equation at the input of the for the input of the flip-flops only one flip-flop is used. So, D is XOR X XOR Q n that we can see this is Q n is feedback, right X or Q n. And what is y output is X ended with Q n prime, very simple, is it ok.

Now if we just go by this state table method, we can go by any other method, ok. So, state table method then we can see the current state we assume to be 0, if not otherwise specified as I said. And if input could input could be now either 0 or 1 because it is coming from outside we do not know for sure. So, if the input is 0, then 0 XOR 0 is 0, right which will make d flip-flop whatever is the input that will go as the output. So, this makes it 0, ok.

But if input was 1 0 XOR 1 is 1 next value would have been 1, ok. And at that time since X Q n bar is the final output, so this is X 1 and Q n bar is 1 so at the time the output is 1. Now if the state is 1 right and you receive a 0, ok. So, 1 XOR 0 is 1 at the flip-flop input and then the output will become, right. And instead of 0 if you receive a 1 then 1 1 XOR is 0, right output will be 0. So, this is how the circuit works.

So, this circuit every time from current state to go to the next state it looks at the input. And based on the input of course the current state it moves to the next one and generates output, right. So, for this we are looking at a state diagram representation as the analysis result, where the state is only 1 state, ok. So, 0 and output is generated based on the input, directly from the input, ok. So, for this we are showing output not inside the state; earlier the output was generated only by this state, ok. So, we showed it inside the state.

Here for input when it is 0, right and the current. So, this is now 0 right and the current input is 1; state change will take place in the next clock trigger in the next negative edge, but when this is happening, right the output is getting generated. In this same cycle clock cycle itself. So, that shows that is shown in the state diagram side by side with the input. So, this is input and this is output, this is the convention more about this kind of representation modelling we shall discuss elaborately later, ok.

. So, 0 is present, 0 is the current state, input is 0 it will remain at 0 the next value will be 0, output is 0. 1 output is 1 is goes to 1. And then if it is 0, right it will when it is at 1 it remains at 1 output is 0 and when it is at 1 it goes to ah 0 and output is 0.

So, what you can see if you now look at this state diagram this particular circuit except, we if you ignored this output why rest of the thing which is there in this box is nothing but your T flip-flop, isn't it. So, in T flip-flop the state transition diagram if we had seen. So, this part was not there, this part was not there rest of the thing as same, ok.

So, we analyse this circuit and see that this is how the circuit will behave. And this is the corresponding text description that its toggles when input is 1. And maintain otherwise mention maintain previous state and output is when output is 1 when input is received at state 0 is 1, else output is 0. So, that is the analysis result.

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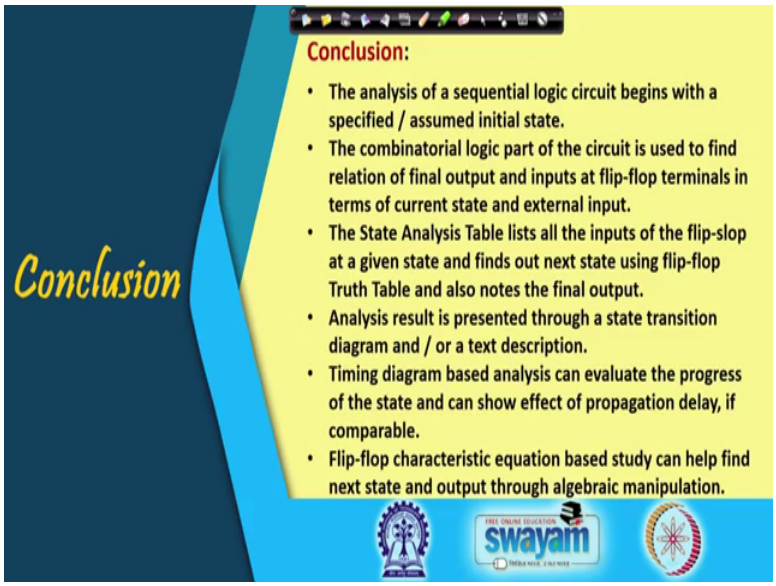

So to conclude: analysis of sequential logic circuit begins with specified initial state. Combinatorial circuit to logic part is analyse to find out the relationship at flip-flop terminals logic relationship and for the output. In the state analysis table all inputs of the flip-flop at a given state is described and next state is obtained, and that serves as the input for current state for the next row of the table.

And it can be presented through state diagram final result or a text description. And timing diagram based analysis is useful to evaluate the progress of the state and it can show the effect of propagation delay; when it is comparable it is very much required and useful. And flip-flop characteristic equation can also be used for analysing the circuit. And for which some algebraic manipulation is required.

Thank you.