Digital Electronic Circuits
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Lecture – 33
Representations of Flip –Flops

Hello everybody in the previous classes we have got introduced to Flip Flops. So, we have seen clock flip flop edge triggered flip flop and we had seen representation of flip flop in the form of truth table.

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So, we shall look at some other representation of flip flop in this particular class, which will be useful for analysis of sequential logic circuit and synthesis of sequential logic circuit which we will come up in future classes.

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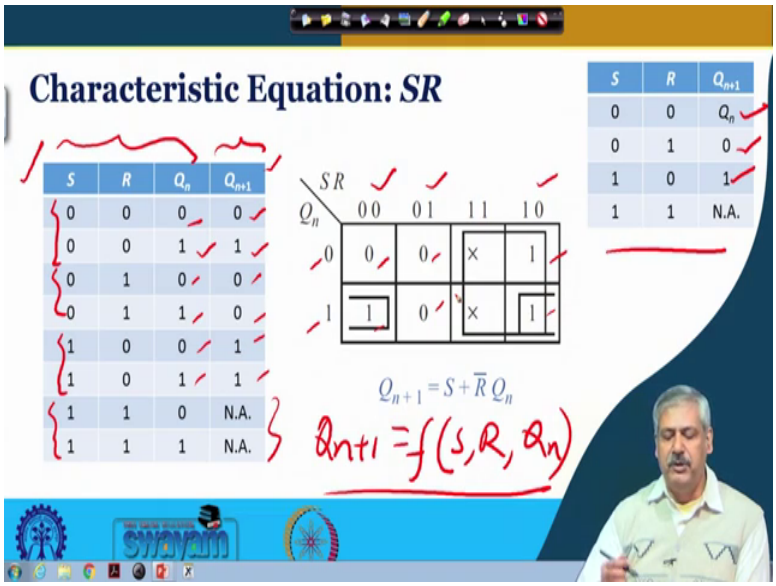

So, we start with SR flip flop and what we discuss now is representation through Characteristic Equation. So, truth table of SR flip flop we had seen before in a compact form like this and more elaborate form which can be represented here ok, so this truth table is also called characteristic table in some of the literature.

So, if you remember that for S and R when input are 0 and 0 then if current state is 0 next state will also be 0, current state is one next state will also be 1 that is previous state is retained ok. If inputs are 0 and 1 then the flip flop will be reset irrespective of what had been the previous state. So, whether it is 0 or 1 next state is 0 and 0, so this is the case we have seen in a more compact representation when it is1 0 it will be set irrespective of the previous value it is 1.

So this is the case in more compact representation and when it is it is 1 1 it is not allowed 1 1 is not allowed. So, if you want to get a characteristic equation that represents this flip flop what we will do, so this is the current value based on which the next one is obtained. So, we get with we form a Karnaugh map or any other minimization technique also is useful.

So, the idea here is we want to represent Qn plus 1 as a function of SR and Qn that is the idea ok. So, you can take mean term base representation and then we can minimise it using Boolean algebra or any other techniques. So, Karnaugh map is handy, so we look at the Karnaugh map based representation of this logic equation right.

So, SR 0 0 if Qn is 0 then the Qn plus one is 0 1 Qn plus 1 is 1 if it is 0 1 it is reset. So, 0 0 if it is 1 0 it is set and 1 1, since it is not allowed we put it put a do not care here that means, from the equation whether we get it 0 or 1 it does not matter because, the value will never appear at the SR flip flop input a case of both being 1 right. So, we shall use that do not care either as 0 or as 1 depending on how the groupings can be obtained and a minimized representation can be made available ok.

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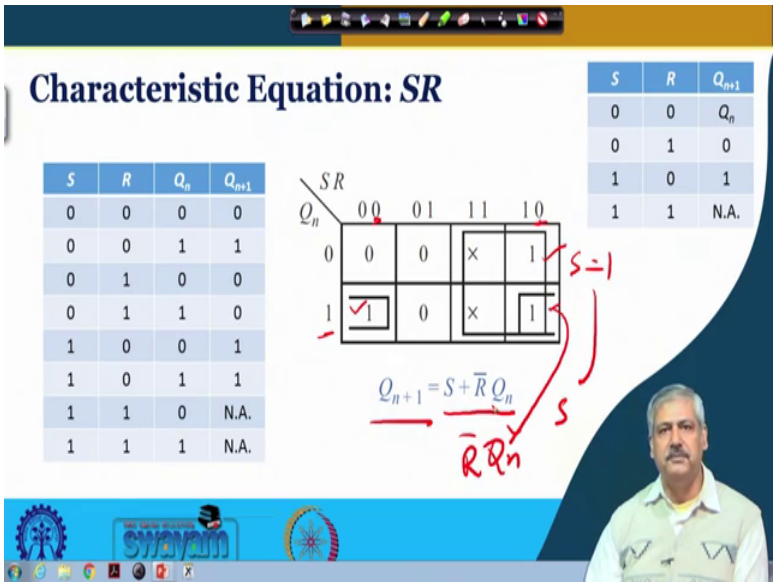

So, for this case what we see the largest group of this ones that can be covered is coming where this do not cares are included and for that we see that S is remaining constant with a value of 1. So, what will be coming here S will come as one of the product term I mean there is no other term which is getting ended with it and this one is not covered this one is already covered, but together you can form a larger group group size of 2 in which we can see that R is 0 here R is 0 here.

So, the variable that will be coming here is R bar one term one literal and the other one is Qn Qn is remaining constant with a value 1, so Qn will be coming for this one ok. So, then we sum it up and we get Qn plus one represented as S plus R bar Qn ok. So, this is the characteristic equation of SR flip flop is it clear right.

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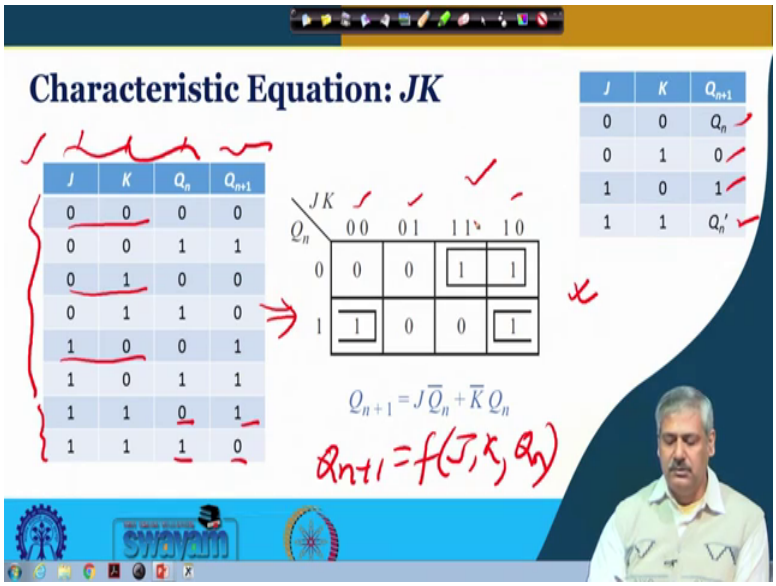

So, next we look at characteristic equation of J K flip flop right, so characteristic equation of J K flip flop again we shall start with the truth table. So, truth table with J K and Qn these are current value based on which the future value will be coming at the next clock trigger and when we try to represent again similarly as a function of J K and Qn right. So, we would like to have a Karnaugh map based representation first and then we shall see how to how to get a minimized representation right.

So, how SR flip flop and J K flip flop you know truth table differ or characteristic table differ. So, up to this 0 0 input 0 1 input and1 0 input they are the same right. So, 0 0 Qn 0 1 0 1 0 1 so only place where it differ is 1 and 1 right. So, when 1 1 is presented as input in SR flip flop it is not allowed in J K flip flop the output the next state toggles. That means, whatever has been the previous state 0 it becomes 1 and if it was 1 it becomes 0, so that is what you have seen over here in a more compact representation.

So, for getting the minimized representation in the Karnaugh map, so 0 0 0 1 and1 0 will be having same entry as that SR flip flop and we can get it directly from the truth table also right for 1 1 for 1 1 now we have got a different entry earlier it was not allowed so we put do not care right here. If it is 0 if it is 1 1 then the next value will be 1 and if it is 1 next value will be 0 right this is understood. So, with this we go ahead with the minimized expression how to find the minimized expression we know the again forming

the larger group possible and we have to cover all the ones if you are looking for SOP representation right.

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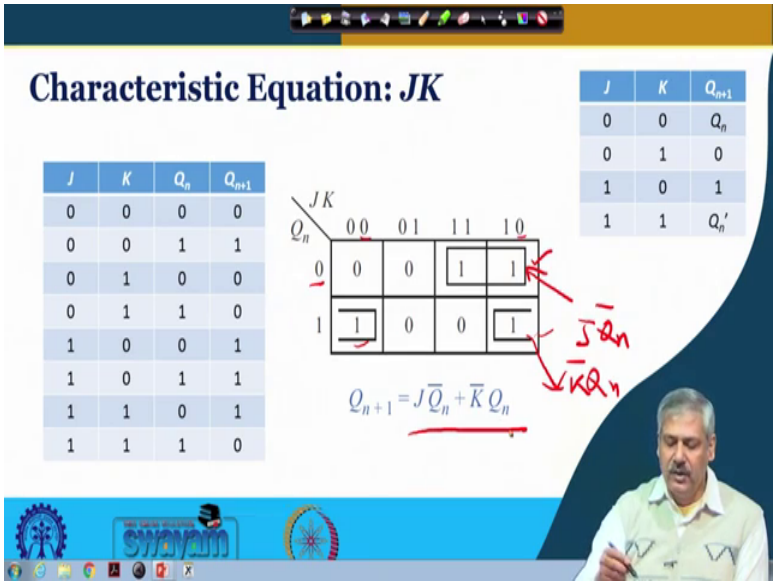

So, this is one group which is covering these 2 1 and this another group which is covering these 2 1 and what we see here that Qn is remaining constant with 0 and J is remaining constant with 1. So, J Qn bar will be 1 product term that is coming and which will represent this group and this group will be represented by similar to what we had see seen in the previous case, so this is your K remaining with 0. So, K bar and Qn is with 1 so Qn so these 2 product term when you sum it up you get the characteristic equation of J K flip flop fine clear ok.

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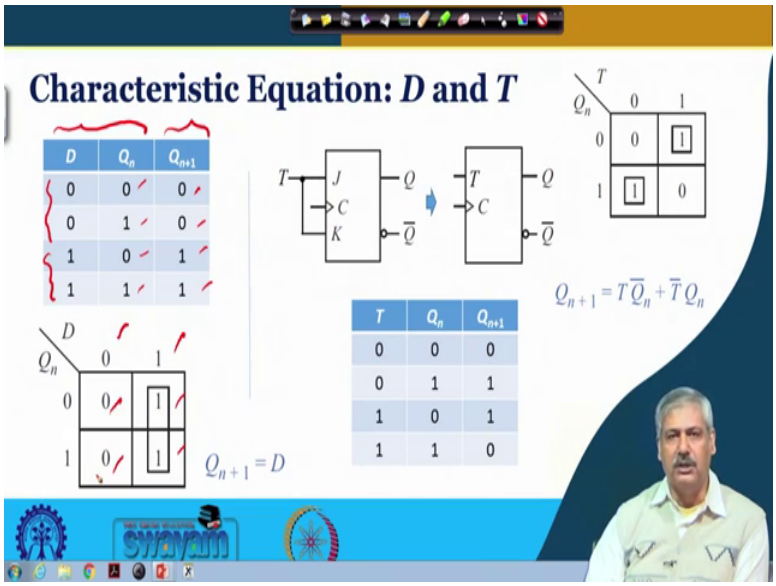

This input is just pushed to there next state right and if 1 1 is presented right. So, the output will become 1 1 irrespective of what is the previous in previous state the next state will be 1 1 right. So, when we put it into the form of a you know Karnaugh map we have 2 variable ok, so for such entries will be required.

So, for D is equal to 0 this is 0 and 0 right irrespective of Qn being 0 or or 1 and D is equal to 1 this is 1 and 1 irrespective of Qn being 0 or 1 ok. So, in this case we have only one particular product term coming out of this because, only one group is sufficient to cover both the ones right and for which D remaining value D is having a value with 1 right. So, Qn plus 1 is simply D ok, so it is just the so this is the characteristic equation of D flip flop clear.

So, here we we introduce another flip flop which we call T flip flop or toggle flip flop right. So, basically if we will try to visualize what would be the internal circuit of logic circuit of T flip flop, then we refer to how J K flip flop is made and then if we connect if we connect both the inputs of J and K and tied together remember between SR and D we had a inverter here there is no inverter ok, from SR to D we had put S as D and then R was D inverted ok. So, there was a not gate here there is no such not gate directly it is connected, so it becomes a single input flip flop right.

So, all those things pushed inside inside the logic circuit within a particular you know group ok, where all the elements are there then what we get is a single input flip flop. Of

course, it is clock positive triggered and all and the Q and Q bar this is outside that is why these bubble is there if it is inside the convention is not to put the bubble I mean this symbols Q and Q bar if they come inside bubble is not put we have discussed this before.

So, this is your T flip flop ok, so this T flip flop then what would be it is truth table right or characteristic table. So, this is your if 0 is presented at the input ok. So, this is like J and K both being 0 0 so previous state will be returned, so if it is 0 it is 0 1 it is 1 and if one is presented so it is like for J K flip flop both the inputs are 1 because T is equal to 1 so the output will toggle alright the next state will become the invert of previous state.

So, 0 becomes 1 1 becomes 0 is it fine right. So, if you try to get a characteristic characteristic equation out of it the minimized expression, so we can see for T is equal to 0 the previous values is returned. So, 0 is 0 1 is 1 and T is equal to 1 so it just toggle so 0 becomes 1 and 1 becomes 0 is it ok.

So, now what we see that larger group of 1 is not possible only 1 member groups are there, so this is 1 group and the other the other one is over here. So, it is T this is T and Qn bar alright and this is the other one is T n bar this is 0 and Q n, so this is your T flip flop characteristic equation is it right. So, you shall make use of all these things later in subsequent classes we shall see how to make use of it.

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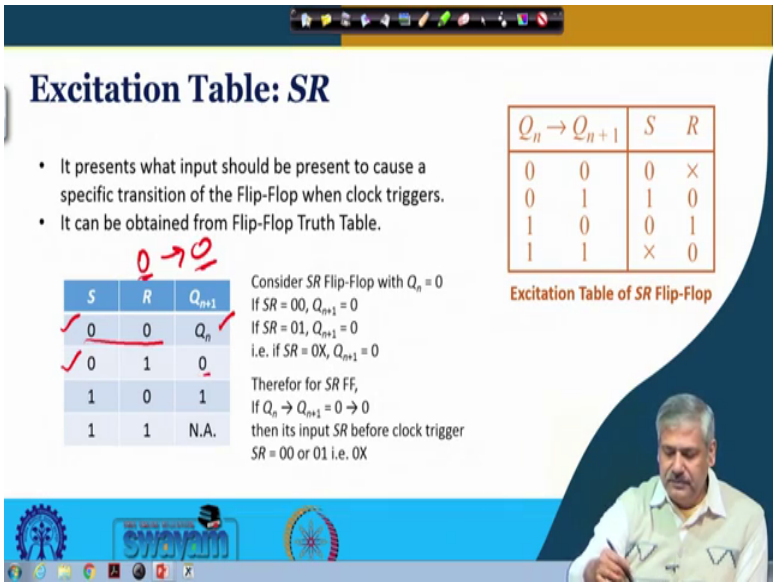

Next is another representation through excitation table ok, this is interesting while characteristic equation and characteristic table or truth table are useful for analysing the circuit excitation table and the one that is to follow we shall discuss that also that is useful that are useful for synthesis design of circuits. So, all those examples we shall take up in subsequent future classes. So, right now we are learning how to represent flip flops in various forms various through various representations.

So, what excitation table tells us so excitation so what sort of excitation should be present at the input of the flip flop right. So, input of the flip flop is S and R for SR flip flop right other one is clock, clock is a simply triggering triggering and based on what is presented at S and R T output you know changes the next state changes and of course, there would be reference to the previous state feedback etcetera etcetera that is another part of the story here. The external excitation external input that is there to trigger need to make a change in the flip flop that is the that is what we are trying to figure out.

So, in that refer in that context, so for SR flip flop we are looking for excitation when we see that the previous state was 0 and next state is also 0 current state to next state right. So, previous state was 0 and next it is also 0 if that is what we observe, then can we figure out what was the input at S and S and R we can figure it out from the truth table if previous value was 0 and next value is also 0 ok, so that means, one in one case we can see that previous state is returned 0 0 right.

So, previous value will be returned so we are talking about 0 previous value was 0 and next value is also 0. So, it will occur when the previous when the input is 0 0 that is possible and instead of input is you know input being 0 0, if input was 0 1 then also the next state will be 0 please understand this part ok.

So, if we refer back to more elaborate truth table of SR flip flop ok. So, we can see if this is 0 1 and previous value is 0 next value is 0 and 0 0 previous value is 0 next value is 0 So in both the cases it is happening right. So, if this is what is observed.

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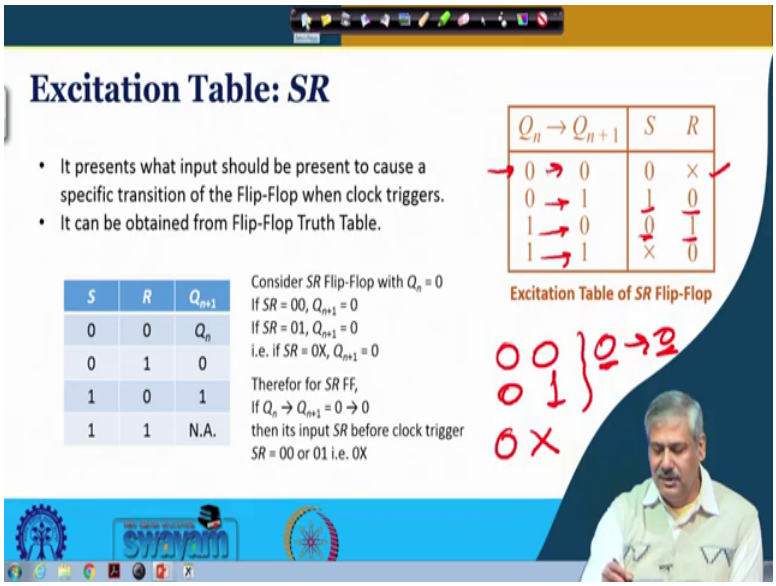

We can say that either of 0 0 or 0 1 was presented at SR to make this happen that it has changed from 0 to 0 and how we can represent it in more compact form, we can write this as 0 X X stands for do not care. So that means, S need to be 0 and R could be any of 0 and 0 or 1 for which if the previous value was 0 next value for sure will be 0 ok, this is what is coming as entry into the excitation table. So, 0 to 0 you can see the input required to be is to be 0 0 or 0 1 in more compact form 0 cross 0 x is it right.

Now, what are the different possibilities of this transition because, it is a 1 bit kind of thing alright it will flip flop contains only 1 bit of information. So, 0 to 0 is 1 possibility that we have already explored, so the other one is 0 to 1 1 to 0 and 1 to 1 right. So, in each of this cases we can figure out if such transition does take place then what has been the excitation at the SR input, so for 0 to 1 right.

So, the previous value was 0 next value is 1, so you can understand from the truth table that input required to be 1 and 0 it is becoming set 0 0 will not occur will not help because, previous value will be returned right. So, if you put 0 0 then 0 will be remain 0 only, so only option left is you have to put 1 and 0 right 1 to 0 0 to 1 and for 1 to 1 for 1 to 1.

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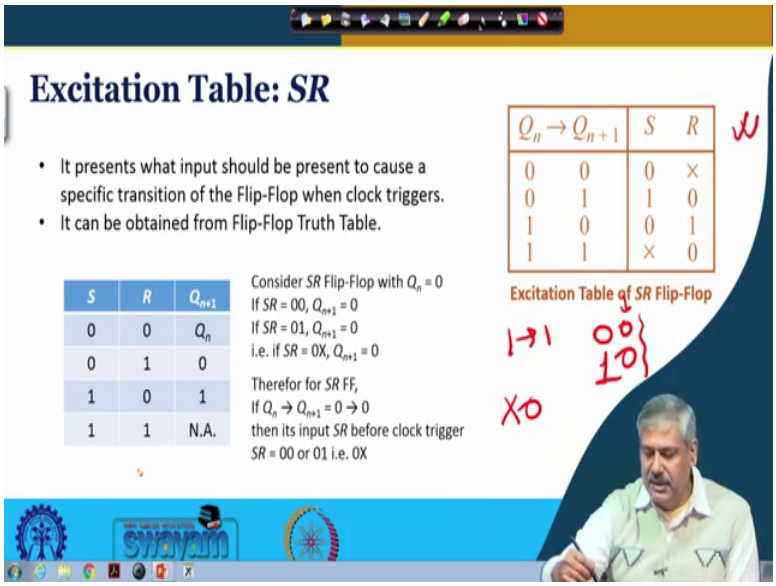

You can have 0 0 case this is 1 to 1 if you have 0 0 right previous value is returned and if we have 1 0 that also will make sure that the next value is 1, in either case for this inputs being present if the previous value is one next value for sure will be 1. So, that is R need to be 0 and S can be any of 0 and 1, so that is the case where we say what we say as cross 0 is it clear.

So, the excitation table of SR flip flop looks now something like this. So, it is re reading of the truth table or characteristic table and putting it in a different manner, that if this is what we desired if the circuit has to move from states 1 state to another and the states are represented by individual elements which are flip flop then to make certain changes happen what should be present at the input ok.

So, this is looking at it from the reverse direction right. Characteristic table truth table if this input is there what will happen what will how the; what change will occur and excitation table if this change is to occur what is to be present as input ok. So, this is the way this 2 representations differ from each other.

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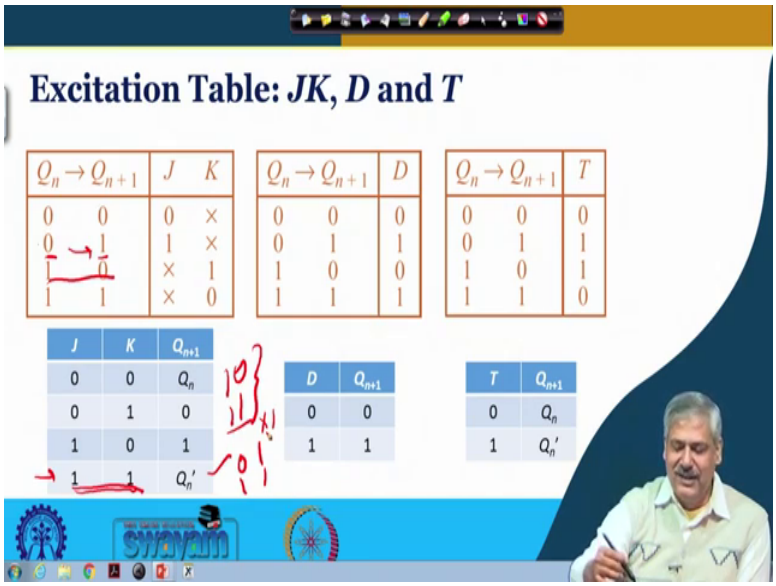

So this is for SR flip flop, so we can see how it would be for other flip flops ok. So, for JK flip flop for JK flip flop, so again this transitions all this 4 transitions are to be considered so 0 to 0 right. So, if 0 0 is present previous state will be returned and 0 1 is there that also will make that the next state is 0 for previous state being 0 ok. So, this is 0 cross and similarly 1 1 like previous case. So, 0 0 and1 0 both the cases it is becoming if the previous state was 1 so the next state becomes 1. So, this 2 we can see we can visualise from SR flip flop excitation table ok. Now coming to the other 2 cases so for 0 to 1 0 to 1 in SR flip flop it was only 1 and 0 ok

But in JK flip flop for 1 1 input we know the output toggles ok. So, if the previous value was 0 the next value will become 1, also for the case when input is 1 1 right. So,1 0 as well as 1 1 why 1 1 because the state toggles 0 becomes 1 and why1 0 because that is how the things get state I mean set similar to SR flip flop setting ok. So, these 2 cases we can see that a 0 to 1 transition is possible, if that is the excitation at the JK flip flop input right. So, we can put this as 1 cross similar to what we did for SR flip flop truth table excitation table.

Similarly, for one to 0 transition earlier it was only 0 1 now 1 1 is also possible because of this toggling part of the truth table in the JK flip flop ok, so this becomes cross 1 right. So, this is how it differs and what is it is significance another things ok, if we want to

realise a circuit using SR flip flop or JK flip flop how these things will come up that we shall explore in future classes.

Now for T D flip flop it is relatively straight forward, so we know if the next state is 0 right the input need to present is 0 if the next state is for 0 to 0 cases1 input need to be present is 1, again from 1 to 0 since next state is 0 input need to be present is 0 1 to 1 again input need to be present is 1. So this is the excitation table of D flip flop and for excitation table of the T flip flop ok.

So, we have got 0 to 0 so previous state is returned, so this is 0 0 to 1 toggling ok. So, input to be need to be 1 1 to 0 again toggling so input need to be 1 and to 1 to 1 previous state is returned. So, input is to be 0 fine so this is how excitation table is through excitation table we can represent different flip flops.

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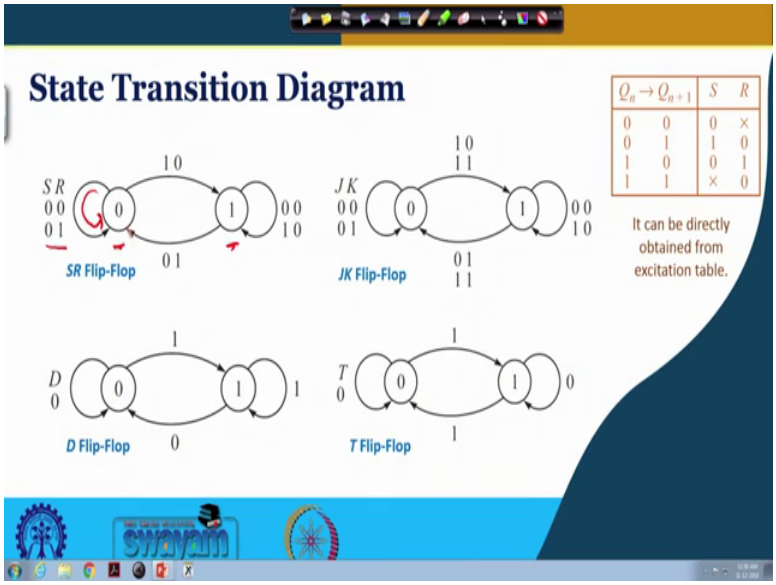

Now the excitation table whatever we have seen there we can put in the form of state transition diagram, this is another way of visualizing what is happening in a flip flop ok. So, for a particular flip flop we have got a one I mean 2 states because, it has it stores one bit information state when it is the output is 1 and state when the output is 0 ok.

Transition means when the excitation comes at the input, so it it is supposed to make I mean it is now can make a transition. So, whether it will make a transition to next state as 1 or it will remain in the same state that is 0 if the present state is 0 ok. So, that is

explained that is visualized pictorially in the form of state transition diagram through a diagram.

So, if we look at the SR flip flop state transition diagram, so this is 1 state with value 0 right and this is another state current state described by 1 ok. Now when it is at state 0 and it receives a input 0 0 what will happen it will remain in the same state, so that is what is shown through this line and this arrow mark will be there to show where it where it is and if it is at state 0 and if it receives 0 1 if it receives 0 1 what will happen it will stay at 0 only is not it right.

So, 0 it is remaining at 0 for the cases 0 0 and 0 1, so we can see from the excitation table also from truth table we can you know in a inverted way we can figure it out right. Now it is at 0 so 0 0 0 1 we have seen if it receives a1 0 what will happen it will get set it will become the out the next state will be become 1 the state of the flip flop will become 1 right. So, it will move to 1 so that is what is shown through this arrow over here from 0 it is coming to 1 and when the input presented is1 0 is it ok. Now it is at state 1 the state at 1 and it is receiving you know whatever is allowed other than 1 1 everything is allowed 0 11 0 and 0 1 right, so these are the 3 things that are allowed for SR flip flop.

So, if it receives 0 0 it will stay at 1 only if it receives 1 1 sorry1 0 it will remain at 1 right and if it receives 0 1 then it goes back to state 0 it goes to state 0 is it ok, sofor each of the stable state right. For SR flip flop this bi stable circuit we can figure out for the allowable inputs what would be the next state and it can we can pictorially depict it through state transition diagram as you have seen here.

So for JK flip flop again current state is 0 right, if it receives 0 and one it will stay here if it is receives1 0 it will go there if it receives 1 1 4 all now 1 1 is also possible, then also it will go to 1 ok. At 1 1 if it receive 0 0 it will stay here1 0 it will stay here and if it receives 0 1 it will go to 0 and 1 1 it will go to again it will toggles it will go to 0 similarly ok. For D flip flop right stable state 0 if it receives 0 it will stay here if it receives 1 it will go to 1.

If it is at 1 if it gets one it will stay there if it is if it receives 0 it will come to 0 and for toggle flip flop if it receives 0 then it will stay at 0 and if it receives 1 it will toggle it will go to one and if at 1 if it receives 0 it will stay at 1 and if it receives one it will toggle and

go to 0 ok. This is the other way other form of representation the another representation through timing diagram ok, in all these cases the delays and other things ok.

However, small it might be is not visible all this representation that we have discussed so far. So, if we represent the flip flop the transitions that are happening for a particular set of inputs and rather all possible set of inputs excitation. So, through timing diagram we can show it ok, so that we shall discuss trough some examples in some subsequent classes.

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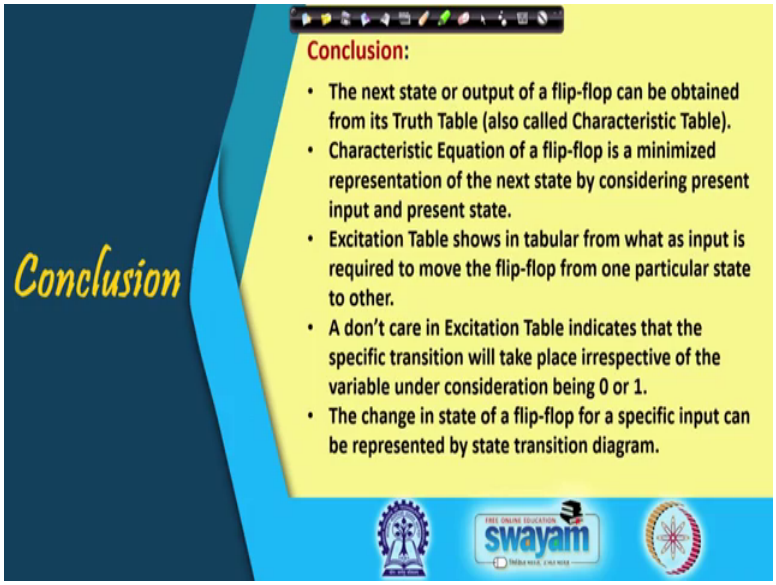

Characteristic equation of a flip flop is a minimized representation of the next state by considering present input and present state. Excitation table shows in tabular form what as input is required to move the flip flop from one particular state to other. It do not care in excitation table indicates that specific transition will take place irrespective of the variable under consideration being 0 or 1 and the change in state of a flip flop for a specific input can be represented by state transition diagram I mean when if you look for a pictorial description.

Thank you.