Digital Electronic Circuits

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Lecture - 32
Edge - Triggered Flip – Flop

Hello everybody, in today's class we shall discuss Edge-Triggered Flip Flop. So, in the last class we introduced ourselves to sequential logic circuit the fundamental primary elements of it we discussed SR latch and SR clocked SR latch.

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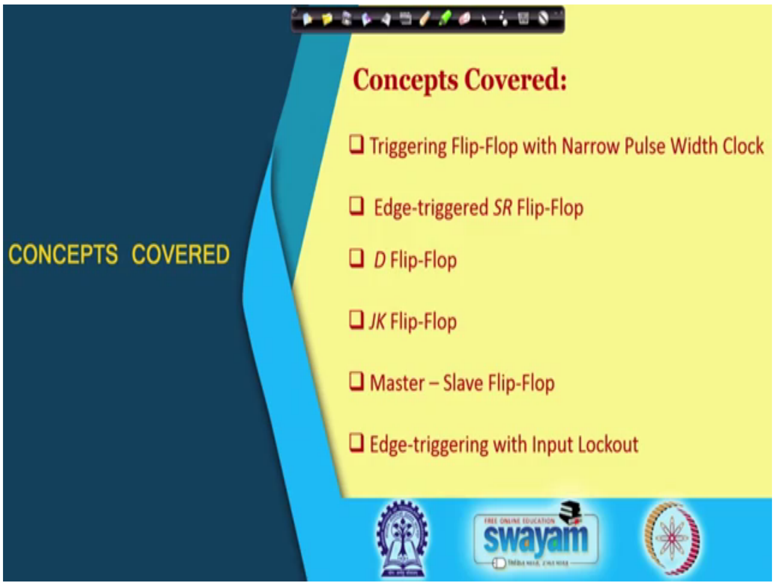

CONCEPTS COVERED

Concepts Covered:

- ❑ Triggering Flip-Flop with Narrow Pulse Width Clock
- ❑ Edge-triggered *SR* Flip-Flop
- ❑ *D* Flip-Flop
- ❑ *JK* Flip-Flop
- ❑ Master – Slave Flip-Flop
- ❑ Edge-triggering with Input Lockout

And we found that how a level triggered SR flip flop is made ok.

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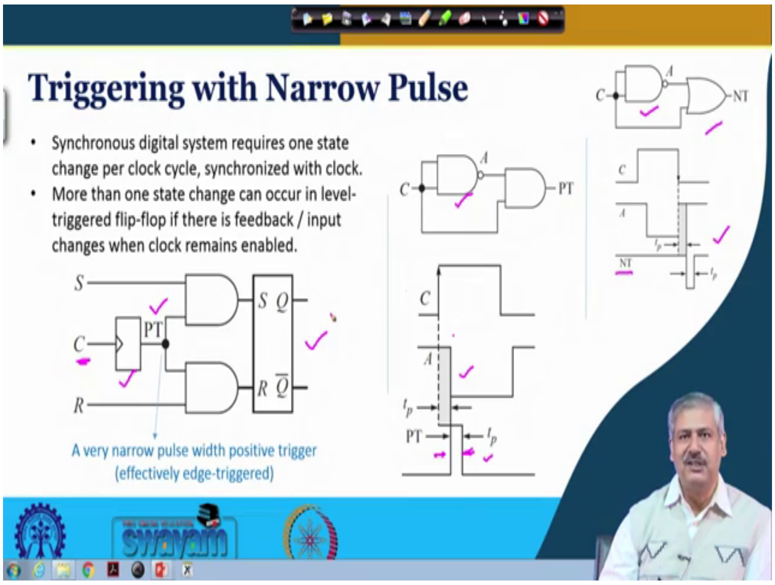

Triggering with Narrow Pulse

- Synchronous digital system requires one state change per clock cycle, synchronized with clock.
- More than one state change can occur in level-triggered flip-flop if there is feedback / input changes when clock remains enabled.

A very narrow pulse width positive trigger (effectively edge-triggered)

Now, why we require a S triggered flip flop ok. We require it because the when it is level triggered during when it is the clock level, the clock output is high so the output can change. And if there is any feedback from output input or some input is changing I mean there is some transients and other things that is coming into the picture from different other part of the circuit. So, that might cause more than 1 change in the state during the period the clock remains enabled is it clear.

So, instead of 1 state change we can have more than 1 state change taking place. And that is not desired and that might put the different you know calculation out of gear in the design process or in the implementation process. So, we need to ensure that only 1 state change takes place and that place synchronous with the clock and for that we are looking for something called edge triggering.

So, edge occurs only you know very short period I mean when the clock is changing. So, either positive edge triggered or negative edge triggered if that is the way it works then we can ensure that only 1 state change will takes place per clock cycle is not it. So, to do that people have thought about various means so, we shall discuss them. So, 1 thing that immediately comes to mind is to make the clock pulse width during which it remains enabled very narrow ok. So, narrow that it is of the order of the propagation delay and by the which the feedback or some changes that is coming from other part of the circuit because of clocking in that particular cycle.

So, by that time it comes it has become disabled see if the clock the pulse high has become low if it is a positive high level triggered flip flop ok. This is the idea that affect of this clock clocking right that will be not getting reflected back in this particular cycle itself that is the idea. So, for that people have thought about the clock is the normal clock here and a pulse forming a circuit ok. And this is giving a positive you know this edge triggering ok.

So, this pulse forming a circuit so 1 way of you know getting it something like this we had seen in the discussion related to hazard before if you remember ok. So, this is effectively a NOT gate. So, the clock is going high here from say low to high at that time. So, this a NOT gate output after the propagation delay it will go from high to low right. And when you and these two then for a short period after this propagation delay right you can see a small positive going pulse.

So, this clock will be available only for this circuit ok. So, because directly getting a clock with a very narrow pulse it is difficult, I mean getting very stable clock. So, a pulse forming circuit like this ensure a small a narrow pulse width ok. Similarly if you want a negative going you know negative going edge a negative a pulse a small pulse width narrow pulse width for negative triggering ok. So, if it is low level triggered basic circuit basic flip flop ok.

Then at that time you can have not and or combination ok. And you can see that we can get a narrow pulse width which is negative going ok. So, for this particular circuit though the basic part of the circuit is level triggered, but effectively you are getting a edge triggering this is not actual edge triggering, but effectively it is edge triggering ok. So, this we can consider and go ahead this ensures one this thing.

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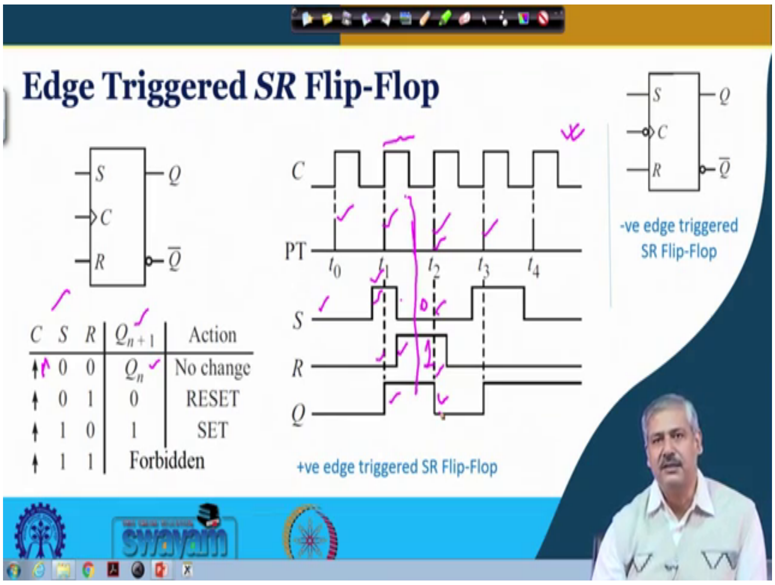

Edge Triggered *SR* Flip-Flop

C	S	R	Q_{n+1}	Action
↑	0	0	Q_n	No change
↑	0	1	0	RESET
↑	1	0	1	SET
↑	1	1	Forbidden	

+ve edge triggered SR Flip-Flop

-ve edge triggered SR Flip-Flop

So, again what we shall see what we shall try to do is to again make a compact representation and by which for edge triggered circuit is edge triggered SR flip flop we shall have a representation like this, where this you can see this triangle like shape here that indicates that it is a edge triggered ok. So, absence of any bubble here inverter means it is positive edge triggered and presence of a bubble like this, that is a inverter ok. So that means it is a negative edge triggered is it clear and for the truth table.

We can indicate this by putting this arrow mark going upward that it is positive edge triggered and when this edge comes so, 0 0 the now we are indicating that only one state change is taking place per clock cycle it is we are ensuring. So, then the previous value is written 0 1 it is 0 1 0 it is 1 and 1 1 as was discussed before it is forbidden and so the corresponding timing diagram ok. So, the way we had seen before, now we can see that whenever in the earlier case if there were when it is high more changes in S and R occurs, I mean then it would have been reflected.

But here it will not be reflected, only in this edges this positive going edges in S triggered flip flop the circuit is state is allowed to change ok. So, at that time it will see what is the value of S and R. So, here it was allowed to change Q as 0. So, that time S and R are 0 so no change ok. So, here again it is at T 1 it is allowed to change at that time it finds that S is equal to 1 and R is equal to 0 ok. So, then the output becomes 1. So, after that here the clock is high this has become 0 this has become 1 you can see that thing if I draw the diagram. But no change in the output has taken place, had it been level triggered immediately there would been a change.

So, that is not what is happening and it will happen again I mean it will depend only again in the this edge whenever it comes and depending on the value of S and R at that time so S is equal to 0 and R is equal to 1 ok. So, it gets reset it becomes value become a 0. So, this is the way it progresses this is a difference between edge triggered and level triggered flip flop and their timing diagram.

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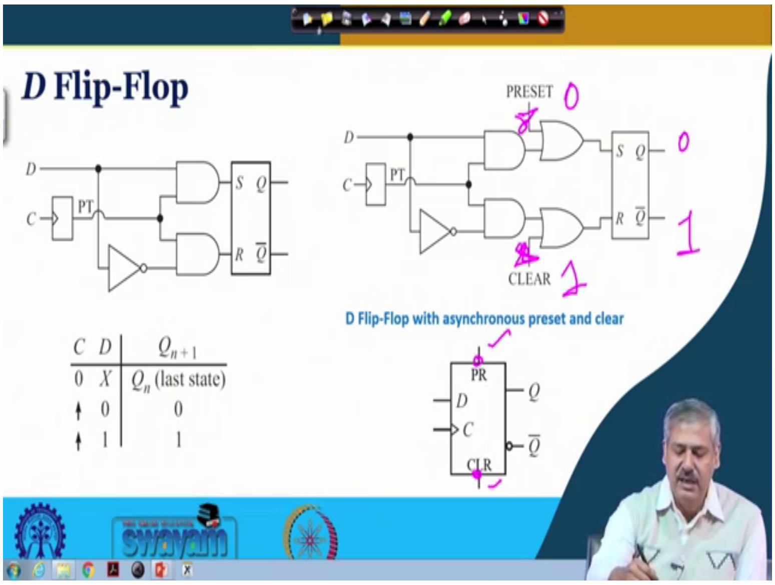

D Flip-Flop

C	D	Q_{n+1}
0	X	Q_n (last state)
↑	0	0
↑	1	1

D Flip-Flop with asynchronous preset and clear

So, now we look at other varieties of flip flop that is used in the sequential logic design so one is called D flip flop. So, what is how D flip flop is designed how does it look like? So, the D flip flop the we know this is basic the SR flip flop part of it. So, this was S input and this was R input and this is the clock that is already known to us. So, you put a inverter between S and R by which this there becomes only one input to it because S and R are connected in this manner ok.

So, this is a single input of course, the clock trigger is there I mean other than that clock and the Q is the output and Q bar of course, a complementary output is there. So, this is the way the flip flop is arranged ok. So, for D flip flop whenever the clock is you know 0 no or 1 I mean the no edge has come this is normal say 0 or 1 ok. So, irrespective of the previous value will be written. So, whenever it is 0, so S is 0 inverted here. So, R is 1 and edge comes what will happen it will get reset.

So, if there is a 0, 0 will be there in the output and instead of these if this was 1 then this is S is 1 and this will be 0 because of the inverter right. So, the output will be when the h comes output will be 1. So, whatever is the input that gets transferred to the out and remains stored there remains stored there ok. And this is how the D flip flop works and more of it is application we shall see later. Now you will see that all these circuit when we employ in complex sequential logic you know implementation.

So, we need in certain cases clearing the circuit or presetting the circuit clearing the state or presetting the state at a given time one important requirement is during initialisation ok. So, you have connected many flip flops and you have made a complex circuit out of it. So, how would you start where from which state do you start usually you may want to start it from say 0 0 0 or say 1 1 1 whatever it is or it could be from 0 1 0 something which you know is predefined ok. So, in that case we need something by which it can be initialised in that manner ok or some state can be introduced without the application of the clock.

So, that is called asynchronous presetting or synchronous clearing so for that what we can do. So, this is the clock part of the circuit right. So, we can just put a another such or gate right and whenever we put preset is equal to 1 and a clear is equal to 0. So, this is 1 and this is 0 which will make irrespective of the clock. Now clocking is not required that is why it is asynchronous whenever it is made like this then this is your, this will be set to 1 and this will be 0 and only when both of them are 0 this or gate will be acting on this input when both of them are 0 right this is a non forcing input for the or gate.

So, whatever is coming from here this AND gate and this AND gate through clocking and all through whatever is present in the D flip flop so that will be deciding. What is the output? So, similarly for clearing will make it over 1 this is 1 and this is 0. So, that will make it 0 and this will become 1 right this is clear. So, this is shown for a D flip flop and then in the case of symbol again to make a compact representation. So, in we putting here pr and clear that is preset and clear.

So, if it was this because it is active high preset active high clear. So, if active low then we would have put a bubble here and the put a bubble here. So, instead of you know this high if there was a NOT gate put before this. Then we would have put a bubble over there is it clear. So, this has been shown for D flip flop it could be for SR flip flop also it could be possible for any flip flop this kind of you know asynchronous preset clear can be designed.

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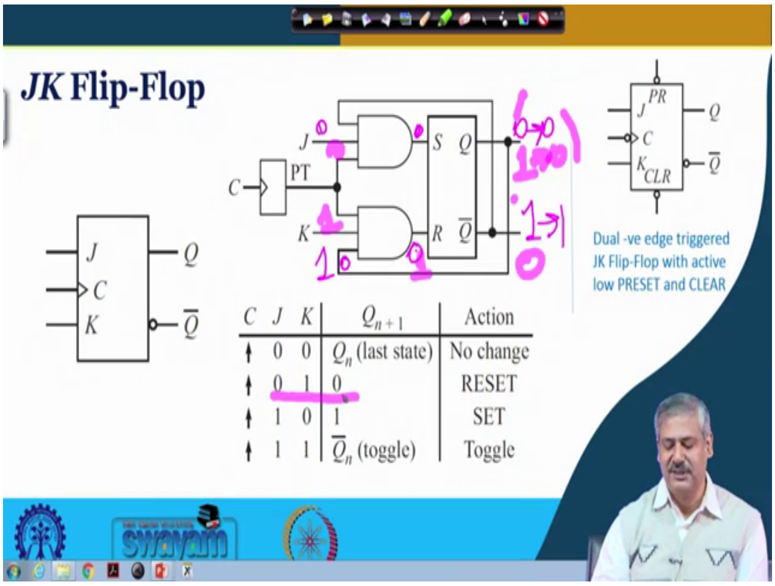

JK Flip-Flop

Dual -ve edge triggered JK Flip-Flop with active low PRESET and CLEAR

C	J	K	Q_{n+1}	Action
↑	0	0	Q_n (last state)	No change
↑	0	1	0	RESET
↑	1	0	1	SET
↑	1	1	$\overline{Q}_n$ (toggle)	Toggle

Now, we come to another type of flip flop which is called JK flip flop. So, JK SR was set reset there were two inputs. So, JK flip flop you can see that two inputs are there. So, this JK flip flop if you see how the connection is made. So, this is the normal SR flip flop these SR latch and the SR flip flop with clock, so this third input was not there ok. So, without this is a standard SR flip flop please understand this part.

So, this feedback is eliminate this a feedback then this is your S and this is your R isn't it is a standard SR flip flop. So, what has been done to get the JK flip flop is Q is connected to this R and we are giving a different name of the input K to distinguish to differentiate it from SR flip flop. And Q bar is coming to where the S was there as a third input to the AND gate ok. And we are giving the name J is it fine. So, this is how the JK flip flop is made right.

So, how the truth table now becomes different from the truth table we had for SR flip flop ok. So, if we investigate we see that whenever J and K are 0 and 0 this is AND gate 0 is the forcing input. So, this input will be 0 and 0 irrespective of what is feedback or whatever you know the other things I mean whenever the clock appropriate clocking is there alright. So, what does it mean? The last value will be there clear first part right.

Then if this is 0 and this is 1 again 0 is a forcing input. So, this will be 0 right and this input this input if Q was 0 and this is 1 please understand this part; if Q was 0, 0 will be feedback here. So, this will be 0. So, 0 0 means previous value will be written. So, if 0 was there it will at 0 1 will remain at 1 ok. Instead if previous value was 1 and then this was 0. So, this 0 comes over here this 1 comes over here and clock is enabling it so this will become 1.

So, 0 and 1 what does it mean the output will become 0 it is reset. So, in either case irrespective of the pulse value was 0 or 1 the output becomes 0. So, 0 1 output becomes 0 is it clear. So, from symmetry you can say for 1 0 the output will become 1. And then comes the last case for which actually this feedback is given and SR flip flop is different from JK flip flop otherwise thee remain the other three rows of this truth table is same.

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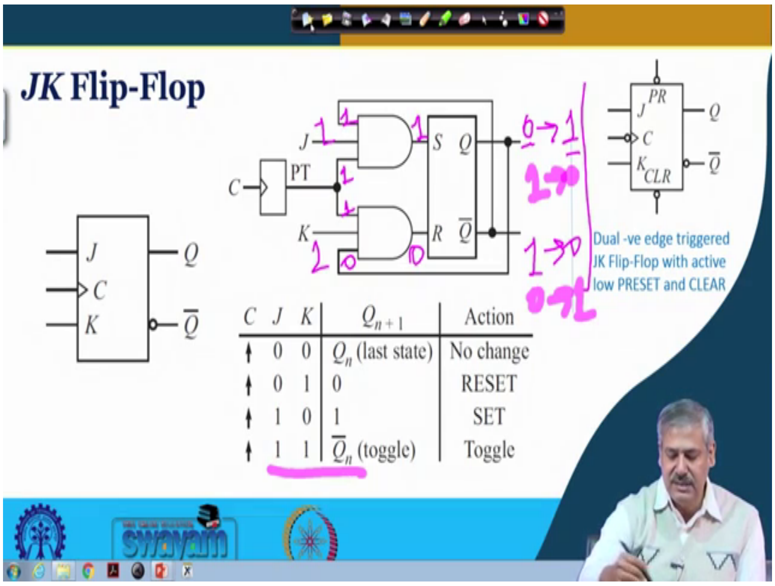

JK Flip-Flop

C	J	K	Q_{n+1}	Action
↑	0	0	Q_n (last state)	No change
↑	0	1	0	RESET
↑	1	0	1	SET
↑	1	1	$\overline{Q}_n$ (toggle)	Toggle

Dual -ve edge triggered JK Flip-Flop with active low PRESET and CLEAR

So, when it is 1 and 1 and say this is 0 and this is 1 the previous value and you have made it to 1 1 and the clock is enabled now. So, this 0 comes over here ok, this clock this 1 goes over there and we are just you know activated the clock at that time. So, what has happened to the output? So, 1 1 1 this output is 1 AND gate and this is 0; so this is 0.

So, 1 and 0 S and R the output will become 1 and this output will become 0 is it clear, so if this was 0 it becomes 1. Again from symmetry you can figure out because it is identical right. So, if the previous output was 1 and this is 0 and it would have been 0 and this would have been 1. And so basically it toggles at that time is it clear. So, this is no more forbidden which was the case for SR flip flop the 1 1 input.

Now if 1 1 is given the previous state is just inverted. So, this is what is the JK flip flop truth table and the symbol will be like this. And if you are having a what is that called active low preset and clear so this is the way the symbol will be presented. So, this is basically may referring to negative edge triggered JK flip flop.

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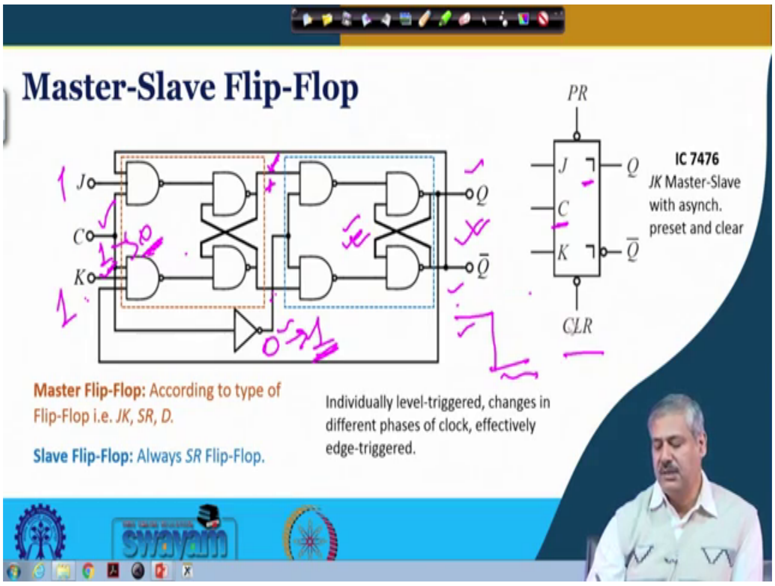

Master-Slave Flip-Flop

IC 7476
JK Master-Slave with asynch. preset and clear

Master Flip-Flop: According to type of Flip-Flop i.e. *JK*, *SR*, *D*.

Slave Flip-Flop: Always *SR* Flip-Flop.

Individually level-triggered, changes in different phases of clock, effectively edge-triggered.

Now, we look at something called master slave flip flop ok. So, when you say master and slave so there will be something which is driving the circuit and slave means the one which is just following it just carrying it to forward ok. So, the JK flip flop example we can take. in that in this case you see that this is one SR flip flop, so the slave is always SR flip flop ok. And the master is depending on the flip flop type here we are talking about JK flip flop right.

So, this is the JK flip flop with the feedback and all and this feedback is coming over here which will be carried to the next level ok. So, there is an intermediate output at this two points. And what is notable here is that there is a clock which is connected, I mean what about the clock goes here the inverted the clock if it is active for this is logic high so when it goes to logic low right, so when it goes to logic low.

So, this will go from logic low to logic high. So, when this is active at 1 this is a level triggered each 1 of them is level trigger you can see that there is no pulse you know forming circuit and other things are there. So, when this is active this is inactive and when this is inactive this is active. So, how does it actually it then help? So, when it is active so because of the input whatever the input is present the output comes up to the master output; it cannot go to the final output because this part of the slave is now inactive ok.

Now, slave when this becomes inactive 0 now slave becomes active right. So, the output of this master whatever was there this inactive means the previous state will be written this these are all 0 is means 1 1. So, previous state will be written so master output is written so, that master output now goes to the final output ok. So, now, even if the feedback is there right and it is asking for to toggle and all. But the clock I mean if the both the inputs are 1.

So, the value will be coming and resting I mean value will be coming here, but it will not be able to change the output. Because the master is now disabled, because clock is low and when clock becomes high slave becomes disabled. So, because of which this is a toggles, but the output will come over here ok, but it will not be going to the next stage slave stage. So, only 1 state change is you know guaranteed within this. But if something is coming from different other places when this clock is high it need to be stable so that is another part of the story.

And effectively then we are getting that whenever it goes it was high master has changed whenever it has gone low this slave is changing ok. And after that there is effectively no change can occur slave can change here, but no way the output can alternate at time because the master has gone low. So, effectively you are getting a negative edge triggering over here is not it. So, that is another way of getting the edge triggering in a roundabout way you can say ok, where; individually they are level triggered and we do not have restriction on narrow pulse width and things like that ok.

But there are conditions like the input need to be a bit stable input need to be stable and all ok. And instead of JK flip flop you want SR master slave or D master slave then we need to have this initial stage to be D or SR and the slave will always be SR flip flop because there are two inputs coming from Q and Q bar of the master ok. And this is one way people have I mean this is the compact way people have make made a presentation of representation of master slave flip flop. So, the clock is level triggered, but the output is changing at the following edge ok. So, this is your flip flop indicator and with there is a preset and clear available ok, then asynchronous so it will be indicated in this manner.

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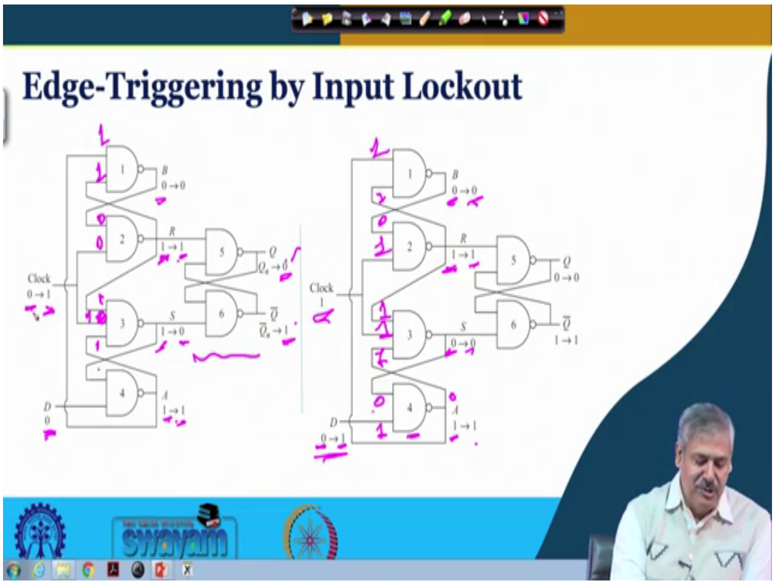

Edge-Triggering by Input Lockout

Now, we shall look at edge triggering by input lockout, this is something which is perhaps you would be finding very close to what an edge triggering circuit should look like. So, no down therefore, to a no narrow pulse width and the pulse forming circuit or master slave and basically stable input at the masters. So, all those things apart can be you know conditions can be eliminated, and let us see how it works and we take a D flip flop as an example ok.

So, the basic circuit you can see that there is 1 kind of you know latch here this is another latch and this is another latch ok. So, 1 2 3 4 and 5 6 right, and one point to be noted that here there is a this 3 is 3 input rest all are 2 input. Now we see how this circuit works how this circuit works we shall go through examples. So, you consider that D is initially 0; D is initially 0 and the output could be 0 or 1 that part we shall we it can be any 1 of them ok. These output is only linked here, it is not feed back to any other stage right.

So, whenever D is 0 this output is because it is a forcing input for the NAND gate so this output is 1. And we are talking about the clock remaining this is a positive edge triggering we are talking about. So, clock is at 0 means it is inactive if the output is not changing the value. So, let us see how it is happening. So, clock is 0 means this is 1 and this is also 1 right. So, this 1 is feedback here, this 1 is there coming from this feedback and clock is also 1 right. So, this 1 is again going back to this place this 1 is over here so 1 1 is making it 0 right.

So, 1 1 the previous value will be written if it is 0 it will be 0 it will be it 1 it will remain 1 and vice versa I mean the Q n will Q n will be just the opposite of it is it clear. Now what happens changes from 0 to 1 ok? So, what are the gates that will get affected first? The gates that are connected directly to the clock ok, so clock becoming so sorry this is 0 and this is 0 and this 0 is feedback here ok. So, clock becoming 1 means this is becoming 1, so this 3 ones this 3 ones make it make it 0.

Now clock has become 1 here, but this particular gate this 0 is over there. So, this 0 is holding it to 1 is there any other change? No, because when this 0 is it has become here. So, 0 feedback here this 0 is holding back it to 1 there is no such change. So, this 1 and this 1 together it is 0. So, what we see that 1 and 0 will be occurring ok. So, that will make this 0 go to 1 because for the NAND gate this is forcing input and this 1 1 feedback it is 0. So, whatever be the previous value 0 or 1 this will be 0 and this is 1 ok. So, if D I is D is 0 Q becomes 0 that is what the flip flop how it should look like.

Now whether it is edge triggered or not, let us see. Now the clock is at 1 right we have seen that when clock becomes high it is changing like this clock has become 1 right. So, what is the what are the outputs at that time this was 0 D was 0 ok. So, D was 0 means this is this was 0 and this is 1 clock is at 1, this is 0 means this was 1 this was 0 right and what else? So, this is 1 and this 0 is coming over here right I am talking about this stage I am not have not talked about you know changes ok. And this 1 is coming over here. So, this 0 is here clock is 1 ok.

So, now, all the inputs have been understood and we are over here at this place right before changing the D. So, clock is 1, now we have changed from 0 to 1. What happens when clock changes from 0 to 1? So, we have to see where it gets first affect where it first affects. So, it first affects this particular NAND gate because D is connected only to that right. So, 0 to 1 when it becomes so this becomes 1. So, what is the corresponding effect? So, these gate already the other input of it is 0 ok.

So, 0 and 1 it will remain at 1 only, isn't it. So, and this 1 is fed back here and it remains 1 only so it remains 0. So, there is no nothing no other gate is getting affected. So, at this change you see the 1 that are important so all of them are remaining at the previous value. So, even if input has changed the input is locked out. So, this is what is happening, even if the clock is high change over here is not making any difference right. Only one clock from goes from 0 to 1 there is a difference there is a change occurring.

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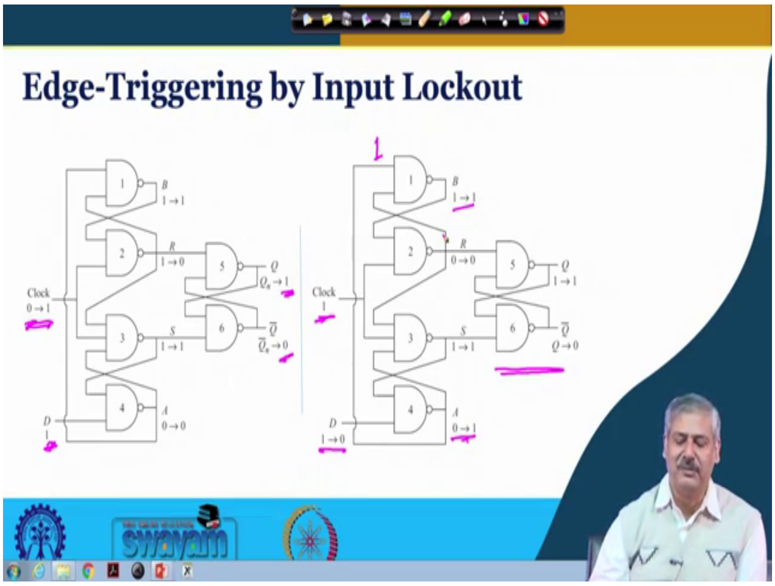

Edge-Triggering by Input Lockout

And you can see the same thing occurs if the situation was for D is equal to 1 and clock was 0 ok. You can you know see that the same way you can look at if you the changes that are taking place ok. That this output will become 1 and this output will become 0 at when the clock goes from 0 to 1, and when it is clock is at 1 and if input changes from 1 to 0 ok. This output will change from 0 to 1; this output will change from 0 to 1. So, this 1 gets feedback here, but the other input of it is 0 so 0 will hold back it to 1 and no further change that gets transferred to the final stage ok.

So, similar analysis like what we had done before so if you do we shall see that and the immediate outputs are shown. That 0 to 1 there is a change the output becomes 1 if this is 1 and when clock is at high then at 1 when it is 1 to 0, the out the changes are taking place only here. But after that no further changes there.

So, basically though there is a change in input the input is getting locked out ok. So, this is so what we note and this is way you can get edge triggering for D flip flop by locking out the input. So, similar thing we can do for SR JK other type of flip flop.

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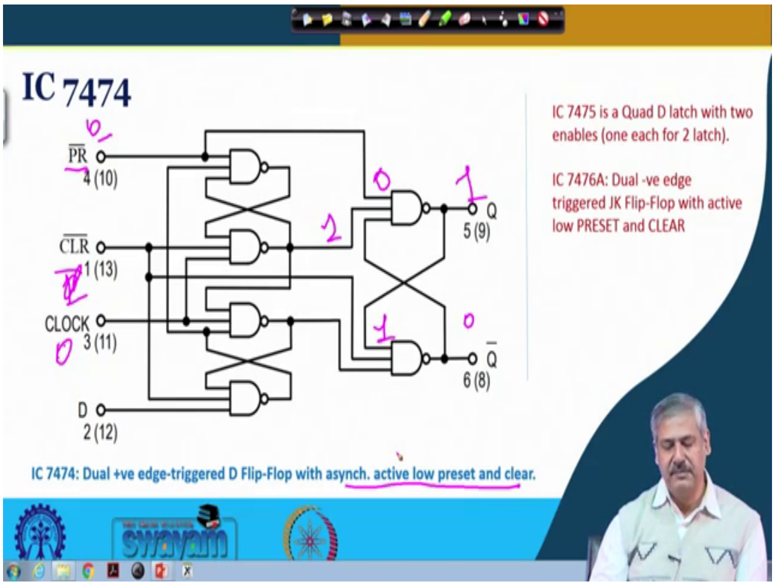

IC 7474

IC 7475 is a Quad D latch with two enables (one each for 2 latch).

IC 7476A: Dual -ve edge triggered JK Flip-Flop with active low PRESET and CLEAR

IC 7474: Dual +ve edge-triggered D Flip-Flop with asynch. active low preset and clear.

And finally, for a D type edge triggered flip flop we can put asynchronous preset and clear and this is a standard circuit that I show you IC 7474 ok. It is a dual; that means two such say positive edge triggered flip flop is there with asynchronous active low preset and clear. So, this preset and clear are there you can see this preset input is going directly over here ok.

So, if it is 0 and this is 1, so this will become 0 and this will become 1 right. And then this output we become 1 and this output will become 0 right. So, that is active low so when it is low it is becoming high right. So, if you look at the cases when the clock is 1. So, basically the clock will be 1 at that time sorry clock is inactive clock. So, this is 0 and this is 1 and so this many things you can see is it fine ok.

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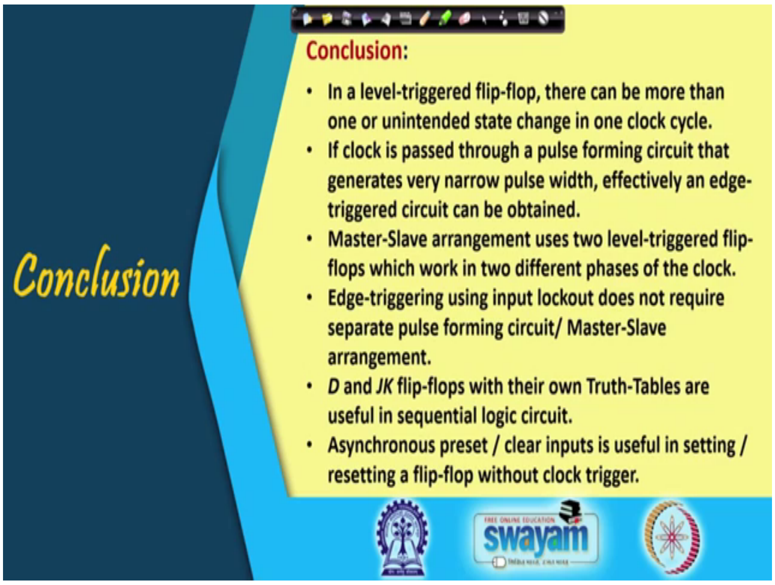

Conclusion

Conclusion:

- In a level-triggered flip-flop, there can be more than one or unintended state change in one clock cycle.
- If clock is passed through a pulse forming circuit that generates very narrow pulse width, effectively an edge-triggered circuit can be obtained.
- Master-Slave arrangement uses two level-triggered flip-flops which work in two different phases of the clock.
- Edge-triggering using input lockout does not require separate pulse forming circuit/ Master-Slave arrangement.
- *D* and *JK* flip-flops with their own Truth-Tables are useful in sequential logic circuit.
- Asynchronous preset / clear inputs is useful in setting / resetting a flip-flop without clock trigger.

So, with this we conclude today's discussion. What we have seen? In a level triggered flip flop there can be more than one or unintended state change in one clock cycle if clock is passed through a pulse forming circuit that generates a very narrow pulse width, effectively an edge trigger circuit can be obtained. Master-slave arrangement uses two level triggered flip flop which work in two different phases of the clock.

And edge triggering using input lockout does not require separate pulse forming circuit or master slave arrangement. And D and JK flip flops we have seen; how they work their truth table. And we also noted that asynchronous preset clear inputs are useful in setting resetting a flip flop without clock trigger.

Thank you.