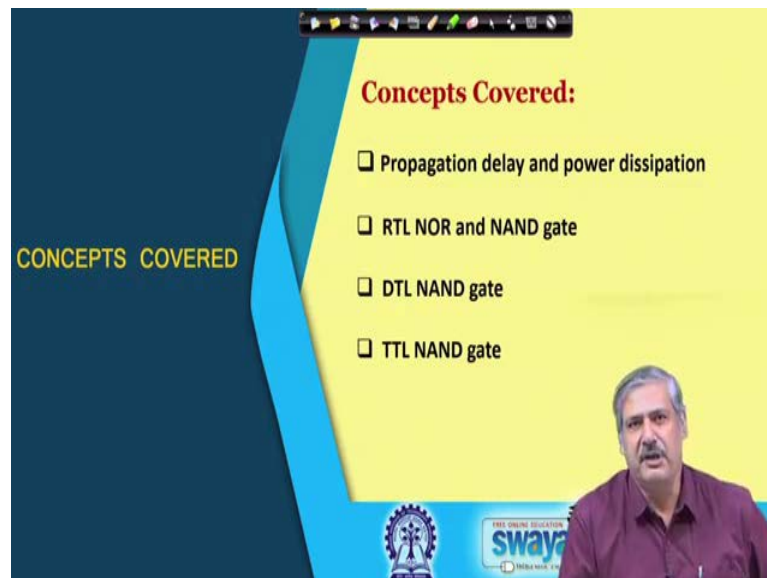


Digital Electronic Circuits
Prof. Goutam Saha
Department of E and EC Engineering
Indian Institute of Technology, Kharagpur

Lecture – 03
Performance Issue and Introduction to TTL

Hello everybody. In the last class we looked at use of transistor as a switch and we also looked at important performance metrics like noise margin, fan out, and some other parameters like logic swing, transition width, with the help of an example which was a simple resistance and one single transistor based inverter.

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The slide features a dark blue background on the left with the text 'CONCEPTS COVERED' in yellow. On the right, a yellow background contains the title 'Concepts Covered:' in red, followed by a list of four items, each with a square checkbox:

- Propagation delay and power dissipation
- RTL NOR and NAND gate
- DTL NAND gate
- TTL NAND gate

In the bottom right corner, there is a video inset of Prof. Goutam Saha. At the bottom center, there is a logo for 'swaya' with the text 'FREE ONLINE DELIVERATOR' and 'INDIAN INSTITUTE OF TECHNOLOGY'.

Today we shall extend that discussion and look at some other performance metrics. And then we shall slowly introduce ourselves to TTL - Transistor Transistor Logic.

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Propagation Delay

- Due finite switching speed of transistors and circuit capacitances

t_{PHL} : Delay in changing output from H to L
 t_{PLH} : Delay in changing output from L to H

Propagation delay, $t_{PD} = (t_{PHL} + t_{PLH})/2$

t_r : Rise time \rightarrow 10% to 90% of max.
 t_f : Fall time \rightarrow 90% to 10% ...

The slide includes a circuit diagram of an inverter with handwritten annotations: V_{in} , V_{out} , R_B , R_C , and V_{CC} . It also features a graph of input and output waveforms with time intervals t_{PHL} and t_{PLH} marked. A small video inset shows a man speaking.

To begin with one of the performance metric which we would like to discuss now is called propagation delay. Propagation delay occurs because of two reasons; one is finite switching speed associated with the transistor. So, transistor from off to on or on to off in that - generally there is a redistribution of charge in the transistor junctions we know that npn transistors there are two junctions base emitter and base collector junctions.

And this re-distribution of charges take finite time it is not happen happens it does not happen instantaneously. So, this is one reason. And the other important reason is there are circuit capacitances which cannot be ignored. Even if it is not explicitly connected between any metal junction and the ground there is a circuit capacitance. Important over here is the circuit capacitance if we look at, if you remember the previous transistor inverse inverter circuit - ok.

So, we are taking this is your V_{in} and this is your V_{out} - ok. So, though we have not explicitly mentioned there is a presence of capacitance, but there is a load capacitance which is present. And, the more the number of load, the more the number of other transistors you connect, more is this value because, those all - these capacitances come in parallel. And this transistor, this capacitance needs to get charged through this path - ok.

So, there is a RC, this RC - this is RC and this is R_B . So, there is a time constant associated for pulling up the value over here. Discharging takes place when this transistor is on. So, that path resistance is less so, it is relatively quicker. And this is visible when you see this

particular diagram. So, this is your one this is your input and in the input side you can see that the input does not, is not possible to change instantaneously though you are saying from low to high there is a finite time, time - again because of the electrical parameter circuit parameters that are associated with the input side of the circuit.

So, this is the 50 percent time that is considered as the one by which it has got sufficiently, you know, become low to high. And the other side if it is - since it is an inverter reaction, when it is following from high to low - the 50 percent time; 50 percent of the magnitude when it - when it happens that is the time between output going from high to low - ok. So, this is the time difference that we see over here - ok.

So, this is time propagation delay output going from high to low, corresponding time propagation delay when output goes from low to high, and you can see that this low to high is relatively higher. One of the reason, as I said is the switching speed the transistor when goes from off to on the charge distribution does not take - that aspect of it, does not take much time, but when it goes from on to off - ok. So, at that time the charges that are there that need to be taken out - so that the deeper into the saturation we want to work it in the saturation mode; so, deeper into the saturation - more is the time required to bring back the transistor from on state to off state - ok. So, for which this delay is more, and if you talk about one entity then it is an average of this two which is the propagation delay. Toward that time parameter that are important here one is rise time another is a fall time.

$$t_{PD} = (t_{PHL} + t_{PLH})/2$$

Rise time is the value from 10 percent, this is 10 percent to 90 percent whatever time it requires. So, that is the rise time and fall time is 90 percent to 10 percent whatever time is required that is your fall time. So, this is your t_{fall} and this is your t_{rise} - ok. So, these are two important parameters associated with so, we shall take note of this.

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Power dissipation

- **Static power dissipation**
 - when transistor is either ON or OFF
 - depends on current drawn in each case
 - power dissipation, P_D is average of these two
 - significant in switching of Bipolar Junction Transistor
- **Dynamic power dissipation**
 - when transistor switches
 - depends on switching speed
 - significant in switching of CMOS Transistor

Figure of Merit,
 $F = P_D \times t_{PD}$
 The lower the F, the better.

The slide also features a video feed of a man in a maroon shirt in the bottom right corner and logos for institutions like SVKM's Deemed to be University and others in the bottom left.

Next important parameter is power dissipation-ok. Power is an important issue - reason being, these transistors or the gates will not work in isolation. There will be large numbers of them and modern integrated circuits have million of millions of them. So, though individual gate, individual transistor or gate power dissipation may be less, but collectively there might be very, very large power dissipation. So, this is an important quantity.

So, there are two kinds of power dissipation; one is static power dissipation, another is dynamic power dissipation. Static power dissipation - when the transistor is in one of its stable state - on or off. So, at that time whatever current is flowing from the power supply we know, the voltage into current is the power that is dissipated.

And total power will be average of these two and in all our calculation we usually consider that the time-on during which it remains at on state and time during which it remains at off state, off state - they are equal - ok. So, that is the way we calculate this thing and the average power - ok. And dynamic power dissipation occurs when the transistor switches, when the transistor switches so, that time during the switching whatever power dissipation occurs. So, this might not be a very clear at this point of time given the example we have seen before - that the simple transistor inverter. This will be clearer when we take up more examples with TTL and CMOS circuits - CMOS logic gates which we shall discuss little later.

So, right now, we more or less understand this part - the static power dissipation part of it. And one more important aspect here - the transistor power dissipation can be reduced by

reducing the amount of current. And that can be done by increasing the value of the resistances, resistances without making much of a changes elsewhere in the circuits. So, if you increase the value of the resistances current reduces, but what is the effect in other parameter - one important parameter that is propagation delay, the time constant will increase. So, accordingly propagation delay will increase. So, it has been seen that to a great extent within the operating condition that can be accommodated, the power dissipation and propagation delay this product more or less remain same - ok. So, if you reduce power by increasing resistance values, propagation delay increases and vice versa. So, this is called one figure of merit of course, if it is lower, the better. So, this is something that we take note of.

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RTL NOR Gate
RTL: Resistance Transistor Logic

- For 3 input NOR gate, another input would come in parallel with A and B.
- More no. of inputs increases delay
- Fan-in: Max. number of inputs a gate can handle

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Now, the circuit that we had seen before that was just an inverter – isn't it? So, when you talk about logic gates there are many different kinds of logic gates that are possible. So, using that particular circuit as the base, one simple element, can we develop other gates? So, let us look at one particular circuit over here.

So, two such inverters except the collector resistance part - they are in parallel – ok. And this if we look at, if you compare what we had seen before - so, this is your R_B , this is your R_B in earlier circuit and this is your R_C so - that made parallel to one another. Now, how does this circuit work in terms of in a logic value? So, any one of them low what happens - and the corresponding - the other one is, say low or high. So, this is a low, this is low or

high what is happening? So, if this is low and the other one is also low ok, so none of this transistor conducts - then, none of the transistor is on.

So, at that time what will be happen to the output voltage output voltage since there is no current flowing here accept the whatever small load current will be there. So, it will be V_{CC} minus that drop so, output will be considered as high. But, this is low and this is high what happens at that time? This is conducting. So, this is 0.2 volt or so, the saturation voltage so, output is treated as low. Now, we look at the other case. So, this is - these are the two cases that we have seen, this one is at high - ok. So, this voltage - this transistor is on - right. So, this voltage stands at 0.2 volt - this is getting a path. So, even if this transistor is off or on does not matter - the output voltage will be kept at 0.2 volt - ok.

So, this is what we see over here for these two cases. Effectively, if you look at the whole of it these output is low for any of the circuit any of the input being high. And, output is high only when both of them are low, both of the transistors are off. So, that is NOR logic that we see and this can be extended - this is now two; three-four to the extent it is possible, and that defines the fan-in - how many inputs can be connected to a particular gate - ok. So, that is another term that we can define over here - that is called fan-in.

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RTL NAND Gate

It will be shown that any other logic gates can be obtained using only NAND gate or NOR gate.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Now, let us look at this circuit, how does the circuit work. Earlier what we had seen - the transistors, the input, inverters were in parallel. Now, what you see over here they are in series - ok? So, when they are in series what happens - any one of them is low; that means,

the path through this transistor - that particular transistor is off; either this one is off or this one is off so; that means, the path to the ground is blocked - right. So, either this one is blocked or this one is blocked or both of them are blocked - right. So, the path is not available. So, what will happen - this voltage minus whatever the load current related drop over here, will be available here so, this is effectively a high voltage, high condition.

And only when, only when both of them are on - a path to the ground; a low resistance path to the ground exists - ok. So, the drop will be 0.2 and 0.2, 0.4 volt or so - right. They are in saturation - which is still considered as logic low, is it fine? So, this kind of circuit behaves like NAND - if you look at the truth table any one of them is low output is high; all of them high, output is low. And, later on we shall see that using NAND gate and NOR gate any other gate we can develop, we can also look at that part, but we shall see later.

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From Archive (Motorola datasheet)

DUAL 3-INPUT GATES PLASTIC MRTL MC700P/800P series
MC715P • MC815P

Two 3-input NOR gates
 $R1 = 450\Omega$, $R2 = 640\Omega$
 $P_D = 55\text{ mW (input H)}, 15\text{ mW (input L)}$
 $t_{PD} = 12\text{ ns}$

The MRTL family of resistor-transistor logic offers the industry's broadest line of digital circuits. Devices in this section are medium-power circuits; low-power mW MRTL circuits are also available.

The slide features a circuit diagram of a 3-input NOR gate with pins 03, 04, 02, 01, 05, 06, 07, 08, 09, 10, 11, and 12. It includes a Vcc pin (11) and a GND pin (04). The circuit uses resistors R1 and R2, and transistors. A small inset photo of a man is visible in the bottom right corner of the slide.

Now, though we said that we will be discussing more of the TTL and CMOS logic gate later, but whatever we have discussed so far, I mean, were there any such practical IC's available at any given time? Yes, long back - 1960's we had these ICs in existence and this is one example that I have taken up from Motorola data sheet that is available as archive. So, what you see over here - it is straightaway taken from the data sheet - one page of it, part of a page. So, what do you see over here is a RTL this is called Resistance Transistor Logic, because of the presence of the resistance and transistor - this IC was available at that time. And this particular IC, these are the different pins that you can see

these pin numbers are there. And this was two 3-input NOR gates. Within the IC, there were two such NOR gates and each one of them was having 3 inputs - ok.

So, this was available at that time. And, for our example case - we used you know, for simplifying the calculation we took R_B is equal to 10 kilo ohm and R_C was 1 kilo ohm and we calculated that the transition width can be reduced if we increase the value of R_C compared to R_B because their slope was minus R_C by R_B those things were there. So, here what we see in practical circuit that they came up with as the IC - R_1 was used as, R_1 is related to your R_B , 450 ohm, and R_C which is R_2 here is 640 ohm - that was a practical circuit that was used at that time. And power dissipation was when input was high input was high means transistor was on. So, current is flowing through R_C through the transistor to the ground, 55 milliwatt. And when it was off for the kind of standard loading it was 15 milliwatt and, propagation delay was 12 nanosecond. So, that is what the data sheet provided at that time.

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DTL NAND Gate
DTL: Diode Transistor Logic

V_{CC}

R_1 R_2 R_3

A B Y

D_1 D_2 D_3 D_4

$V_p = 3 \times 0.7V$ turns ON transistor.)

R_3 provides discharge path of stored charge at BE junction that reduces t_{PLH} .

Any of A or B low (0.2 V), $V_p = 0.9$ V, insufficient to turn ON the transistor.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Now, to go to transistor-transistor logic, let us have a look at something that was intermediate. This was called diode-transistor logic it does not mean that resistance was not used, but just to keep, you know, this thing later. So, earlier was resistance transistor logic, this is diode transistor logic. So, transistor remains because that only provides the inverter action not action and regarding use of diode we have already seen diode as a switch in our first class, if you remember lecture 1.

So, there we had seen this diode resistance combination - right. So, between this two input A and B and this Y what was the relationship any of the input is low - output is low, because current is going in this direction. Only when both of them are high the voltage is available here that is no current is flowing all right and at that time the output was high. So, this was effectively AND logic - right. So, you see over here in the diode transistor logic in the first stage, you have got this particular block this particular block this particular block, which is providing you the and logic - ok.

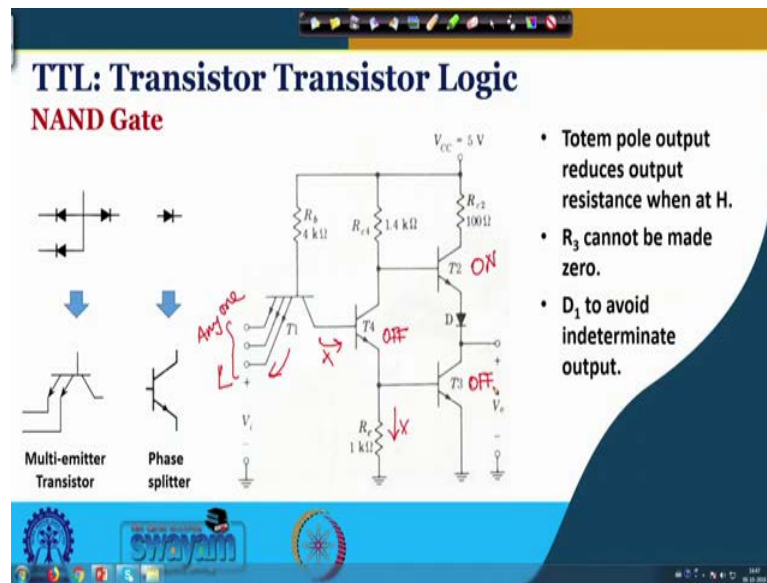
And after that there are two diodes what are they doing they are just doing the job of level shifting - ok. So, how this level shifting is useful the level shifting is useful because, earlier what we had seen? We had seen that the transistor turns on when base emitter drop is 0.7 volt.

Now, if you put another diode before that so, you need two diode drops 0.7 and 0.7. So, then it will only you know turn on so, that is known as level shifting - ok. So, there are these two diodes that are present which are level shifters - right. Now, this diode conducts current only in this direction. So, in this base emitter junction wants to come out of the saturation so, the charge need to go back to the ground for that, since diode does not allow that path. So, there is this resistance is there which is providing a path for the charge to get redistributed when the transistor comes out of on state to off state.

So, this is how it is there and to turn this transistor on what is required? 0.7 volt, 0.7 volt and 0.7 volt so, 2.1 volt will be required over here then only it will be able to turn on. So, any of this low so, the voltage over here is available is low means similar circuit you know connected before something like this. So, low means 0.2 volt or so, over here. So, 0.2 and a diode drop there; so, 0.7, so 0.9 volt is available here which is not sufficient to turn this on. So, any one of them low - output, this transistor is off output will be high and when both of them are high then only the transistor is on and the output is low. So, that is what kind of logic is that this is NAND logic so, that is why we called it DTL NAND gate - ok.

Now, we shall get introduced to what we said earlier that TTL NAND logic - ok.

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So, we remember the DTL circuit - just in the previous slide we had seen. So, this input block what do you see over here - there are two diodes, and there are three diode combination and in TTL this is replaced with a transistor which is something like this. This two diodes refer to two multi-emitter two emitters in a multi-emitter transistor; this diode refers to the base-collector junction over here; this is the base-emitter junction, these two correspond to and this is the block which is coming in place of the one that we had seen in the DTL case - ok.

So, there was a diode over here one level shifter. So, that level shifter the second one that we had seen. So, this level shifter is present here as a transistor. So, this base-emitter junction is providing the diode kind of you know drop that is required - clear. So, with these two changes in the previous circuit, these two changes; so, this is changed, this is replaced by a multi-emitter transistor. And this is replaced by another transistor - we go to the circuit that is over there. I shall talk about this little later - what is the significance of this - ok.

So, this particular transistor which is now coming in this particular place, it has got another name called phase splitter - ok. So, how does it work - let us see. Then it will be clear why it is called phase splitter. Now, when any of this input, multi-emitter input is low, what is happening - it is happening similar to what was happening in the case of DTL. So, the transistor, the current will be going in this direction - right. So, current is not driven towards this transistor which is numbered as T4. So, this transistor is off, so, this transistor

is off right so, in this transistor is off; that means, I am talking about any of them is low any of them is low - ok.

So, the current is going in this direction not much current in the other direction so, this is off. So, when this is off, no current is flowing in this direction right, when no current is flowing in this direction, no sufficient I into R_e drop to turn on this base emitter junction this transistor T3. So, T3 is also off - is it clear? Right. When any one of them are low any one low - ok. So, this is off, this is off and when both off all right - current is not going in this direction. What is happening to this voltage? This voltage will be V_{CC} , 5 volt minus whatever current flowing through it as base current over here - considering some load is connected.

So, that is a base current so, relatively small current will be there - ok. So, that drop will be very small so, that way this voltage over here will be sufficiently high - ok. So, this voltage will be sufficiently high. So, that sufficiently high voltage will do what - will make this transistor on - ok. So, this transistor will be on at that time. Why the diode is required, that part we will come later. So, right now we consider that this transistor will be on at that time and if a load is connected here. So, load will get current from this path, this path through this on transistor - is it clear? So, any one of them low this is what is happening. Now, let us look at the other case when all of them are high - all the inputs are high.

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TTL: Transistor Transistor Logic
NAND Gate

Multi-emitter Transistor
Phase splitter

$V_{CC} = 5V$

$R_{B1} = 4k\Omega$
 $R_{E1} = 1.4k\Omega$
 $R_{B2} = 100\Omega$
 $R_{E2} = 1k\Omega$

V_1
 V_2

- Totem pole output reduces output resistance when at H.
- R_3 cannot be made zero.
- D_1 to avoid indeterminate output.

Handwritten notes: All HIGH, ON SAT., OFF, ON $V_{ce} = V_{cc}$

What is happening at that time? So, the current is driven towards - some current is driven towards this direction - right. So, this get sufficient base current for which this transistor becomes on this transistor becomes on - so much on that it is goes into actually saturation that part we shall see later - ok. So, then the current flowing through this transistor is so much all right minus the base current over here that gives you sufficient drop across this to make this voltage greater than the V_{BE} on greater than. So, this transistor is also on again this transistor is also on so much so that it also goes to saturation.

So, what is the voltage then available over here? So, this is saturation 0.2 volt and this is saturation 0.2 volt 0.1 volt and of that range and this is saturation 0.7 volt. So, about 0.9, 0.95 volt is available over here - ok. So, let us consider say, 0.95 by volt on the higher side - ok.

Now, with this particular voltage, this transistor – right, here it is 0.2 volt because this is in saturation. So, if this diode was not there 0.95 and 0.2 this voltage would have been sufficient to make this transistor on and go to saturation – ok.

So, this is what is prevented by placing the diode over here. So, you require actually two diode drops; that means, about 1.4 volt or so, to make them on. So, at that time what is happening this transistor is actually off, because of the presence of the diode - ok. So, that is the importance of having the diode over here - ok. So, these are the other cases, this is the other case - when all of them are high all high output low; anyone low output high. What is that logic? That is nothing but the NAND logic. So, this is what - how this particular circuit works. Now, one important thing over here.

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TTL: Transistor Transistor Logic

NAND Gate

- Totem pole output reduces output resistance when at H.
- R_3 cannot be made zero.
- D_1 to avoid indeterminate output.

Multi-emitter Transistor Phase splitter

Active pull-up

$V_{CC} = 5V$

$R_1 = 4k\Omega$ $R_{e1} = 1.4k\Omega$ $R_{e2} = 100\Omega$

$R_2 = 1k\Omega$

V_i

V_o

C_1

Earlier, you we had seen the charging of the output capacitor was through a passive resistance – right. Now because of the presence of this transistor. Now, what is happening - it is known as active pull up which effectively reduces the resistance of the output circuit, output impedance below 100 ohm which is of the, I mean, almost 10 times less then what would have been the case if this was not present. So, that is why the charging time of this capacitor decreases - discharging is through this path. So, that is small, because of this as a very low resistance path - ok. So, effectively this helps in switching, reducing the propagation delay. So, that is another important aspect of this and the whole of it, the one that you see this structure is known as totem pole output.

So, this is like one physical structure if you see that. So, totem pole is something like this ok. So, that kind of it is - that is the similarity. So, that is why it is called totem pole output and this has got it is own advantage of charging and discharging a bit faster. So, we shall discuss more about this TTL circuit, how it works in the next class.

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Conclusion:

- Propagation delay, power dissipation and their product, defined as figure of merit, are important to characterize a logic gate.
- RTL NOR gate is formed of parallel connection of transistors acting as switches akin to NOR logic formed of electrical switches. Similarly, RTL NAND gate is formed of series connection of transistors.
- DTL NAND gate uses diode AND logic, level shifter diode and transistor inverter.
- TTL NAND gate uses transistor at the input stage, for level shifting and phase splitting, and also totem pole output to improve switching speed.

swayam
MOE, GOVT OF INDIA

And, just to summarize what we had seen today is the propagation delay power dissipation. And their product figure of merit; their importance. RTL NOR gate getting formed by parallel connection of transistors the kind of thing we have seen using electrical switches we are getting NOR logic, we got NOR logic that we discussed in the 1st class - lecture 1.

And similarly, we got NAND logic by placing the transistors in series - ok. And we had discussed that fan-in is you how many say, it you if you are putting it in input - how many such gates can be - so, the maximum of that is called fan-in that is another important parameter for this logic gates - ok. So, in the DTL NAND gate, we have seen the diode and AND logic was there in the first stage after that there was level shifters. And, then there was transistor in inverter.

And in the TTL NAND gates we found that in the input stage that diode AND logic has been removed with a multi emitter transistor. And the level shifting diode has been removed using a phase splitter phase splitter is called because the collector and the emitter of that phase splitter transistor - they are always out of phase - ok. When one is high another is low making one of the totem pole, one of the transistor in the totem pole output on - another is off; both of them are not on simultaneously except during switching; except during switching. That we shall discuss more later, and this totem pole output improves switching speed.

Thank you.