Digital Electronic Circuits
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Lecture – 02
Transistor as a Switch

Hello everybody, we move to lecture 2 of this particular course. In lecture 1, that is in the previous lecture, we had seen why digital technology is important, what constitutes digital technology, the importance of switching, association of switching with logic relation and use of diode as a switch. So, this is what we had seen earlier. And in that discussion we had seen that diode as a switch can be used for developing AND and OR logic - ok. We left ourselves with a question that whether you can get an inverter logic or NOT logic using diode which we found that from our common understanding it is not possible, but transistors can be used for generating NOT logic or inverter - ok.

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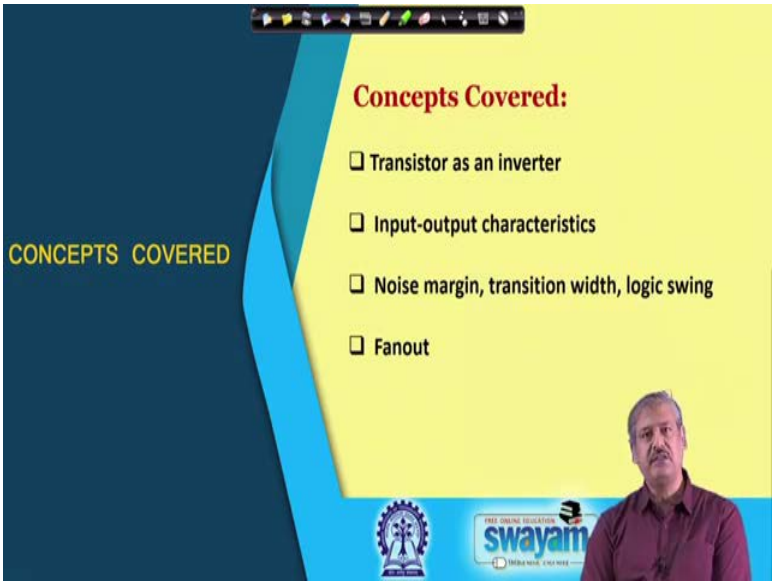

So, in today's lecture we shall cover Transistor as a switch. So, we shall look at its input output characteristics and some important parameters like noise margin, transition width, logic swing and fanout.

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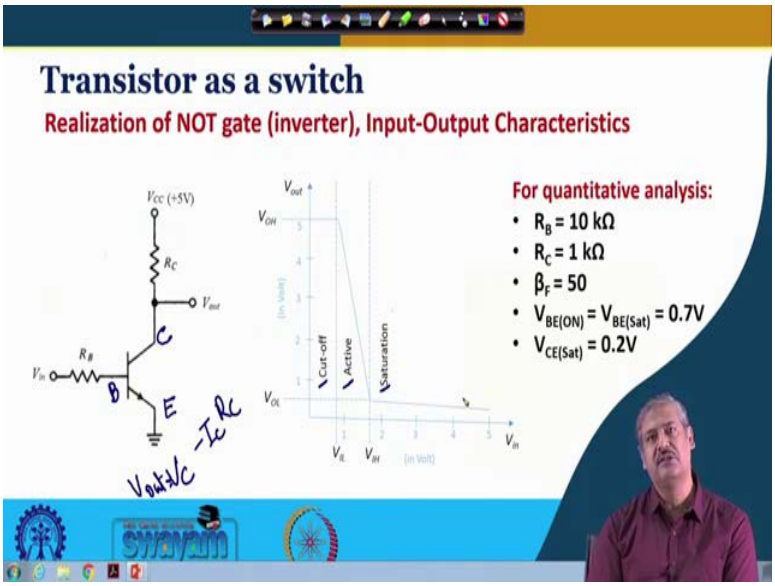

So, we start with a basic circuit of a very simple circuit of transistor based inverters. So, what we see in the left hand side of the slide is a circuit where we see this is an NPN transistor bipolar junction transistor, this is the base, this is the collector and this is the emitter - ok. So, this collector is connected through this R_C to power supply, the V_{CC} a positive power supply, we considered 5 volt here. And, the base is connected to an input voltage V_{in} through a resistance which is R_B, this resistance R_B; this is collector resistance R_C - ok.

And output is taken from collector C - right. So, this is the basic configuration which we shall examine. Now if you look at this circuit and we try to plot V_{in} versus V_{out}, V_{in} versus V_{out} - ok. So, this side this x axis is V_{in}, independent variable along the x axis; y axis is the dependent variable V_{out}. So, how this circuit will work right in the beginning when V_{in} is 0 ok. So, the transistor is in off state. So, at that time what will be the output? See this transistor - this transistor is off, no current is, no I_C current is flowing, no collector current is flowing.

So, collector current: that I_C into R_C this drop V_{CC} minus I_CR_C that is your V_{out}, this is your V_{out} - ok.

$$V_{out} = V_{CC} - I_CR_C$$

So, since I_C is equal to 0 so, the voltage that you get here is the V_{CC} which is about 5 volt over here - right. So, how long it continues? It continues up to a maximum voltage, up to a maximum voltage, when this base emitter junction becomes sufficiently forward biased; so, that this starts conducting - ok, this transistor starts conducting. So, that maximum voltage that maximum voltage we define here in general as V_{IL}; that means, the voltage at the input side which is considered low. The maximum of the input voltage at the input side which is considered as low, any voltage less than that - what will it be, how will it be considered?

It will be considered as low, logic low only because at that time you see the output is remaining at high voltage which is an inverter action, I mean, the first part of the inverter action, we shall see the other part also when input is high whether the output is low or not ok. So, input is considered low up to a maximum point V_{IL}, is it clear? So, after that the transistor starts conducting. So, this from cut-off region transistor enters into next region. What is that? Active region - right and when the transistor starts conducting I_C is getting increased, what will happen? This voltage, this V_{out} will slowly come down. We shall see later for this particular arrangement under certain approximation this fall is approximately linear, that relationship we shall soon see.

So, this is now the current is increasing, the voltage is getting increased. So, I_B is increasing accordingly I_C increasing, βI_B is the current, I_C value the in the active region. And, this will continue till it enters the next stage what is known as saturation – right, what is known as saturation, when both base collector and base emitter junctions are forward biased - ok. So, at this point what is the voltage here? It is approximately some 0.2, 0.1 volt or whatever, depending on the transistor that you are using - ok. So, that is the maximum voltage at the, sorry, that is the minimum voltage at the input side which is to be present after which the transistor will enter, move into saturation - ok. Any voltage higher than that in the input side, it will move into saturation, is it clear? Let me repeat once more.

So, from V_{IL} when the transistor starts conducting which is in the active region, gradually with increase in V_{in} this current increases corresponding collector current increases V_{out} starts falling, it continues up to a level which is known as - when it enters the saturation. So, after that any increase in the voltage, after that any increase in the voltage V_{in} the transistor remains in saturation, we put that it comes out of the situation is it clear. So, you we tell that particular voltage as V_{IH} - V_{IH} - ok. So, what happens at that voltage? At that

voltage we know formally that the output is in saturation and the voltage is here about 0.2, 0.1 volt also which is considered as low at the output level, low at the output level.

So, any voltage higher than that will be considered as, at the input side, will necessarily make the output low - ok. So, otherwise speaking what is the significance of V_{IH}? V_{IH} is the minimum voltage required at the input side which is treated as logic high - any voltage higher than that at the input side will be treated as logic high ok, is it clear? So, you see the relationship the inverter relation, inversion relationship input is low over here ok, output is high, input is high, output is low - right. And, we will see there are two other voltages this is the V_{OL} that is the voltage at the output side which is treated as low any voltage less than that will be treated as low.

Then V_{OH} is the voltage at the output side which is stated as high any voltage higher than that also will be treated as high. This is in general we see a characteristic of an inverter which is also a kind of getting - there is correspondence between this transistor input-output characteristics, is it clear? So, we would like to do some sort of, you know, quantitative analysis and we shall keep it very simple for our understanding of the way the logic circuit or digital circuit works and we shall keep say, R_B 10 kilo ohm ok. So, 10 all 0s are there; so, it will help - R_C 1 kilo ohm, beta - transistorβ, the current gain as 50, β_F stands for beta forward, β_R is beta - reverse beta that we shall take up later.

This $V_{BE(ON)}$ when the transistor is ON we shall consider the voltage at which it becomes ON is remains on is 0.7 volt and when it goes to saturation there is a small increase in this voltage, but again as I said this is an approximate analysis; we shall keep it at 0.7 volt only - ok. But, actually there will be small increase in this voltage when it goes to saturation and V_{CE} saturation, we'll consider as 0.2 volt which again as V_{in} increases falls little bit - ok. So, this is what we are going to do.

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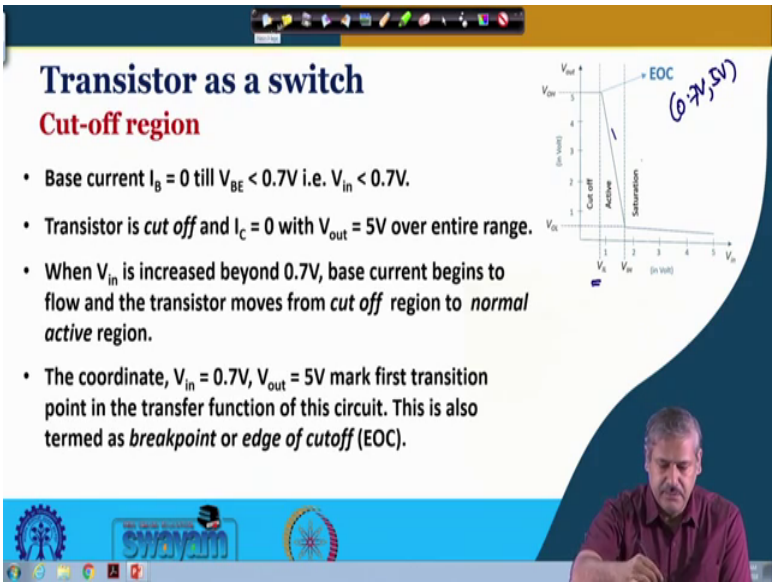

Right! So, with this let us, let us look at that characteristics ok. So, the first thing that we shall try to get is what at which voltage, at which voltage this fall starts occurring - right. And, as we know, in this particular case, it is very simple, this V_{IL} in this case is nothing but voltage when it comes out of cut off region and enters the active region. And, it occurs based on whatever values we have already taken, occurs at 0.7 volt - right. So, the coordinate of this is 0.7 volt and 5 volt 0.7 volt and 5 volt - ok. This is this coordinate that we see for the analysis that we are making. And, this is also known as edge of cut off, edge of cut off. That means, at this point it is just coming out of cut off - is it clear?

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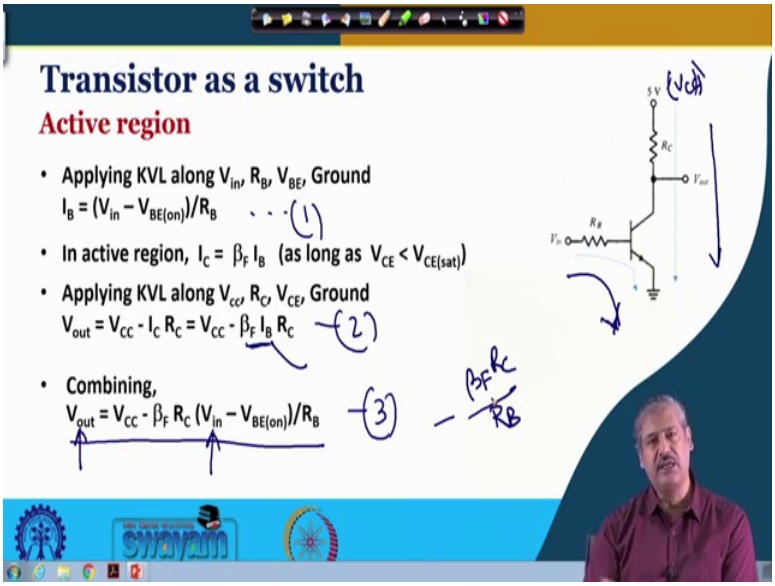

Next, we shall see what happens when it enters into active region - ok. So, when it enters into active region current flows along this loop 2 loops that you can see over here, one is along this loop, another is along this loop - right. So, we shall look at we shall apply Kirchhoff's voltage law along this loop and from that we shall do a quantitative analysis right. So, when we apply along this particular loop, this particular loop, what we see for this voltage - I_B will be V_{in} minus $V_{BE(on)}$ the voltage drop over here divided by R_B - right.

$$I_B = (V_{in} - V_{BE(on)})/R_B$$

From that, we can see the current through this, I_B is V_{in} minus $V_{BE(ON)}$ that is the rest of the drop is over R_B divided by R_B is what is your I_B, is it clear?

Now, in active region we know I_C is equal to $\beta_F I_B$ and in active - this is the other loop along which we are applying KVL.

$$I_C = \beta_F I_B$$

So, this is 5 volt that is the V_{CC} that we have already mentioned. So, this is generally speaking - we write it as V_{CC} because we can change it to some other voltage - other than 5 volt, if so required. For generalization purpose, we write this as V_{CC} - ok. So, V_{out} is nothing, but V_{CC} minus $I_C R_C$ and this I_C is nothing but your $\beta_F I_B$ - we will replace it with this one.

$$V_{out} = V_{CC} - I_C R_C = V_{CC} - \beta_F I_B R_C$$

Now, this I_B - this was your equation 1 and this is your equation 2; so if you take the I_B from equation 1 and combine and place it here. So, this is the thing - that this is the relationship that you get, is it ok? So, V_{out} is equal to V_{CC} minus $\beta_F I_B R_C$. So, R_C is there - I_B is nothing, but your V_{in} minus $V_{BE(ON)}$ divided by R_B, is it fine? So, as long as it is remaining in active region this is the relationship it will follow and we look at V_{out} versus V_{in} - rest of all are constant. There is $V_{BE(ON)}$ - will slightly change with increase in V_{in}. So, we are neglecting that part - it is an approximate calculation - right! So, rest of them - all the parameters are constant. So, we have V_{out} and V_{in} relationship between them is linear - straight line - ok.

$$V_{out} = V_{CC} - \beta_F R_C (V_{in} - V_{BE(on)})/R_B$$

Straight line with a negative slope of what minus $\beta_F R_C$ by R_B - is it fine? So, if we want a faster fall – right, we want more of, more often the circuit remains in one of the two stable switched states that is logic low or logic high. Then we would like to have this transition region; this active region which is also known as transition region, that width, as small as possible - ok. So, we would like to have a faster fall. So, in that case we would like to have a R_C mode compared to R_B. We shall - we would like to have increase in R, but - again we shall see later, if we increase R_C then the circuits current delivery capacity - the I_C part of it gets reduced which actually makes it difficult for the circuit to get connected to many other circuits that particular thing also, we shall see today - ok. So, there is always, when you talk about design, there is always trade-off, ok. But, this is what we take from this particular discussion - is that there is a linear relationship and the slope is negative for the circuit in the active region - ok.

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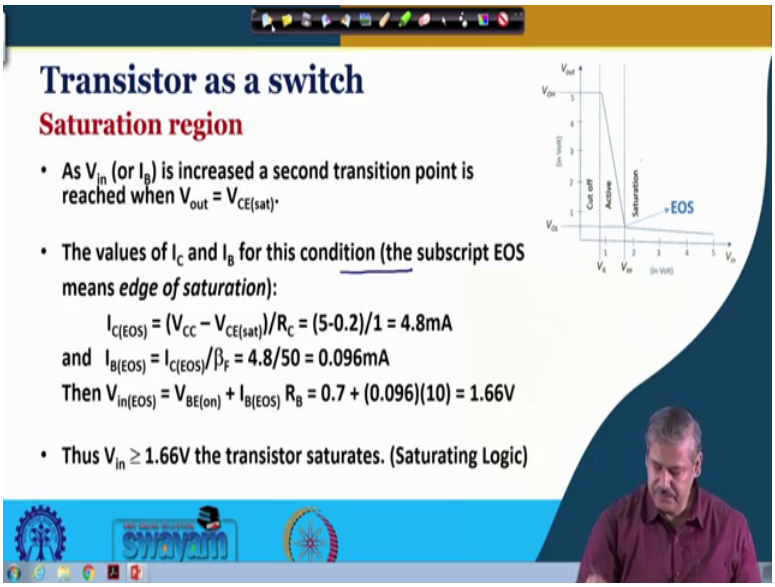

Now, next is saturation region - right. So, in this saturation region again we would be interested to see when it enters saturation - ok. As long as it is remaining in the active region, it is falling linearly with the negative slope – that, that part we have already seen that is what we have already noted in the previous slide - ok. So, when this particular point, this we define as edge of saturation, when it just enters the edge of saturation which considers that it is still following the previous equation. After that it goes into saturation region - it is no longer that linear relationship, that will be maintaining.

So, at edge of saturation, it is still maintaining - right. So, at that time this V_{out} when it just enters the edge of saturation, at it, is at the edge of saturation is V_{CE} saturation - right. So, at that time the current I_C we define with a suffix edge of saturation when it is just entering here is V_{CC} minus V_{out} is now $V_{CE(Sat.)}$ divided by R_C. So, that is 5 - 5 volt we have considered as V_{CC} minus 0.2 volt divided by R_C - R_C is equal to 1 kilo ohm - that is 4.8 milli ampere - ok. If we increase the R_C the current will reduce which is - which we'll have a look later in some other cases. So, we cannot you know just change it the way we like you have to look at other considerations in situation like this.

$$V_{out} = V_{CE(sat)}$$

$$I_{C(EOS)} = (V_{CC} - V_{CE(sat)})/R_C = (5\text{-}0.2)/1 = 4.8\text{mA}$$

$$I_{B(EOS)} = I_{C(EOS)}/\beta_F = 4.8/50 = 0.096\text{mA}$$

$$V_{in(EOS)} = V_{BE(on)} + I_{B(EOS)}\, R_B = 0.7 + (0.096)(10) = 1.66\text{V}$$

So, this is edge of saturation I_C - right. So, edge of saturation I_B is what this $I_{C(EOS)}$ - I_C edge of saturation divided by β- because, it is still in active region it just entering the saturation region. So, 4.8 divided by beta forward which is 50 - 0.096 milli ampere, simple calculation right. So, at that time what is the V_{in} –right. You refer back to that equation 1 that we had before. So, V_{in} is equal to $V_{BE(ON)}$ – right, the base emitter drop and I_BR_B drop. So, I_B edge of saturation in to R_B in the KVL in the base emitter junction - that particular loop - right. So, in this loop, this is the loop, in this loop. Sorry. So, this is the loop that I am talking about - ok.

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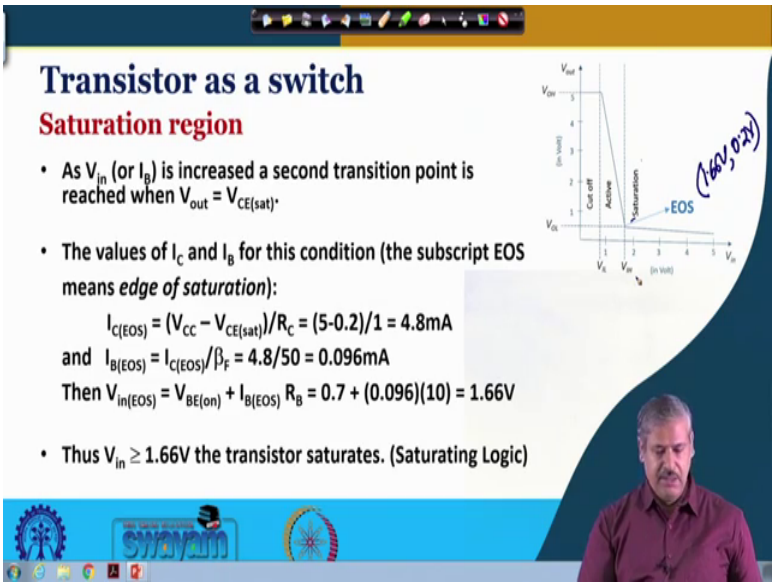

So, we in this particular loop when we impose these values – right, we have 0.7 volt, I_B edge of saturation 0.096 and R_B we have taken as 10 kilo ohm so, 1.66 volt - ok. So, thereby, we get this particular point also edge of saturation, which is also important to us and this coordinate is 1.66 volt and 0.2 volt. Is it fine? Ok. So, any voltage greater than 1.66 volt at the input, at V_{in} definitely the circuit is in the saturation - right. So, that is the significance of V_{IH} I was trying to tell, that this is the minimum voltage required at the input side which can be treated as logic high which you ensure for the inverter that the output is - output remains at logic low – clear? Right.

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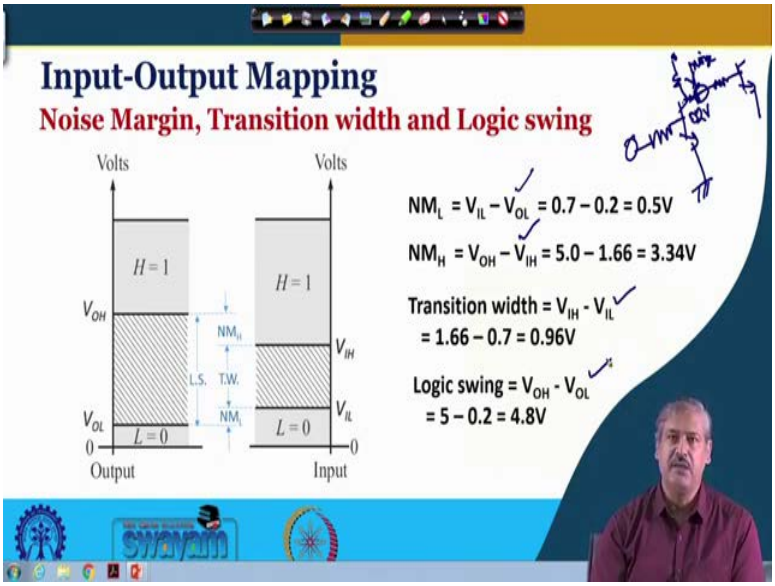

Now, we come to some important parameters - noise margin, transition width and logic swing - ok. Transition width - we have already seen, but again more formally we shall introduce ourselves to these terms over here - ok. So, in the left hand side what you see is a generalized representation, not specific to the example that we have taken. We have taken the example to make a better understanding of these different terms. And all using a simple transistor inverter, actual circuit will be more complex - which we shall take up later - right. So, this is the output side - ok.

So, V_{OL} we have already seen, the voltage at the output which is treated as low. Any voltage less than that will be treated as low, in that example 0.2 volt. Any voltage less than that treated as logical low, this is the shaded region over here ok: V_{OH} voltage at the output side, minimum voltage which is treated as logic high; any voltage above that will be treated as logic high. So, it was 5 volt there and any voltage more than that 5 volt will be treated as logic high without any ambiguity – clear! And, then the logic swing - this is defined as logic swing - is the difference between V_{OH} and V_{OL} - ok.

Now, if you look at the input side; what is happening? This V_{IL} as you have already seen in that particular example, but it is true for every other cases for inverter like this, that from 0 to V_{IL} this is treated as logic low. Any voltage, even less than 0 also, because of noise and other things, if it is less than V_{IL}, as long as it is less than V_{IL} - it is treated as logic low, the input is treated as logic low - right. And, at the input, at the input side any voltage greater than V_{IH} will be treated as logic high - ok. In that example it was 1.66 volt, any voltage more than that it will be treated as logic high; the output will be low at that time - right.

So, the difference between V_{IL} and V_{IH} - the time, the phase or the duration, if we are continuously increasing the V_{in}, input voltage that is being in your transition width; the active region in which where it is staying - ok. So, after understanding these terms once more now, we define noise margin high, no - noise margin low as V_{IL} minus V_{OL}. What is the significance of it? The significance of this is this that up to V_{IL} we are treating in this as logic low. Here if this inverter is connected to another inverter, another similar device to the next stage. So, when it is at logic low, what is the voltage it is offering? 0.2 volt or less, maximum voltage is 0.2 volt - ok.

Now, imagine some noise gets into - gets corrupted by additive noise - right. So, the 0 if it is a 0.1 volt and 0.1 volt noise so, the voltage at the output will be 0.2 volt ok. So, what I mean over here let me draw a diagram which may make it clear to you. So, I am talking about this is being connected to another device another such inverter or other gates right. So, here it is 0.2 volt maximum I mean when it is treated as logic low, it can be less than that, but let us consider the limiting case - ok. And, then noise gets added say, at additive noise and is getting added over here, so this is noise right. So, how much noise you can allow so that this low is treated as low here. The maximum voltage that can treat as low is 0.7 volt - ok.

This is maximum at the output when it is logic low is 0.2 volt, it can be less than that. So, what is the difference? The difference is the maximum voltage that can be accepted as noise which is added as with positive polarity - if it is negative value – say, 0.2 volt and noise is minus 0.1 volt then there is no issue - ok. But, noise with positive polarity if it comes noise it then this is the thing that we are need to remember, is it clear? So, that a 0.5 volt margin is there with me. So, this is noise margin low generally speaking for any such situation where V_{IL} and V_{OL}, V_{OH} are defined this is the difference - is the noise margin.

$$NM_L = V_{IL} - V_{OL} = 0.7 - 0.2 = 0.5V$$

$$NM_H = V_{OH} - V_{IH} = 5.0 - 1.66 = 3.34V$$

In this specific example that we have taken from which we are trying to understand this terms - it is 0.7 minus 0.2 volt which is 0.5 volt - ok. So, similar thing is noise margin high: So, when the output is at logic high say V_{OH} - right and at the input it has to be treated as logic high - right. So, what is the - now if noise gets added, but if it is positive polarity it will be V_{OH} plus some value - then there is no issue. This we are in this region, but if it is negative polarity! Now, the polarity of noise if so negative, if negative, then we are in a bit of concern. So, this V_{OH} can come down, it comes down and crosses V_{OH} then we are in a problem; the input will not be treated as high - ok.

So, this V_{OH} minus V_{IH} is the noise the margin of noise that - it can accommodate. So, accordingly, these two terms are defined and in this specific example that we have taken it is 5 volt minus 1.66 volt which is 3.34 volt. So, transition width of course, is the difference between this V_{IH} and V_{IL} and logic swing (is V_{OH} and V_{OL}). So, these definitions

that you see these are general, irrespective of the example we have taken. And this is applied to any logic family and the corresponding gates - ok.

$$\text{Transition width} = V_{IH} - V_{IL} = 1.66 - 0.7 = 0.96V$$

$$\text{Logic swing} = V_{OH} - V_{OL} = 5 - 0.2 = 4.8V$$

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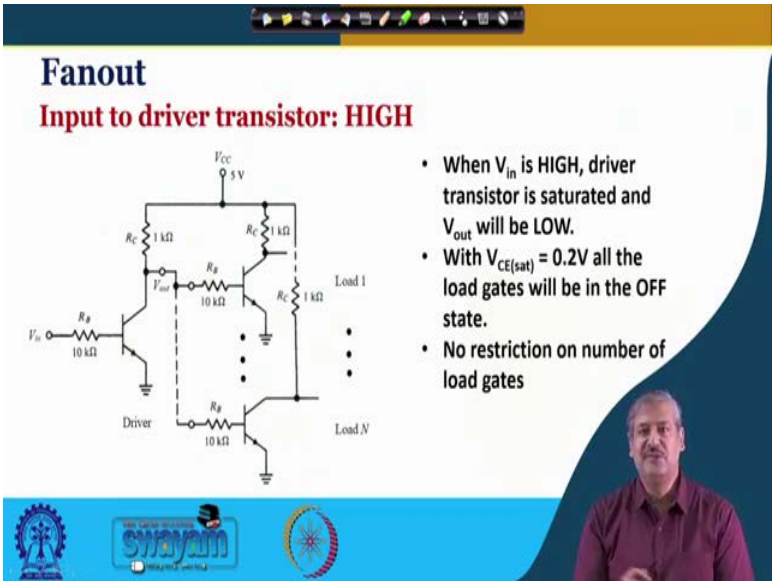

Now, we shall end with one important term called fanout and the example that we had been talking about - noise margin we know, we will take it little bit further. So, here what we see is that a transistor, a gate will never work in isolation. We know that hundreds, thousands you know such a gates are you know working together in an integrated circuit. So, this particular inverter is connected to many such inverters - ok. And when the input so, this is the driver and these are the loads load 1, load 2, load N we shall figure out how much, how many loads can be connected - ok.

So, at the input side when the input is say logic high; what will be the value here, output will be low. So, 0.2 volt also or even less - then none of this load transistors will be on, because it represents a 0.2 volt ok. So, you can connect since it is not drawing any current, you can connect many such load transistor, load gate without any difficulty, load inverter without any difficulty, is it clear?

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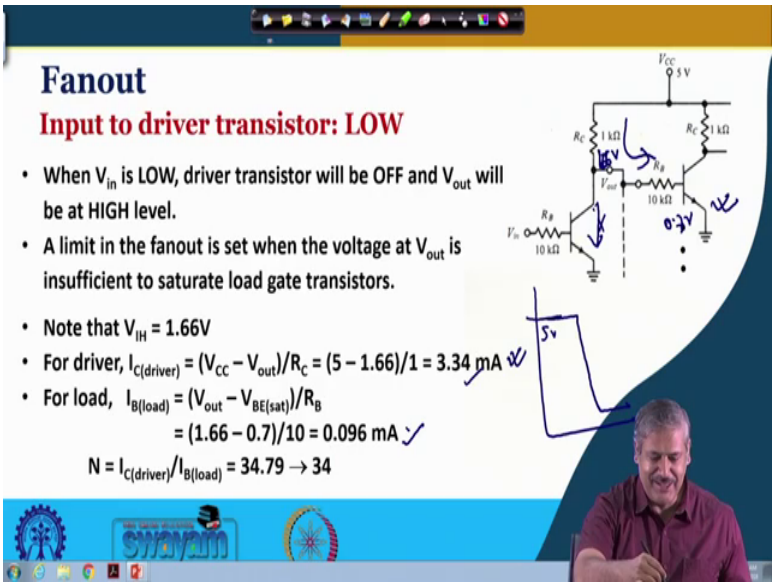

But there may be an issue when the input to the driver is low. So, this is the input to the driver when it is low the output is high, you have, you have already seen right; the characteristics part of it - isn't it? So, the characteristic show us like this. So, when input is low the output is high; so this particular thing - right. So, this output high we are connecting to many such gates - right and, whenever it is connecting these are drawing base current - right.

And though there is no current in this direction, but there is a current in this direction for which there will be I_CR_C drop; more such connection, more such more amount of current has to be delivered. And the voltage will be keep coming down, it will not - no longer be 5 volt. So, how much it can come down? So that it is still treated as logic high at output side there is a limit on that right, that is, 1.66 volt in this particular example. After which it will not be treated as logic high, it will enter into the active region; this load will be entering into the active region - ok.

$$I_{C(driver)} = (V_{CC} - V_{out})/R_C = (5 - 1.66)/1 = 3.34 \text{ mA}$$

So, that will define, that will decide how many such gates can be connected - ok. So, this is the way we calculate this one. So, for the V_{IH} we say this limiting case is 1.66 volt and driver at that time how much current it can deliver, V_{CC} minus V_{out} that is 1.66 volt divided by 1 kilo ohm. So, that is the 3.34 milli ampere, that is the maximum current it can deliver without this voltage going below your 1.66 volt, the limiting value; after which it will be

no longer treated as logic high at the input at the load gate side - ok. And for the load gate, when it is high, what is the current it is drawing? We have already calculated this one - ok.

$$I_{B(load)} = (V_{out} - V_{BE(sat)})/R_B = (1.66 - 0.7)/10 = 0.096 \text{ mA}$$

$$N = I_{C(driver)}/I_{B(load)} = 34.79 \rightarrow 34$$

So, V_{out} minus $V_{BE(Sat)}$ divided by $V_{BE(Sat)}$ divided by R_B - ok. So, this is your own 1.66 volt 1.66 volt limiting condition we are talking about and this is 0.7 volt over here right divided by R_B. So, this is 0.096 milli ampere, this is the current that is 1 load gate is taking - ok. So, how many such load gates are there, how many load gate you can connect by this? This divide the amount of current it can deliver divided by this one. And, this number is quite big I mean 34, we have to consider more, you know other issues into it, and then it will be clear - ok.

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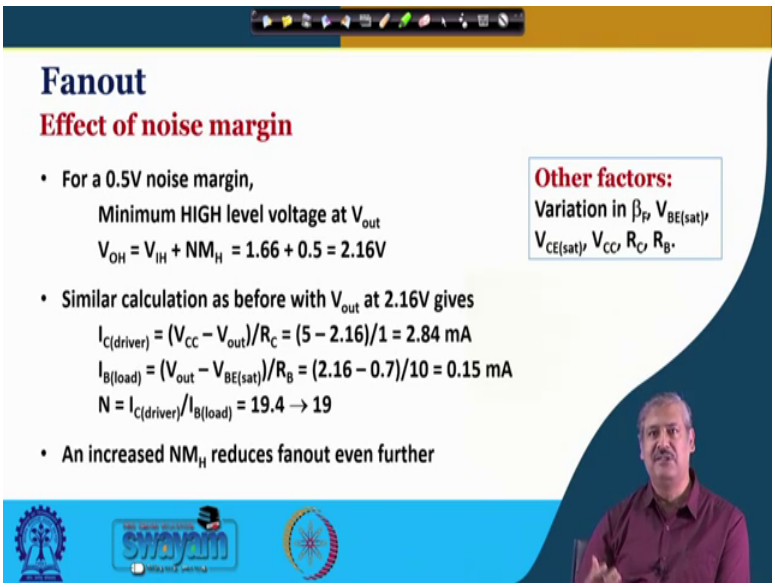

So, this is the last slide for this particular discussion. So, what is the effect of noise margin - ok? So, earlier when we talked about, when we are bringing down to 1.66 volt – ok, what becomes the noise margin, there is no noise margin there - ok. So, if you want to, because whatever was possible the we have brought down to that particular level - any noise now getting added, any noise now getting added at the output 1.66 volt and some noise with negative polarity 0 point minus 0.1 volt or so - ok. It will not be treated as logic high anymore. So, there is zero noise margin ok.

So, if you want to keep a noise margin of a desired value depending on the environment in which it is operating, then you have to consider that also into our calculation, that factor. So, this 1.66 volt will not - no longer be a 1.66 volt; it has to be plus the noise margin that we are talking about say 0.5 volt that makes 2.16 volt - ok. So, then the driver side current the maximum current it can deliver is V_{CC} minus V_{out}; now it has now considered V_{IH} as well as the noise margin - ok.

$$V_{OH} = V_{IH} + NM_H = 1.66 + 0.5 = 2.16V$$

$$I_{C(driver)} = (V_{CC} - V_{out})/R_C = (5 - 2.16)/1 = 2.84 \text{ mA}$$

$$I_{B(load)} = (V_{out} - V_{BE(sat)})/R_B = (2.16 - 0.7)/10 = 0.15 \text{ mA}$$

$$N = I_{C(driver)}/I_{B(load)} = 19.4 \rightarrow 19$$

So, that makes it 2.84 milli ampere - right and at that time what will be the load current for each of the gates. So, $I_{B(load)}$ is 2.16 minus 0.7 divided by this base resistance - is 0.15 milli ampere. And, then you look at if you just reduce the division, the number comes down to 19, from 34 it has come down to 19 drastic fall - isn't it? So, if you have more noise margin then there will be more such issues - right. So, I mean more fall in the number and then there are other parameters also,that we have not considered in this discussion. Like the beta that we have considered 50, it might be when you use the transistor it could be 40 also, it could be 30 also - depending on the make and there will be a transistor to transistor variation. So, you have to keep a you know, a consideration like what this scenario is, also.

So, each of this parameter might vary and may not be you know, the V_{BE} saturation also we have said, it is not exactly 0.7 volt can vary little bit, V_{CC} can vary 5 volt power supply may be 4.5 volt or 5.5 volt. So, these are the different things for which the actual thing, actual value we will see it that for this particular configuration from 34 to 19, now actual practically, it can come down to 5, approximately 5 such - ok. So, these are some important parameters - with an example we have noted.

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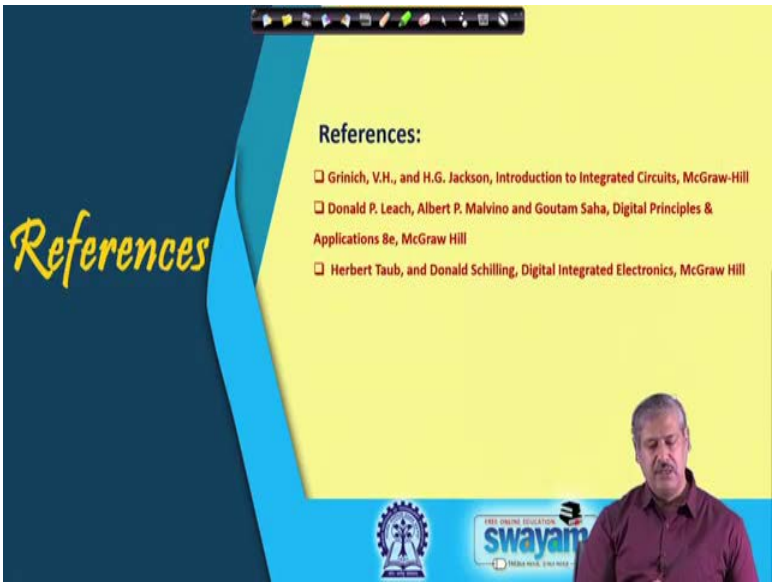

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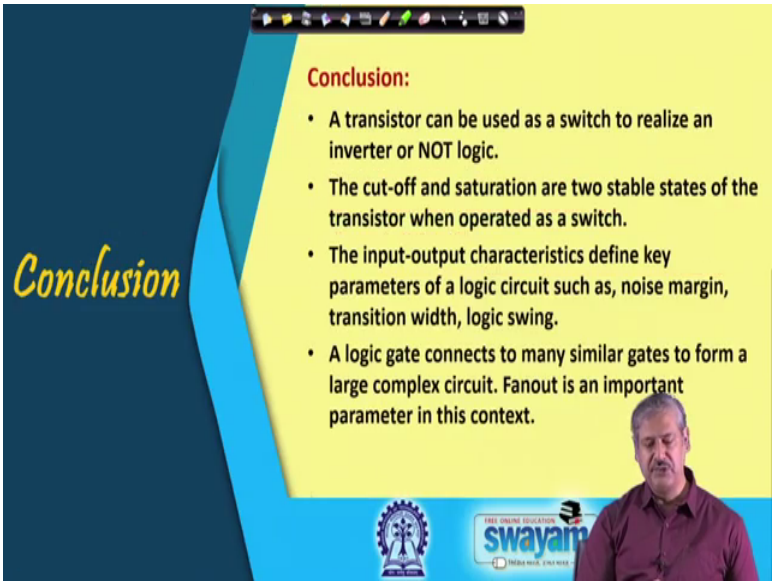

So, these are the references. So, quick summary: transistor can be used for a NOT logic. The cut off and saturations are two stable states. We have seen the input and output characteristics and from that we have derived some very important some generalized terms: noise margin, transition width, logic swing. And, we have taken up one example case and put some values and understood its significance. And, fan out is also another important parameter that also we have seen what does it mean and what is its significance and how to calculate it.

Thank you.