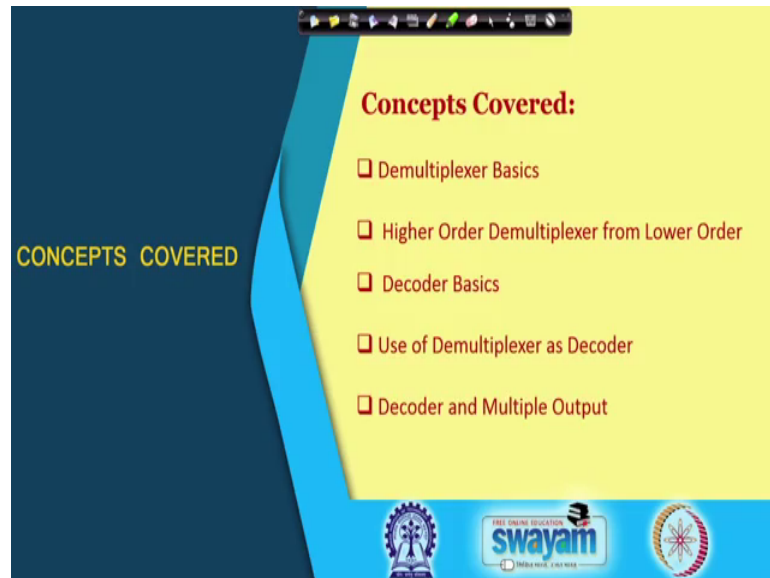


Digital Electronic Circuits
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Lecture – 18
Demultiplexer / Decoder

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Hello everybody. In the last two classes, we discussed multiplexer. And in today's class, we shall look at Demultiplexer, which is also acted together with decoder, though functionally they are different, but the circuit for each of these is essentially same. So, these are the topics that we shall cover.

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Demultiplexer

The slide illustrates a 1-to-2 demultiplexer. On the left, a block diagram shows a 1-to-2 DEMUX with input D and control input S_0 . The outputs are Y_0 and Y_1 . A truth table is provided:

S_0	Y_0	Y_1
0	D	0
1	0	D

On the right, a logic diagram shows the internal structure. The data input D is connected to two AND gates. The control input S_0 is inverted and connected to the first AND gate, and connected directly to the second AND gate. Handwritten notes in red ink show the Boolean expressions: $Y_0 = S_0' D$ and $Y_1 = S_0 D$. A video inset in the bottom right corner shows a man speaking.

And to begin demultiplexer the function of it is just opposite to multiplexer. So, in case of multiplexer, if you remember, what we had seen that it steers one of the many inputs, one of the many inputs to the output ok. So, this is we may consider this is a communication channel, which is shared by the inputs, whenever they feel like depending on the control input one of the data input is getting access to the transmission channel.

Now, when it comes to the receiver side say this is the receiver, and this is to be connected to multiple recipients, then there will be a control input to steer it to that input data to one of those recipients. So, this is just the opposite of multiplexing operation. Multiplexing was many to one, here it is one to many. So, this is the demultiplexing operation that we have to functionally understand the function of it and realize the circuit.

So, if it is a 1 to 2 demultiplexer that means, 1 input and 2 output ok. How do you do it is circuit is similar, similar to what we have done in the case of multiplexer, the similar logic we have to adopt. So, in this case this is a select input. So, when select input is low ok, we consider that it will be steers towards Y_0 the output Y_0 .

And when a S_0 at that time what is happening to Y_1 , if this is low, this is always at 0. And Y_0 because of this is 0 that is 1, so 1 and D . So, whatever is the value of D , goes to the Y_0 . So, whenever D changes from 0 to 1, Y_0 will also change from 0 to 1 and

vice versa ok. So, in the case of S being 1, what happens? So, this becomes 0 AND gate, so this will be held at 0.

And this is 1, so, Y will get Y 1 will get the D right. So, whenever D changes from 1 to 0, Y changes from 1 to 0, and also when D changes from 0 to 1, Y 1 will also change from 0 to 1 ok. So, this is what we understand as the basic circuit. If it is a 2 to, 1 to 4 demultiplexer, so we shall have similar to what you have done you had seen in case of multiplexer design, we shall have two control input through control input is S 1 and S naught and amongst them, they will be generating S 1 prime is naught prime, S 1 prime S naught, S 1 prime S 1 sorry and S naught prime, and S 1 S naught. These four combination using appropriate number of NOT gates that will be you know generated, and they will be connected to the corresponding so AND gates ok.

So, there will be four such an AND gates with 3 3 inputs similar to what we had seen in case of multiplexer. So, this is the basic circuit. And again when you work with similar to multiplexer, we shall use we shall be using a block diagram to designate a demultiplexer. So, if it is 1-to-2 to demultiplexer, this is the block diagram. So, S naught is the select input data is going to Y naught, when S not is 0, and Y 1 when it is going to when S naught is 1 this is clear.

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1-to-4 Demultiplexer

Block diagram: A 1-to-4 DEMUX block with input D and select inputs S_1 and S_0 . The outputs are Y_0 (00), Y_1 (01), Y_2 (10), and Y_3 (11).

Equations for outputs:

$$Y_0 = S_1' S_0' D$$

$$Y_1 = S_1' S_0 D$$

$$Y_2 = S_1 S_0' D$$

$$Y_3 = S_1 S_0 D$$

Handwritten notes: $S_0 = 00$, $Y_0 = 1.1.D = P$

S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	D	0	0	0
0	1	0	D	0	0
1	0	0	0	D	0
1	1	0	0	0	D

So, we extend it to 1-to-4 demultiplexer. So, they will be then to select inputs S 1 and S naught showing their 00 data is going to Y naught, 01 going to Y1, 10 Y 2, and Y 11 Y 3

ok. So, what will be the corresponding 3 input AND gates we have the output of the 3 input AND gate how will you write. So, we shall write it in this manner Y naught will be S1 prime S naught prime ended with D ok.

And similarly, for others and when this is 00 S 1 and S naught 00, what is happening Y naught is equal to 11 D is equal to D. And all list of the cases, these are 0, all three are 0. So, output is changed Y naught output is only changing according to D ok. So, if we have got a different combination of the select input, so we shall have Y 1 or Y 2 or Y 3 taking the value of D, other outputs remaining 0 ok. So, this is can be written in the form of a truth table as has been shown here.

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IC 74155

STROBE (2) 1G
DATA 1C (1)
SELECT B (3)
SELECT A (13)
DATA 2C (15)
STROBE 2G (14)

(7) OUTPUT 1Y0
(8) OUTPUT 1Y1
(9) OUTPUT 1Y2
(4) OUTPUT 1Y3
(6) OUTPUT 2Y0
(10) OUTPUT 2Y1
(11) OUTPUT 2Y2
(12) OUTPUT 2Y3

B	A	G ₁	C ₁	1Y ₀	1Y ₁	1Y ₂	1Y ₃
X	X	H	X	H	H	H	H
X	X	X	L	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L

$1Y_0 = (B'A'G_1'1C')$
 $1Y_1 = (BA'G_1'1C')$
 $2Y_0 = (B'A'G_2'2C')$
 $2Y_1 = (BA'G_2'2C')$

IC 74155: Dual 1-to-4 DEMUX

So, we now look in to one practical implementation of demultiplexer, this is similar to what we had seen in case of 4-to-1 multiplexer. So, IC 74155 is a dual 1-to-4 demultiplexer. So, if we look at the circuit, we can see that the select line is common so this is the select line which is common, and this is one 1-to-4 demultiplexer, and this another 1-to-4 demultiplexer right. S

o, this is we can observe. And for this we can see that is the strobe separate strobe, and this is another separate strobe that is present, and separate data that are present. There is one difference over here, this data over here has got a inverter, this data over here does not have been inverter ok.

So, this is we take note of, and because of which what we see the output over here can be written if you combine the logic circuit you know this inputs and the corresponding output, so we can write $Y = B' A'$ this is the output over here, as B' prime A' prime you can see this connection going over here, this is B' prime and this is A' prime ok, so this is we write as G_1 so this is G_1 prime because of the presence of the inverter and C ok. So, this is C that is there because of the two inverter that is present here is one inverter, another inverter over there.

And finally, the whole thing after this AND gate earlier there was there was only AND gate at the output. Here we see after AND gate, there is a inverter. So, whole thing is inverted ok, so this is the equation that we get. So, this is for the first case right where we have taken this example with B and A has low. And rest of the cases will be $B A'$ prime and $B' A$ the other case that will be there ok. So, this will be sorry $Y = B' A'$ will be B' prime A and so on and so forth alright.

Next one will be $B A'$ prime, and last 1 will be $B A$ right ok. So, now how then the truth table will map out. So, we will see that when the strobe is at high so strobe is this is at high, this is the value over here. So, when the strobe is at high, so that will make this output this particular output is high means this is 0 , so this a product term. So, 0 prime is 1 that is high. So, irrespective of the presence of the other value, when strobe is high all the outputs are high, this is what we can see clear.

And what we see other than that for normal operation, so this strobes should be low this should be low ok. Now, if we consider this C the input right, if this input is here low alright, so this is the case that you are talking about right. So, again the output will be high for all the cases right, and what does it imply what is it significant we shall see later. And when this is high, this is low, and this is low, and this is selected B' prime A' prime both are low. So, this is the case with example that you are showing here. So, what will happen at that time, the output is becoming low.

Now, in this case if C changes from H to L what will happen? The Y will change from low to high right. So, output this output is following the input, but just a inverted manner ok, so output is a inverted version of it. Do you see, this particular thing happening right. So, similarly for every other cases, we will see that when this is selected

as low and high right, that is B is low, and A is high. So, please correct this one right B is low and A is high right.

Then at that time when C 1 is high, the 1 Y 1 is these getting low. So, at that time if you makes C 1 low, so if you make this C 1 low, so this will go to high, we will follow this one over here. So, it is just following the input 1 Y 1 for this particular case right, 1 Y 1 is following the input, but just a inverted version of it, is it clear.

So, similarly for the other inputs for other combinations. So, this is what we see for the first set of 1-to-4 demultiplexer. So, the output is inverted in respect to with respect to the input. And for this one what we see, there is no such inversion present. So, output is just following the input, see you see if you are here it is C 2 is low right, and then the output is also low. If you it becomes high, then the output will become high. So, this is just exactly following the output the same way is it clear fine.

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1-to-16 Demultiplexer

IC 74154: 1-to-16 DEMUX

$Y_0 = (A'B'C'D \cdot \text{DATA} \cdot \text{STROBE})'$

$Y_1 = (A'B'C'D \cdot \text{DATA}' \cdot \text{STROBE})'$

.....

$Y_{31} = (ABCD \cdot \text{DATA}' \cdot \text{STROBE})'$

If STROBE = 0 and A = 0,
select inputs BCD steers
DATA to one of $Y_0 \dots Y_7$
outputs: 1-to-8 DEMUX.

So, now we look at another example, earlier we had seen 1-to-4 demultiplexer. So, if we look at 1-to-16 demultiplexer, this is IC 74154 ok. So, in this case also, we had got a strobe input right. So, this they basic equation following the same bank of you know AND gates at the output right, and there is a you can see this is the basic circuits. So, these are the select inputs right, and the output will be you see the data is inverted here, and output is also inverted here.

So, basically then output will be following the input. So, whenever input goes low, output will go low and whenever input goes high, output will go high. Corresponding output will go high, depending on this selective inputs right, so that is what you can see here.

And of course, similar to previous case, these this will work properly, when the strobe is low so this strobe is low. If strobe is high, irrespective of this selection input or the data input all the outputs are high ok. So, in strobe is low so if the data is low right, and if selection is L L L L that means, A, B, C, D is the first one is getting selected over here, all the inputs are low.

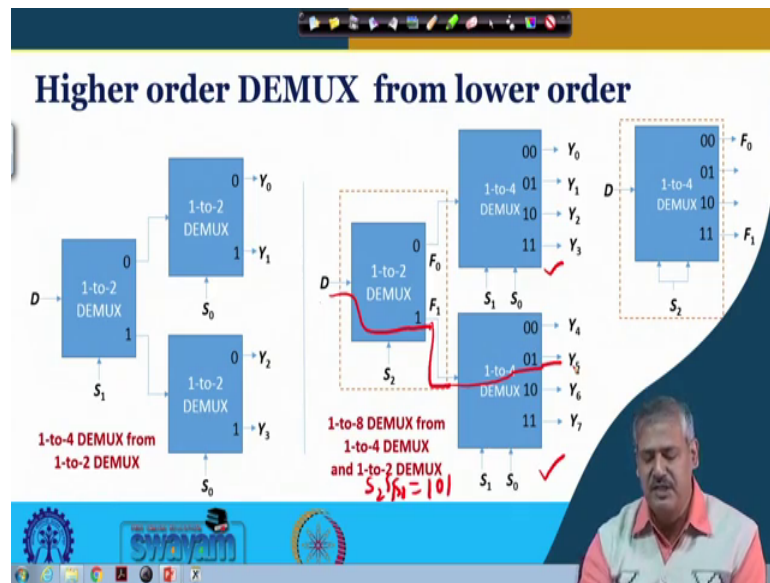
So, then corresponding Y naught is becoming low, least all are high. And if A, B, C, D is 0001 L, L, L, H low low low high, then Y 1 is low and all least are high ok. So, this is the way the similar thing what we had seen before 1-to-16 multiplexer also follows the same philosophy, and we can understand how it works.

Now, if we make strobe is equal to 0 right strobe is equal to 0, and A is equal to 0 so strobe is equal to 0 and A is equal to 0, what will happened. What is essentially, you are looking at you are looking at only the this part of the truth table right.

Now, depending on the select inputs that is B, C, D that is present, because this is always low right. So, data will go data will go data will go ok, this input data will go either to Y naught or Y 1 or Y 2 or Y 3 or finally to Y 7. So, essentially it is a 1-to-8 demultiplexer. So, form a higher order we can always get a lower order demultiplexer by making appropriate choice of this selection input, how you know give place values to the input side.

If we had made A is equal to 1 in state right, then would have looked at, we would have looked at this block right. So, depending on the B, C, D, the output would have been steered to Y 8 to Y 15 ok. So, this is the understanding we carry from this particular discretion.

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So, then how to get higher order from low order demultiplexer. Again the philosophy is similar to what you had for the details of you know multiplexer right, getting higher order multiplexer from the lower order multiplexer. So, here is an example where we see 1-to-4 demultiplexer, we get from how to get from 1-to-2 demultiplexer ok. So, there are two select lines S_1 and S_0 right.

So, depending on S_1 , so if it 0, so D will be steered in this direction alright, so data is going in this direction. And if S_0 is also 0, so data will go to this direction right. So, when S_1 and S_0 are 00, so D is connected to Y_0 D is steered towards Y_0 . If S_1 is 1, and S_0 is 0, what will happen in that case? So, S_1 is 1, so D will be steered in this direction. And S_0 is 0, so that means it will be going in this direction, so Y_1 it will get selected ok. So, we can understand that using three 1-to-2 demultiplexer, we can get a 1-to-4 demultiplexer right.

So, similar thing can happen for 1-to-8 demultiplexer if you want to get using lower order, so we have got one 1-to-4 demultiplexer here, and another 1-to-4 demultiplexer at the in the cascaded you know final stage second stage, and before that 1-to-2 the multiplexer right. So, if we take S_2 , S_1 , and S_0 as say 101 that is an example, then what will happen? So, S_2 is 1, so D is going in this direction right, so it is coming over here. Then 01, so S_1 and S_0 is 01, so it will go here right. So, D will be

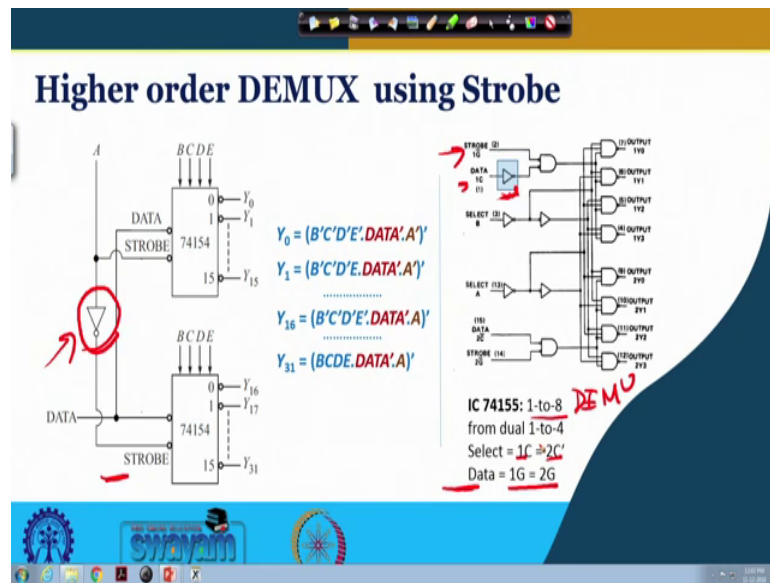
connected to Y 5 that means, D is getting steered towards Y 5, is it clear right. So, this is how we can get it.

And if we have in the stored only say in a conceptually that only 1-to-4 demultiplexer is present ok, so then this block needs to be realized by 1-to-4 demultiplexer, because 1-to-2 demultiplexer is not available with you. So, this can be realized by a 1-to-4 demultiplexer simply by converting a 1-to-4 demultiplexer to a 1-to-2 demultiplexer. One method we had seen before that one of the input we are making low or high.

So, this is another example, where both the inputs we are making common and connecting it to S 2 right. So, if S 2 is 0, so it is going here; if S 2 is 1, it is going to 1 1 that is the output. So, F naught and f 1 will be connected from 1-to-4 demultiplexer 00 output and 11 output ok. And finally, these 1-to-4 demultiplexer D 1 that you have seen we see here can be realized by three 1-to-2 demultiplexer (Refer Time: 17:47) we have done it before.

And similarly, this one also you can realize in that manner ok. So, this 1-to-8 demultiplexer can be obtained using only 1-to-2 demultiplexer, by here 1-to-2 multiplexer, and this here three 1-to-2 multiplexer, and here another three 1-to-2 demultiplexer. So, 3 plus 3 plus 1 7, 1-to-2 demultiplexer can obtaining by cascading ok. These similar to what we had seen, just the deduction is opposite, there we had gone from multiple more number of inputs, to one output here, one input to more number of outputs.

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Now, we had seen that there is a strobe input available. So, this strobe input can be useful in getting a higher order demultiplexer from a lower order demultiplexer, because within the strobe by using an inverter the way we saw here in this example, we can get a 1-to-2 demultiplexer made.

The basic 1-to-2 demultiplexer circuit if you remember, what we had done before? So, this is the basic 1-to-2 demultiplexer circuit right, S naught is selecting S naught to bar D and S naught D, one of these two inputs output is selected. So, similar thing we can employ here right, where this is the strobe input.

So, this particular combination is behaving, this particular combination is behaving like a 1-to-2 demultiplexer right. So, when A is high right, so then this is low so this is the one that is getting selected this block is getting selected. And when A is low sorry this is an active low, when A is low so this one is getting selected; and when A is 1 this 1 is getting selected right. So, this is the corresponding exam equation. So, you can follow this equation, so basically this A prime now becomes higher order the select line ok.

So, if this is S 3, S 2, S 1, and S naught, this becomes your S 4 right. So, this is your 1-to-16 and this is 1-to-16 together with this one, we are getting your 1-to-32 demultiplexer clear. So, this is basic IC 74154 equation, which we have seen before. So, strobe we are converting to a select input ok.

Now, we look at the other example. So, in this particular case, IC 74155 is seen. So, IC 74154, we had seen before, in this we have noted that that the strobe and data input are going to the same circuit over here same this is basically your if you consider this as input A and this is considered as input b, so this is what you are getting here is A prime and B prime.

So, basically whether you exchange A with B, and B with A, there is no difference ok. What I mean from the logic point of view output over here, they that cannot distinguish between A and B, now how does it help. So because of the presence of the inversion over here if you put strobe as data, if you put strobe as data and this data is strobe, then this inverter which is already present can be used to get a 1-to-8 demultiplexer from these two 1-to-4 demultiplexer.

And we do not need these external NOT gate, as we had see in this example, because they NOT gate is already present there. So, how we need to connect, we need to connect this 1 C and 2 C prime just connect them, as the select input the additional select input, third select input, and the data is connected fate through this strobe. So, 1 G and 2 G, we are connecting and we are feeding as data ok. So, you will look at this example and this example. So, we can you make use of environment you know presence of the NOT gate inverter in the case of IC 7415 because of the equivalence between these two.

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Decoder

A decoder decodes input bit pattern by appropriate logic and activates the output when specific combination is present.

To decode $AB = 01$ (active HIGH)

To decode $AB = 11$

1-to-4 DEMUX

2-to-4 Decoder

$Y_0 = S_1'S_0'D$
 $Y_1 = S_1'S_0D$
 $Y_2 = S_1S_0'D$
 $Y_3 = S_1S_0D$

HIGH

Now, this equivalence is useful, and we shall look into the next part of the discussion, where we are using a decoder. So, this decoder is a circuit where the input bit pattern is identified by an appropriate logic and the output will be accordingly activated. So, if you want to decode say $A B$ that is a you know two bit that are presented, so whether 0 and 1, A is 0 and B is 1 such a situation has arisen or not ok.

Then how we you know find it out, we can find it a would by simply a logic circuit like this. So, if you want to realize understand this, so $A \text{ prime } B$, so this with this we can figure it out. So, when is A is 0 and B is 1, Y will become 1. Otherwise, it will remain 0 for other three possible cases of A and B , it will remain 0.

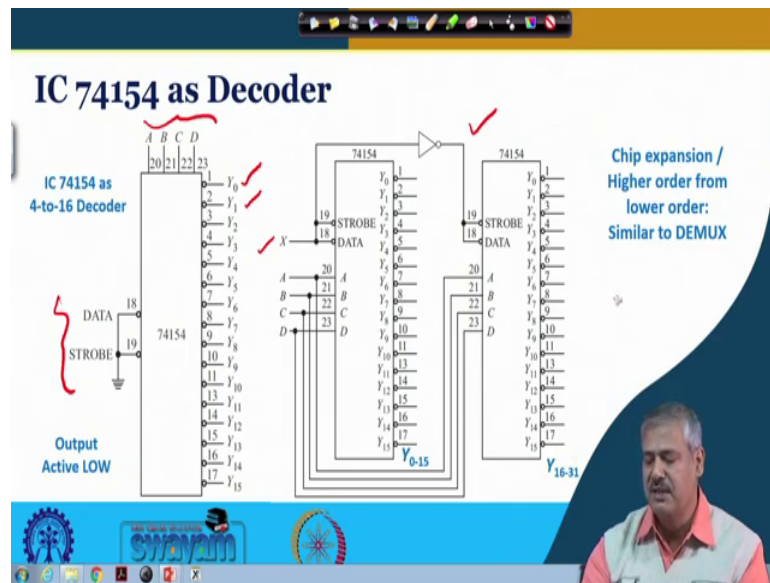
So, to decode AB is equal to 11, we need this kind of circuit. So, if you want to have a circuit which can decode all four possible combination depending on our requirement, we can make use of one or the other. So, we can see inherently the 1-to-4 demultiplexer circuit that we had it is following this in a particular output you know combinations.

So, essentially if D is equal to 1, in each of these cases this Y naught, Y_1 , Y_2 , and Y_3 , there actually decoding the select inputs isn't it. So, Y naught is $S_1 \text{ prime } S$ naught prime, so it is equal to 1. So, in this case if 00 is present, Y naught will be 1. So, if Y naught goes high, then we can say that $A 00$ has been presented right, and for any other combinations it will be 0.

So, if you want to decode say 10 right, so D is high. And if we shall just look at Y_2 , whenever Y_2 goes high, we know that a 10 is present. So, this will be the corresponding circuit, so that is what I said that decoder and demultiplexer circuit is essentially same.

So, just we have change in the orientation. So, this select lines now becomes the input line ok, input you know combinations that need to be decoded, and these are the corresponding output, and data input we are making high ok. So, if there is a strobe, strobe also will sell make activate at that time. Basically, it is between a understanding a relationship between the select lines and the output in demultiplexer, which is converted to data or bit patterned to output in decoder.

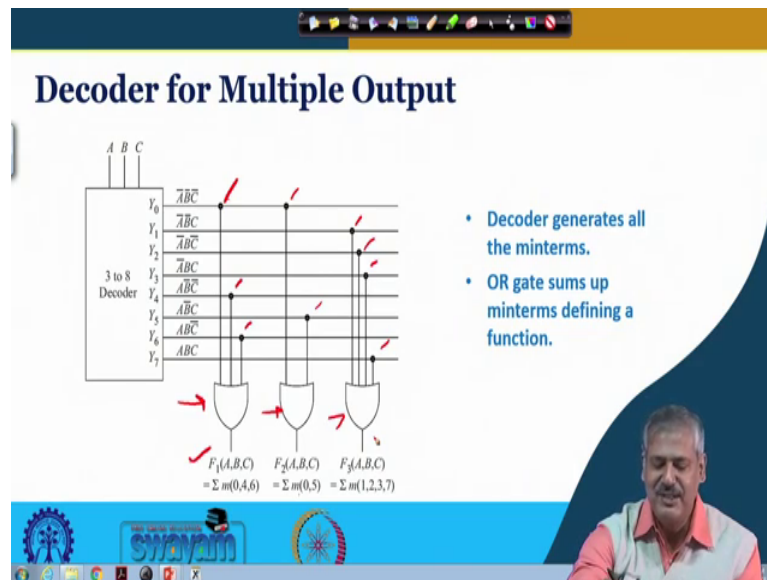
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So, the IC 74154 which is a you know 1-to-16 demultiplexer. If you want to make it to make it work like a 4-to-16 decoder, so what we need to do? We shall just discuss we shall make this as active right, but that is active low, so that is why it is connected to ground. And now it is the decoding the presence of the A, B, C, D. So, these are the data pattern.

If 0000 is present, so this is activated; If 0001 is present, this is activated and so on and so forth. And if you want to make a instead of you know 4-to-16 decoder say 5-to-32 decoder. So, the why we are done in case of demultiplexer, we shall use the same kind of you know cascading using strobe and data right. So, this is the fifth input by which we can get a 5-to-32 decoder ok. So, this is similar to the remarks concept, we had remarks expansion concept that we had seen before.

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And finally, while we are talking about you know decoding, and steering a output input from one of the many possible output. So, this decoder can be useful or this particular demultiplexer decoder can be useful in generating multiple outputs. So, if you are looking for in a particular problem multiple output, so we can make use of a decoder or combination ok.

So, this decoder so these an example given, so 3-to-8 decoder. So, this Y_0 to Y_7 , it is generating actually all the minterms. So, in A, B, C all are 0, this will be high Y_0 will be high is not it. And on A, B, C is 001, so Y_1 will be high. So, this is nothing but the corresponding minterms that is getting generated. So, if you want to generate a function if you want to you know realize a function F_1 , which is a sum of minterms 0, 4, 6, F_2 sum of 0 and 5, and F_3 sum of 1, 2, 3, 7.

What we need to do, this outputs are there ok. And we are just making appropriate or of them so 0, 4, 6. So, this one Y_0 , this Y_4 , and Y_6 right. And similarly 1, 2, 3, 7 this is Y_1, Y_2, Y_3 and Y_7 . 0, 5 Y_0 , and Y_5 . And just we are summing name of with an OR gate, multi input OR gate, and the job is done ok. So, this is one usefulness of another usefulness of decoder demultiplexer circuit.

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Conclusion

- A demultiplexer steers the data input to one of the many outputs based on control input(s).
- With n control inputs, the data input can be steered to up to 2^n outputs.
- Strobe or Enable input of a demultiplexer chip need to be active for usual operation.
- Higher order demultiplexer can be obtained from lower order and vice versa by appropriate connection.
- A decoder decodes input bit pattern and activates the output when specific combination is present.
- Demultiplexer circuit can be made to act as decoder e.g. 1-to-4 Demultiplexer can act as 2-to-4 Decoder.
- Decoder generates all minterms. Decoder-OR combination can generate multiple outputs.

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So, with this we conclude today's discussion. And demultiplexers steers the data input to one of the many output to based on control inputs with n control inputs, the data input can be steered to up to 2 to the power n outputs. Strobe or enable input of a demultiplexer chip need to be active for usual operation. Higher order demultiplexer can we obtain from lower order and vice versa by appropriate connection.

A decoder decodes input bit pattern and activates the output when specific combination is present. Demultiplexer circuit can be made act as a decoder, for example 1-to-4 demultiplexer can activate 2-to-4 decoder and since decoder generates all minterms. Decoder or combination can generate multiple output by summing the minterms that is generated out of the decoder.

Thank you.