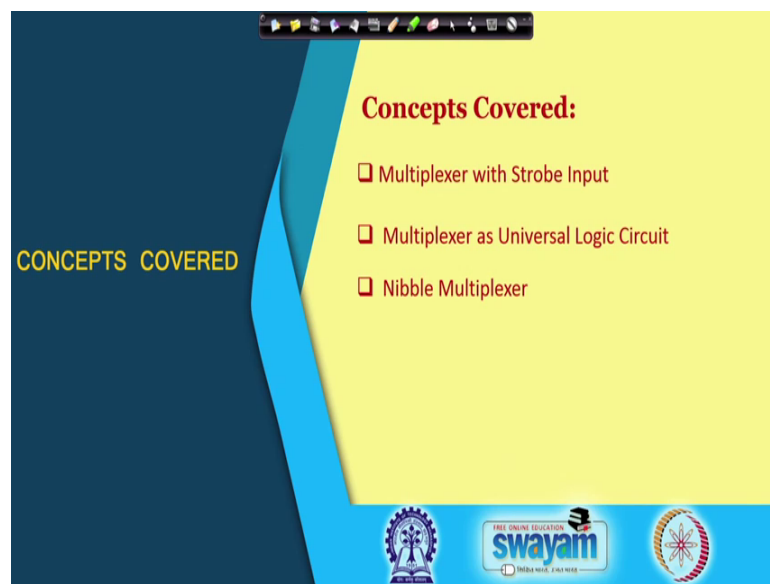


Digital Electronic Circuits
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Lecture – 17
Multiplexer: Part II

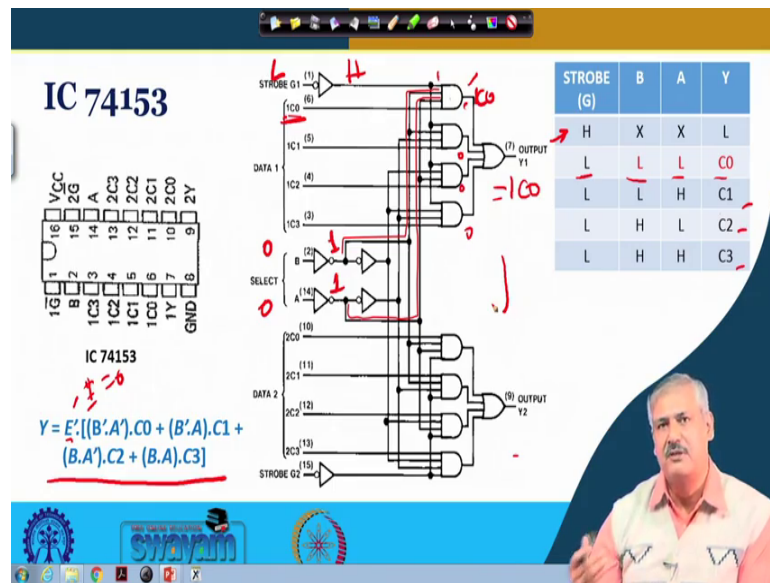
Hello everybody, we are in the 17th class and this is where we discuss the Multiplexer, second part of the multiplexer.

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In the last class we had seen the basic concepts concept of multiplexer and in this particular class we shall look at some practical ICs Integrated Circuits which are used for multiplexer multiplexing operation and we shall look into how they are developed and how they work. So, this class will be mostly on the practical use of multiplexer in your lab or any project or any design activity that you plan how you take the go for the hardware implementation.

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So, in the first slide we discuss IC 74153 ok. So, in this particular IC we see a 4 to 1 multiplexer. So, 4 to 1 multiplexer the basic concept we have already seen we had seen in the last class ok, but in when you practically implement it you see in this particular IC there are 16 pins, this is 1 to 8 and 9 to 16 and this is how the circuit is made up of. So, in the circuit if you look at it I will discuss it I mean with all the inputs and other things. So, first thing you can see there is 1 4 to 1 multiplexer over here this is 1 4 to 1 multiplexer that you can see there are some other additional inputs you shall discuss later.

So, this is another 4 to 1 multiplexer that we can see. So, basically this is a dual; that means 2 4 to 1 multiplexer is there. The other thing that we can see is that the select input B and A it is termed as B and A. So, this is common for both the units this multiplexer and this multiplexer select input is common that is what we can see. And the third thing we see that each of this multiplexer has separate 2 separate input one called STROBE G 1, another this is; another STROBE G 2. So, this G 1 you see is connected you can see from here to here. So, this strobe is not getting connected to this place this strobe G 2 is connected to this 4 ok.

So, the strobe part is individual. So, this strobe is affecting only this 4 to 1 multiplexer and this strobe is affecting only the bottom 4 to 1 multiplexer this is what we can visualize. Now we will look at how this particular circuit works this practical circuit which is there in the form of integrated chip IC. So, integrated circuit we shall see how it

works. So, when strobe is high. So, there is an inverter of what is there it is actually a NAND operation that is happening. So, this output is 0, if strobe is high 1 this output is 0. So, if this is 0 for all the odd all the and gets the output will be each of them, if they output is 0. So, their final output Y_1 will be what 0 1 that is low irrespective of whatever is the value of B A and these are the data inputs whatever be the value the output will be low.

So, that is what you see over here when strobe is high the output is low irrespective of X X means do not care the value of B and D this is happening for the bottom one also if this strobe is this strobe over here is high then this output will be low. So, this is symmetrical fine. So, for normal multiplexing operation this strobe needs to be at low ok, then this is high and get. So, the operation goes to the other inputs now let us just take a one particular example. So, the select input is a 0 0 ok. So, then this is 1 and this is 1. So, these 1 is connected over here to this and gate this 1 goes to the and gate (Refer Time: 04:50) line right.

So, this is the other input. So, these 3 inputs are 1 now. So, these and gate output now will be whatever is 1C 0 that is the data inputs. So, 1 here means first block this is dual package C NAND is the D NAND the equivalent of what you had seen in the last class ok. So, this is the data input. So, this is what when you will get 1C 0 over here and for all the other and gates you will see this select input these are connected in such a manner that one of them is 0 ok. So, one of them 0 means irrespective of what about the data inputs are each of these are 0 right. So, what will be the output then is 1C here ok.

So, when this is low right and these 2 are low and low then the output is this C 0 is the output over here similarly over here in the bottom place also, when this is low and high it will be C1 high low this is C 2 and this is C 3 this is nothing, but the multiplexing operation.

So, additional thing over what we discussed in the last class you see is the presence of this strobe which is nothing, but an enable like control input that when strobe is high the multiplexer is disabled when strobe is low the normal multiplexing operation is taking place and we can have the corresponding equation over here. So, we can see if E is equal to 0, E is your strobe is enabled. So, if E is equal to 0 then this is 1 and normal

multiplexer multiplexing equation is there and when is equal 1. So, this is 0 this whole thing is 0.

So, is this clear? So, nothing to be scared like you know what is this circuit looks like it is nothing, but 2 4 to 1 multiplexer with additional enable input, that enable input is going to the and gates each one of them and making it operational, I mean the normal multiplexing operation for a specific value and other value it is a fixed logic low it is you know holding at the output.

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Multiplexer with inverted output

INPUTS				STROBE G	OUTPUT W
A	B	C	D		
X	X	X	X	H	H
L	L	L	L	L	E0
L	L	L	H	L	E1
L	L	H	L	L	E2
L	L	H	H	L	E3
L	H	L	L	L	E4
L	H	L	H	L	E5
L	H	H	L	L	E6
L	H	H	H	L	E7
H	L	L	L	L	E8
H	L	L	H	L	E9
H	L	H	L	L	E10
H	L	H	H	L	E11
H	H	L	L	L	E12
H	H	L	H	L	E13
H	H	H	L	L	E14
H	H	H	H	L	E15

$Y = (E_0.A'B'C'D'.D_0 + E_1.A'B'C'D'.D_1 + \dots + E_{15}.ABCD'.D_{14} + E_{15}.ABCD'.D_{15})$

So, if this is clear. So, we look at another circuit multiplexer circuit which is there where the output is inverted earlier we have seen all the output is just you know whatever is the input output is following the input ok.

So, I is equal to D naught D 1 and so on and so forth. So, here is the circuit IC 74150 this is a 16 to 1 multiplexer right. So, it also has got a strobe input. So, strobe now we understand no problem. So, whenever the strobe is high irrespective of the others what is there in the select input output is high, why output is high, you see this is and gate and this is a or gate after that there is a inverter ok. So, in the earlier example we had seen that if this is high. So, this will be 0 all of them will be 0. So, they output we will be 0, but because of the presence of the inverter now we see the output is high is this clear.

So, only when the strobe is or the enable is low the normal multiplexing operation is taking place. So, low, low, low, low so, all these things are low then E naught will go to the output right E naught will go to the output. So, Y will be E naught, if this bubble is not there in inverter is not there since this inverter is present Y will be E naught bar Y will be E naught bar, similarly for other cases E 1 bar, E 2 bar, E 3 bar and so, on and so, forth ok. So, in earlier cases examples we had considered these inputs to D naught D 1 data input. So, previous I C chip we have seen that that was use as C naught and here, here the manufacturer the datasheet they are representing it as E I, E naught E 1, E 2, E 3.

But you know the meaning dimension is same is it clear. So, this is what we can see and corresponding then equation becomes what this is the basic equation we had seen which we had seen before which enable with ok, now because of the presence of this inverter the whole thing after that there is a inverter connected ok. So, this is what become the equation and the corresponding logic circuits simple.

(Refer Slide Time: 09:28)

IC 74153 ✓

$$Y = E'[(B'A).C0 + (B'A).C1 + (B.A).C2 + (B.A).C3]$$

	B	A	Y
F(0,0)	L	L	0
F(0,1)	L	H	1
F(1,0)	H	L	1
F(1,1)	H	H	0

$Y = B'A + B.A'$

$Y = (B'A).0 + (B'A).1 + (B.A).1 + (B.A).0$

¼ IC 74153, E=0

IC 74151 ✓

8-to-1 MUX with STROBE (EN'), both non-inverted and inverted output

$$Y = F(A, B, C) = \sum m(0, 2, 3, 6, 7)$$

Now, we look at realization of certain truth table using multiplexer right. So, earlier you had seen in the last class that this is possible using Shannon's expansion theorem and all right here we are taking some practical IC and we looking at it is realization.

So, in this case we are looking at IC 1 74153 to the 4 to 1 multiplexer, we have changes before with strobe or enable input. So, that is the basic equation of that and you want to

realize a truth table which is something like this ok. So, this truth table $F = 0, 0$ whenever these 2 values are $0, 0$ it is $0, 0$ $1, 1$, $1, 0$ 1 and $1, 1$ so, this is 0 . So, this is corresponding you know logic equation basic logic equation. So, this we can write in terms of all the main terms $B' A' \cdot 0$ $B' A$ ended with 0 , $B A$ ended with 1 $B A'$ ended with 1 and $B A$ ended with 0 .

So, this looks like a multiplexer equation with D_0 is equal to 0 , D_1 is equal to 1 , D_2 is equal to 1 and D_3 is equal to 0 , is not it right and in the 74153 context this is our C_1 , C_0 , C_1 , C_2 , C_3 so, C_0 is 0 C_1 is 1 C_2 is 1 and C_3 is 0 ok, C_0 , C_1 , C_2 and C_3 right.

So, what we do we take only half the top part of the IC 74153 or bottom part one part of it right B and A we connect the $B A$ you know we does just the input is connected right. We put E is equal to 0 or the strobe is equal to 0 if you are taking the top part then the top part of the strobe G_1 we take as 0 and the corresponding $1C_0$, $1C_1$, $1C_0$, $1C_1$, $1C_2$, $1C_3$ we put as 0110 and we will take from Y the first part and the this particular true table is realized is it clear. So, that was for a 2 variable realization. So, for a 3 variable realization we can look at IC 74151 which is a 8 to 1 multiplexer.

So, 8 to 1 multiplexer it also has got a strobe input similar to that and, but it has got both non- inverted and inverted output. We have seen non- inverted output for IC 74153 and you have seen inverted output for IC 74150. So, IC 74151 has got both the version. So, basically you can have you can use any one of them depending on your requirement and you want to realize the truth table which has got this mean terms $0, 2, 3, 6, 7$ ok.

So, how do you go about? So, this is the 8 to 1 multiplexer these are the select inputs and we know $0, 0, 0, 0, 0, 1$ to upto $1, 1, 1, 1$ these are the corresponding data inputs and going by the previous discussion in the earlier class and just now what you have done for 4 to 1 multiplexer 2 variable example. So, wherever these mean terms are existing corresponding D_0 value at D_0 , D_1 value we put them as 1 . So, 0 is there. So, D_0 in place of D_0 we will put 1 , then 1 is not there interm 1 is not present. So, in place of D_1 we shall put 0 so, accordingly $0, 2, 3, 6, 7$. So, $0, 2, 3, 6, 7$ we put 1 and rest of the places we put 0 .

And we take the output from the non inverted output and the function is realized is it clear. So, this is the way it can be realized by the ICs in hand.

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Multiplexer as Universal Logic Circuit

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

$$Y = (E'.A'B'C'D'.D_0 + E'.A'B'C'D.D_1 + \dots + E'.ABCD'.D_{14} + E'.ABCD.D_{15})'$$

$$E = 0,$$

$$Y' = A'B'C'D'.D_0 + A'B'C'D.D_1 + \dots + ABCD'.D_{14} + ABCD.D_{15}$$

$$Y = F(A,B,C,D)$$

$$= \sum m(0,2,3,4,5,8,9,10,11,12,13,15)$$

$$Y' = \sum m(1,6,7,14)$$

And because of this we can tell we can find that multiplexer can be used as a universal logic circuit. What does it mean? It means that any logic function can be realized using a multiplexer Y appropriately placing the input values. The data input values appropriately placing just it is a how you (Refer Time: 14:08) you know place the zeros and ones at the input side you get the logic function realize. So, you have to just in expand the logic function logic Boolean equation in terms of where all the mean terms are present and accordingly we will place the inputs.

So, this is a 4 variable example and if it is a 4 variable example we what shall we use, we shall we use 74150 which is 16 to 1 multiplexer. So, in this 16 to 1 multiplexer one thing we need to take note of for IC 74150 that this is a, this is giving a inverted output this is giving a inverted output. So, to realize what we can do let us see one example. So, this is the basic equation of IC 74150 which you have seen before ok. So, this is the inversion that we are talking about right and so, first of all we put E is equal to 0 that enable otherwise the multiplexing operation will be not be there. So, this is a strobe and the truth table that you want to realize is, this is the truth table that you want to realize ok.

So, we give select input ABCD over here like this, these are the corresponding pin numbers right and this truth table in terms of minterms this is how you write 0, 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 15 ok. Now if Y is this particular function over here this is prime, then Y prime is what you get over here, you take in a prime you know inversion in the

both sides. So, this is your Y prime and this is the basic multi multiplexer equation. So, these are this is if you are trying to realize these as Y what is the corresponding Y prime? Y prime is the terms that are not included here the maxterms these are the main terms ok. So, Y prime if you write in terms of you know the terms that are left over is 1 over here, 6 over here, 7 over here and 14 over there ok. So, Y is like this, Y prime is this one is it fine.

So, in this case since it is generating Y prime by this equation. So, what you need to you know connect so, 1, 6, 7, 14. So, 1 D 1 D 6, D 7 and D 14 you connect to high logic high and rest you connect to ground, is it clear. Otherwise you would have needed if you go by the normal thing that 0, 2, 3, 4, 5 you put connect it one then you have to put another inverter after this ok, but it is equivalent truth table is Y prime is wherever 1 is there that is there is a 0 and wherever 0 is there, there is a 1. So, you realize Y prime that is equivalent to get realizing Y the same truth ok. So, this is what you can do when you have got inverted output you can make a judicious decision and that will reduce your hardware and all.

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Entered Variable and Multiplexer

The slide illustrates the implementation of a 3-variable function $Y = F(A, B, C) = \sum m(0, 2, 3, 6, 7)$ using multiplexers. It includes the following components:

- Truth Table:**

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1
- 8-to-1 MUX:** A diagram showing an 8-to-1 multiplexer with inputs 000 to 111 and outputs A, B, C. The output Y is connected to the data input of the 4-to-1 MUX.
- 4-to-1 MUX:** A diagram showing a 4-to-1 multiplexer with inputs 00, 01, 10, 11 and outputs A, B. The output Y is connected to the data input of the 8-to-1 MUX.
- Equation:** $Y = F(A, B, C) = \sum m(0, 2, 3, 6, 7)$

Now, so, far we have seen that as many number of variables for realization as many number of control input or select inputs will be required ok, but if you have got a problem where you want to realize a 3 variable function, but you have got only 4 to 1 multiplexer available with you. Can you go ahead, it is possible if we utilize the concept

of entered variable which we had done in earlier case where entered variable map based minimization and all ok.

So, let us look at how this can be done through an example. So, this is one particular truth table that we want to realize ok. So, 1 0 these are the terms main terms which is present and accordingly if it is 2 multiplexer this realization it is very simple wherever 0 0 0 this is 1. So, this is a one present and we are just following this over here. And the circuit is realized it is as simple as that using 8 to 1 multiplexer.

Now since 8 to 1 multiplexer is not present we have got only 4 to 1 multiplexer. So, we can look at combining the inputs the why we had done in case of entered variable you know based minimization. So, if we consider C as the variable that will enter.

So, you form pair in this manner right if we recollect. So, here both A and B are 0 0 right. So, when both A and B 0 0, we see that Y is just in you know prime of C. So, Y is C prime and for other cases we see Y is equal to 1, Y is equal to 0 and Y is equal to 1 just if you take them as pair ok, how the output is there output is not dependent on C other variable. So, only in this case it is dependent on C, but just C prime ok.

So, in the 4 to 1 multiplexer with a b as select input now for 0 1 this is the 0 1 case 1 0 and 1 1 this 3 cases we put 1 0 1 as you see over here right and for 0 0 we put C prime ok. So, these also realize the 3 variable function, but using a 4 to 1 multiplexer ok.

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8-to-1 MUX and 4-variable function

$Y = F(A, B, C, D)$
 $= \sum m(0, 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 15)$

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1

$\Rightarrow Y = D'$
 $\Rightarrow Y = 1$

ABC	000	001	010	011	100	101	110	111
D=0	1	1	1	0	1	1	1	0
D=1	0	1	1	0	1	1	1	1
Y	D'	1	1	0	1	1	1	D
8-to-1 MUX data input	$D_0 = D'$	$D_1 = 1$	$D_2 = 1$	$D_3 = 0$	$D_4 = 1$	$D_5 = 1$	$D_6 = 1$	$D_7 = D$

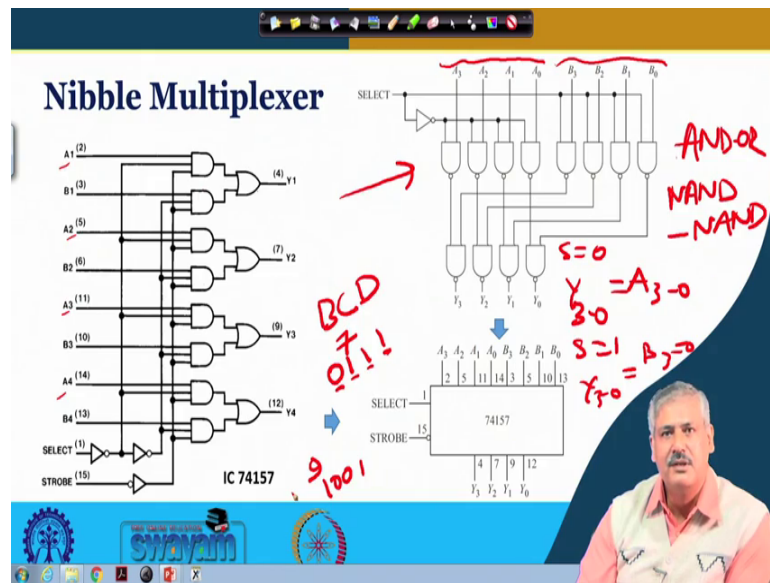
IC 74151
EN = 0

So, this is the usefulness of this exercise and this can be extended to realization of 4 variable function using 8 to 1 multiplexer just 1 1 order less the way we had seen it before how it happens for inter variable based you know minimization in a (Refer Time: 20:25) map similar thing we see that one order list is required for the multiplexer to be used for realization of the truth table. So, in this case there is another example where we have got 4 variable the main terms are 0, 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 15.

So, these are the main terms that we generate again we form pairs the way we had done it for the previous example ok. So, when ABC is 0 0 0. So, 8 to 1 multiplexer means 3 select inputs will be there. So, output is just invert of D and here the output this is Y is equal to D prime, this is Y is equal to 1 ok. So, this is the why the rest of the things will be there in form of a table you can see what has been shown here. So, B is equal to 0 0 0, D is equal to 0 and D is equal to 1 these are the 2 cases. So, this is 1, this is 1, this is 0, this is 0. So, Y is equal to just opposite of it.

So, basically it is for 0 it is 1 1 it is 0. So, it is D prime. So, similarly you compute the rest of the things you will see that Y is equal to D prime over here, 1 1 0 1 1 1 and this is D ok. So, then you are corresponding realization using IC 74151 with enable as 0 and you are taking these non inverting output then for 0 you are putting D prime. So, this is D prime and for 7 over here ABC 111, you are putting D D 7 as D and rest of the cases you are putting zeros and ones as per the requirements. So, 3 is equal to D 3 is equal to 0 and rest of the D 1, D 2, D 4, D 5 and D 6 their work and circuit is realized truth table is realized. So, that is how this multiplexer is very useful in and used as a universal logic circuit.

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Now, we shall look at some aspect of a practical multiplexer IC which is 74157. So, this is 74157 if I ask you how many multiplexer is there and what is the time, then you can see first of all how will you investigate this circuit. So, one is strobe at the inputs and you can side you can be see which is there common to all of them. So, if strobe is here it is a low sorry high then it is low. So, all the all of them will be the output will be 0 ok. So, when strobe is low then only the normal multiplexing operation is there. So, that is what we have studied before and we are understanding the other thing that we see that there is only one select input ok. So, one select input.

So, this is with one select input you can get 2 to 1 multiplexer right fine and we can see that there is one block over here, there is another block over here, there is another block over here and there is another block over here. So, 4 2 to 1 multiplexer is there ok. So, this is called quad 4 is quads. So, earlier we had seen dual this is a quad. So, this 4 2 to 1 multiplexer is there with one common select and common strobe right. So, if I write in the form of a logic circuit you for a in a better understanding.

So, this is what you can see. So, this is A 1, A 2, A 3, A 4 in the, this is the as far as the you know manufacturers you know data sheet, what we are representing this here as same the same thing as a 3 to A naught for certain reason which I tell you later. So, similarly B 1 to B 4 we are representing the exactly the same thing B 2 to B naught I

mean basically the same inputs just designation is different and when select is 0 select is 0 this set is selected.

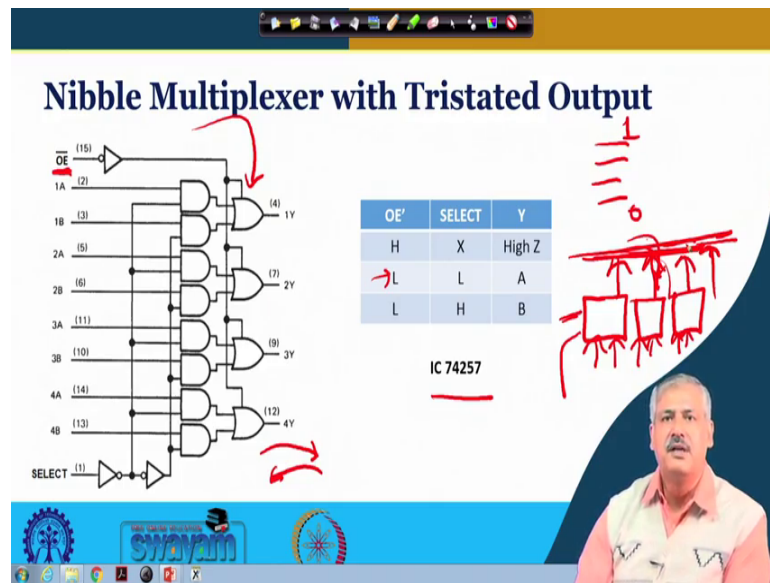
So, basically this is AND OR and or is also your NAND NAND operation. So, that you have seen before in earlier weeks. So, meaning remains same it should be realization using and or and NAND NAND. So, this is an alternate representation of the same circuit. So, what you see here is that when select is 0 this Y_3 becomes A_3 and when select is 1, then Y_3 becomes B_3 to 0 is it fine ok.

So, this selection of four such bits as a whole. So, this 4 bit as a group is called nibble ok. So, this is also known as nibble multiplexer and this has got its usefulness say we are talking about we shall see later in more greater detail see binary coded decimal ok. So, a decimal number say 7 we want to code it in binary how will you do it, 0 1 1 1 ok.

So, this is the zeros bit first bit second bit and third bit. So, there is certain weight associated more of that we shall discuss later in the subsequent weeks and if we represent 9, what is 1 0 0 1 ok. So, these are the way they are represented. So, if you want to output one of these 2 numbers depending on certain condition being fulfilled say either 7 or 9 right. So, we need a group of 4 bits.

So, this 4 bits have come in as a whole either 7 will come or 9 will come and accordingly there will be some display and other things more of that we can discuss later. So, this is what is done and this can be done through nibble multiplexer. So, 4 bit can be selected (Refer Time: 27:11) if we require more than 4 bits then we have to (Refer Time: 27:17) we have to have another such unit there. So, this is the corresponding circuit you can see.

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So, now, at times this nibble multiplexer is connected in a manner where many such units are trying to place data. So, this is one block, this is one nibble multiplexer, this is another nibble multiplexer right and they are trying to place data over a common line depending on which one is getting selected.

So, if this is selected that is the strobe is there right and the other I mean all this these cases. So, corresponding depending on the value one of the 2 set of inputs will go there right. Now if one common line is there in which all of them are trying to send data then the data might get no corrupted because if out of this 4 lines one is sending one another is at the time is sending say 0 there is a you know problem.

So, when one is sending the other one must not send ok. So, and not only that it must not also take any value take any you know electrical energy from this particular circuit. So, it should remain electrically insulated. So, this is known as high impedance. So, this is we have seen a discussed before this is achieved by a tri stated you know output. So, this try stated output is useful whenever we are talking about sending or grouping multiple of multiple bits and sending from one place to another is you know it is more important in that context.

So, in this case IC 74257 earlier we had seen IC 74157 is a nibble multiplexer ok. So, IC 74257 is also a nibble multiplexer. But now we have got an additional input over here which is output enable ok. So, this output enable is what does it do it is just tri stating the

output; that means, if this is not if this is high then irrespective of what is selected nod output will be at high impence. So, neither it will send anything nor it will take anything from the external world it is connected to external electrical circuitry. It is connected to only when it is low the output will be following the, you know basic multiplexing operations so, the nibble as a nibble multiplexer.

So, this is different from the strobe thing which you need to understand strobe what does it do, output will be all high or all low depending on how it is connected output is inverted or non inverted. But it is having some value it is not high impedance and that might corrupt the data over here if it is having a common bus kind of architecture right, but in tri stated this is only a high impedance case. So, this is something which we take note off.

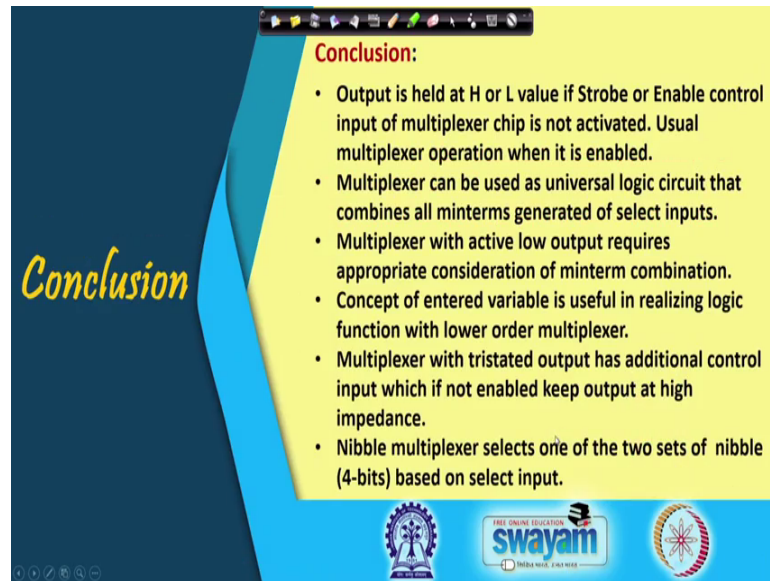
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The image shows a presentation slide with a dark blue background on the left and a light yellow background on the right. The word "References" is written in a large, yellow, cursive font on the dark blue background. On the right side, under the heading "References:", there is a list of two items:

- Donald P. Leach, Albert P. Malvino, and Goutam Saha, Digital Principles & Applications 8e, McGraw Hill\
- Technical documents from <http://www.ti.com> accessed on Oct. 08, 2018

In the bottom right corner, there is a small video inset showing a man with grey hair and a mustache, wearing a light-colored shirt, looking down. At the bottom of the slide, there are logos for "swayam" (Free Online Education) and "INDIA WITH EDUCATION".

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Conclusion:

- Output is held at H or L value if Strobe or Enable control input of multiplexer chip is not activated. Usual multiplexer operation when it is enabled.
- Multiplexer can be used as universal logic circuit that combines all minterms generated of select inputs.
- Multiplexer with active low output requires appropriate consideration of minterm combination.
- Concept of entered variable is useful in realizing logic function with lower order multiplexer.
- Multiplexer with tristated output has additional control input which if not enabled keep output at high impedance.
- Nibble multiplexer selects one of the two sets of nibble (4-bits) based on select input.

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So, with this we complete the depletion on multiplexer very quickly what you have seen that output is held at high or low depending on output is inverted non inverted by when the strobe enabled control input of the multiplexer chip is naught not activated and when it is activated normal multiplexing operation takes place multiplexer can be used as universal logic circuit ok.

And a lower order multiplexer can be used where the concept of entered variable comes into picture by which we can obtain a logic function and multiplexer with tristated outputs as additional control input which not enabled keep the output at high impedance and enable multiplexer is useful when group based binary operations are done ok.

Thank you.