Digital Circuits
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Lecture – 40
Data Converters (Contd.)

So in case of ADC Analog to Digital Converters so, there are several errors that can come up. So, 2 major error are aliasing error and quantization error.

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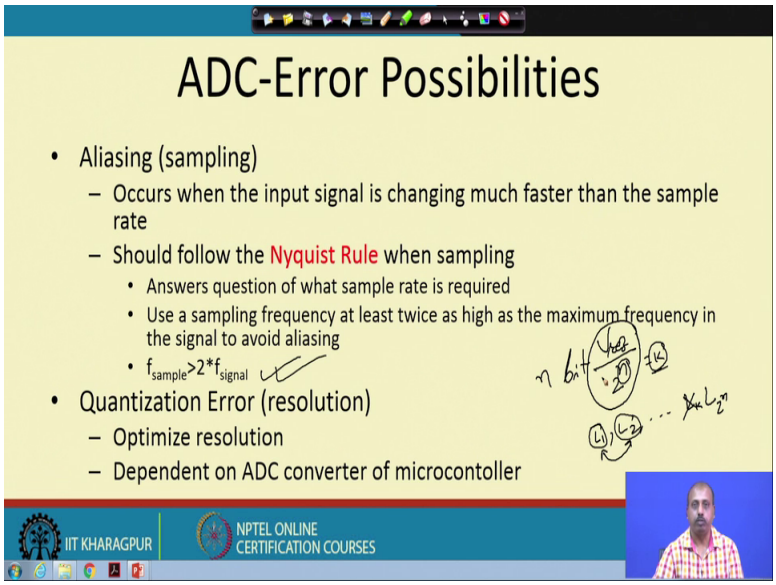

So, aliasing error so, or sampling errors so, this occurs when the input signal is changing much faster than the sampling rate. So, we have seen previously while discussing on sample and hold circuit, that the sampling rate should be sufficiently high so that signal can be reconstructed at the receiving end.

So, here also when we are converting one analog signal to digital signal, the sampling rate should be sufficiently high so that we have enough information about the signal and later on when that digital signal is processed. So, this digital signal is having enough information about the analog signal so that later reconstruction maybe possible. So, there is a theorem called Nyquist rule which is to be followed for this sampling.

So, this sampling in Nyquist rule so, it answers question of what sample rate is required. So, it is required that a sampling frequency should be at least twice as high as the

maximum frequency in the signal to avoid aliasing. So, maximum frequency of a signal in a signal means, in the in the analog signal for example, if there is a say music that is playing. So, there are several frequencies that are there

So, if you if you want to get a true picture about the music so, it you have to find out what is the maximum frequency in that music and the sampling rate should be twice that of the highest frequency. So, if you do not do that so there will be aliasing, so, later on the reconstruction maybe problematic so, you may not get the actual the original signal back in its true form.

So, the third point here is actually telling us that; what is the formula. So, this one the sampling frequency should be twice the signal frequency or you can say the maximum frequency in the signal so, this is the aliasing error. Another type of error that can come we have seen in the quantization process. So, quantization as we have discussed in the last class so, we the while converting from analog to digital signal so, we do not have all the levels of analog signals available for the um for to be so, converted into digital form.

And if I have got an n bit ADC, then the number of different digital pattern is 2 to the power n. So, if the total voltage is say V reference. So, this V ref divided by 2 to the power n so many different voltage levels are only possible to be recognized by the analog to digital converter. So, if this levels are named as a L 1 L 2 up to say l so, this quantity being equal to say k so, this L k.

So, between L 1 and L 2 there is a change in voltage. So, any signal which lies between L 1 and L 2 any analog signal. So, that is quantized as a equal to L 1. Similarly anything lying between L 2 and L 3 will be quantized as a L 2. So, naturally it introduces error. So, this error is the quantization error. So, if we want to reduce this quantization error so, we have to increase the resolution. So, if I want that this value of k should be large, then this number of levels should be large then what we have to do is that we have to. So, we have; so, there are 2 to the in this case there are 2 to the power n levels so, if we want that to be large than the value of n should be large.

So, as a result this is the voltage difference. So, this is not L k. So, this is L 2 to the power n so, L 1 L 2 up to L 2 to the power n. So, if I want that we I have large number of levels, then this value of n should be sufficiently large so; that means, that this converter will be more complex.

So, this is dependent on the ADC convert of the microcontroller. So, they have they very often. So, the underlying processor or the microprocessor or microcontroller so, they have got built in ADC, and this ADC, ADC for the ADC the resolution is fixed. So, we cannot change it so, error is dependent on that. So, these are the 2 sources of error in case of ADC applications.

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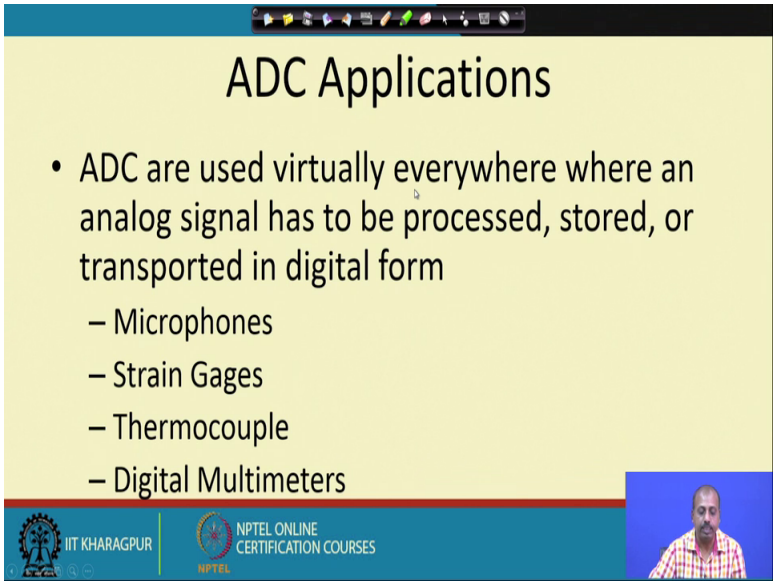

So, ADCs are used virtually everywhere, where an analog signal has to be processed stored or transported in digital form like microphones, strain gages, thermocouple digital multimeters. So, everywhere you will find some application of ADC; so, ADC.

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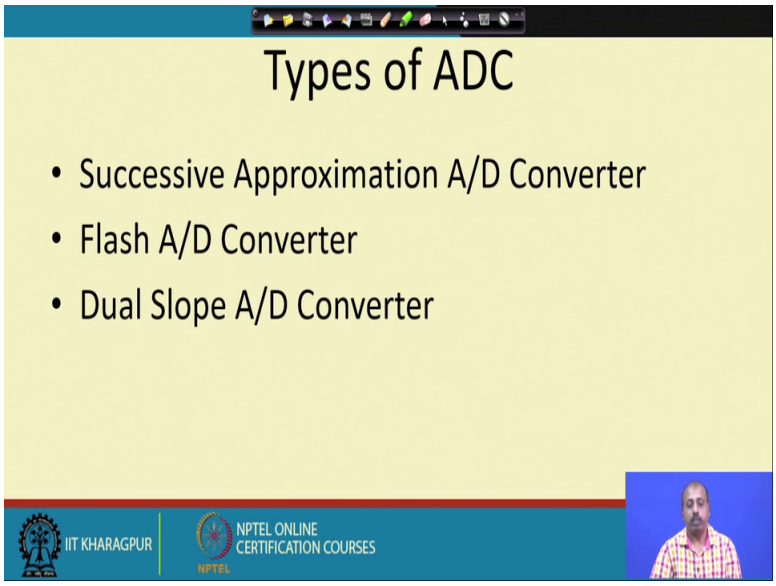

So, next we will be look into different types of ADCs that are available. So, of course, this is this least is not exhaustive. So, in fact, this analog to digital converter design by itself is a research area.

So, there so, even you today you can find lots of research papers on this analog to digital converters, but the purpose of this course is to understand the basic analog to digital converter designs. So, we will be looking into three alternative designs. So, one is known as successive approximation ad converter, another is flash type ad converter, another is dual slope ad converter.

So, successive approximation ad converter so, this is a serial converter. So, this we will try to approximate it will it will try to guess like what is the value of the analog signal, accordingly it will set some bits and then if the signal value is higher than the guessed value, then we will be further turning on some more bit. So, it will go like this, so, we will see how this is done.

So, in a step by step fashion so, if there are say n bit for an n bit ADC so, it will be doing in n steps by setting and resetting the bits. On the other hand this flash type ADC is they are pretty fast so, their. So, this it uses a number of comparators and these comparators they work in parallel. And accordingly this flash ADC will be setting this comparator outputs to high such that we can get the corresponding digital bit pattern to understand like what is the corresponding digital value. And this dual slope ad converter so, this uses

some reference signal and with respect to that it tries to see like what is the amount of what is the level of the given analog signal so, that way it is doing a duel slope ad converters.

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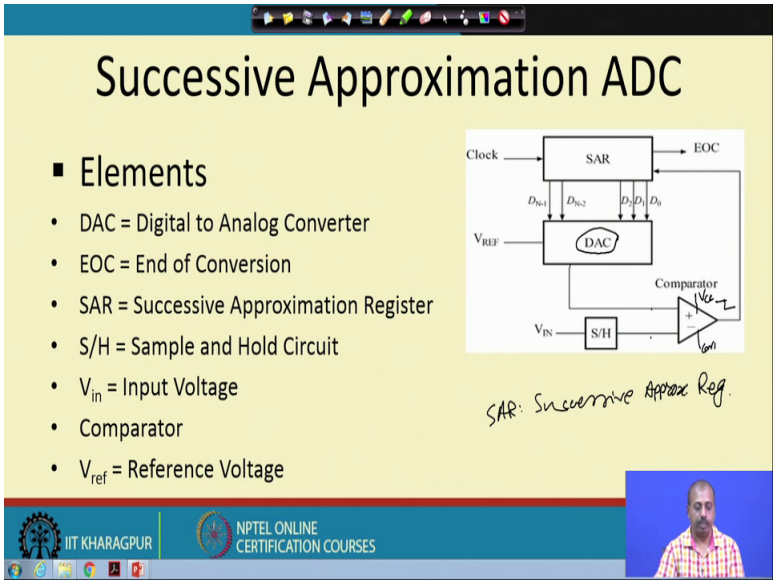

So, we will see them one after the other. The first one is the successive approximation ad converter. So, here what we have is that so, this is there is a successive approximation register this SAR. So, the SAR stands for Successive Approximation Register. So, this successive approximation register so, if I have got an n bit ADC then the size of this successive approximation register is also n.

So, interestingly it uses one digital to analog converter as a module in this ADC. So, while designing this ADC we need a DAC to be a implemented DAC to be available. So, the there are a few signals like clock signal means that in every clock. So, it will be doing some operation. So, this SAR registers so, it has got a clock so, that at every clock output at the clock active point, so, the bit pattern will be available on these lines. There is an end of conversion signal or EOC. So, this tells the outside world that the conversion is over.

And also we have got a sample and hold circuit. So, this sample and hold circuit the input signal is applied here. So, this will be sampler the value will be sampled and held for some time. It will be doing a comparison and then the comparator output will be fed to this SAR. So, that the SAR will be changing in the bits so, we will see it how it

changes. Now after n such steps this EOC signal becomes high, telling the outside world that for this current sample the conversion is over

So, whatever be the value of this D 0 to DN minus 1 so, that gives me the digital equivalent of the analog input signal V in fed here. So, you have got this DAC which is the digital to analog converter, end of conversion signal successive approximation register SAR the sample and hold circuit SH input voltage V in a comparator and a reference voltage. So, this comparator is simply an operational amplifier, which is connected in open loop configuration and you see that if this if this signal is more than the output from the DAC is more than V in, then this will be high a this will go to plus V CC.

So, if we assume that this has got supply voltage of connected to VCC and VCC and ground then what will happen is that. So, when we this value is higher than this then the output will be a high, and later on when this V in becomes less than a V in becomes higher than this DAC output then it will become a loop. So, that way this is a comparator that works in this is a operational amplifier that gives only 2 levels of output plus BCC and ground ok. So, that is and V ref is the reference voltage. So, how does it operate? So, let is try to understand.

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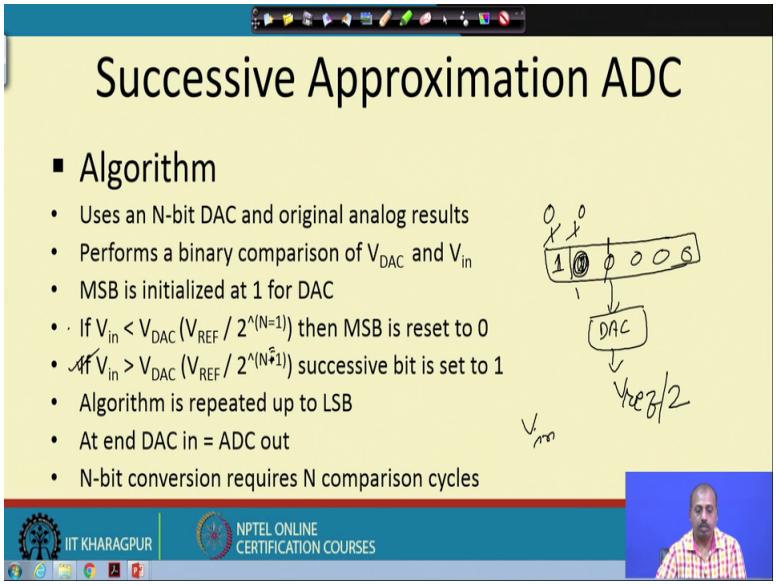

So, this SAR the successive approximation type ADC, it uses an N bit DAC and original analog results. And it performs a binary comparison between v voltage coming out from

DAC VDAC and V in. So, this is the VDAC coming out of the digital to analog converter. So, this is the VDAC and V in they are compared, and then this is compared. So, VDAC is compared with V in initially the most significant bit is initialized to 1 for the DAC

So, this successive approximation register what is done is that, the most significant bit that is d n minus 1 is set to one and rest of the bits are set to 0 as a result this DAC will be outputting a voltage, which is we are equal to V ref by 2. So, this V ref by 2 is compared with V in and if va V in is higher than V ref by 2 that means, this output will be this comparison output in that case a. So, V in is less than a VDAC divided by V ref by 2 to the power n 2 to the power 1 that is V ref n equal to 1.

So, then MSB is reset to 0. So, V if V in is less; that means, the value that we have guessed through this successive approximation register, that voltage value is higher than the V in value. So, as a result in the digital counts the MSB should not be 1 so, it should be 0 so, MSB is reset to 0. On the other hand if V in happens to be greater than V DAC which is in this case in this case it is n equal to 1.

So, it this actually if this comparison fails a V in is not less than V DAC so, this is say a bit confusing here. So, we should better say that if V in is greater than VDAC, where n equal to 1 n equal to 1. So, that means, in this previously we have said this MSB to be equal to 1 in the SAR register and all other bits were 0. So, with that we have got the output from this DAC which is V ref by 2 which is V ref by 2. Now if this V in happens to be more than V ref by 2 that is a second condition this condition is true.

So, this bit must continuous one now I have to try to set this bit ok. So, that is that is what is done. So, if V in is greater than VDAC then successive bit is set to 1. So, this bit I try I try with setting equal to 1 now, these 2 bits being 1 so, VDAC value will be even higher and then again the comparison will be done. So, if now it happens that this is less in that case this will be reset to 0 and then this will be turned to 1 so, it will go like this.

On the other hand if we if it is the initial point itself V in is less than V DAC. So, this bit is reset to 0 and we set this second bit to 1 and it proceeds like this. So, this way the algorithm is repeated till the least significant bit position at the end DAC input equal to ADC output. So, that so, their ADC output is that one and this for n bit we need some n comparison cycles for this purpose.

So, this way this conversion takes place.

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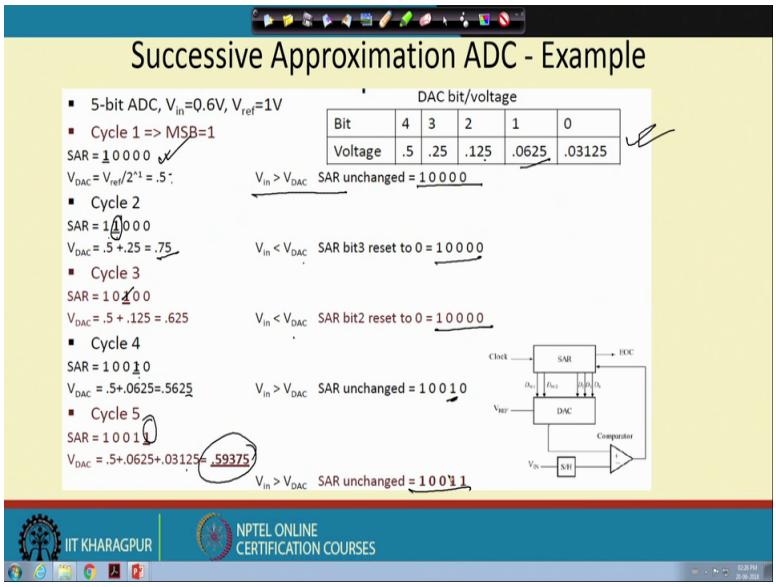

So, we have a got an example that will tell how this is going to happen. Suppose we have got a 5 bit ADC with V in equal to 0.6 volt, the analog voltage value is 0.6 volt and V ref reference voltage is 1 volt. So, in the in the first cycle MSB is set to 1. So, this is the 5 bit pattern that we have. So, this is the 5 bit pattern that we have so, there this MSB is set to one.

So, V ref or the VDAC value is V ref divided by 2 that is 0.5. So, when we compare 0.5 and 0.6 so, V in is greater than VDAC. So, as a result the successive approximation register content remains unchanged in the second cycle this SAR the second bit of the SAR is set. So, it becomes 1 1 0 0 0. So, DAC bit per voltage. So, if you for every bit, so in this table we have listed the voltage value corresponding voltage value.

So, in cycle 2 when these 2 bits are set so, 0.5 plus 0.25, so that will be the VDAC output so, that is 0.75. So, 0.75 is more than 0.6 volt. So, in this case V in is less than VDAC as a result this bit will be reset. So, it the DAC content becomes this SAR content becomes like this then we come to the third bit. So, third bit is turned 1 and third bits configuration is 0.125.

So, 0.125 is added. So, it becomes 0.625 again V in happens to be less than VDAC so, this bit will be this set so, we again remain at this position. In the cycle four we will be

trying out the fourth bit. So, this bit is turned one and then so, the contribution is 0.0625. So, it becomes 0.562. So, 0.5625 is less than V in. So, V in is greater than VDAC. So, this bits survives. So, this bits remains as 1; in the fifth cycle.

So, in the fifth cycle so, we turn on the LSB and then the contribution is added. So, the value becomes 0.59375 and since V in is greater than VDAC. So, this bit remains in change unchanged. So, this bit remains one only. So, this way through this so, through an iterative step; so the every individual bits from the MSB side is turned on and then if the content becomes if the VD DAC output becomes more than the input voltage input voltage then the bit is reset.

If the if the um DAC output is less than this input voltage then the bit is retained to 1; of course, for if the V in and this reference this VDAC. So, these 2 are equal then also we have to retain the value and in fact, in that case we do not need to proceed with further bits rest of the bits will always be 0, but anyway. So, that is not shown here as a case, but you can always do that exercise. At any point of time V in becoming equal to VDAC whatever be the SAR content so, that is the digital output and we can terminate the conversion process there though it is difficult to detect that situation. So, normally we do for all the n cycles and get take the DAC output after end cycles only.

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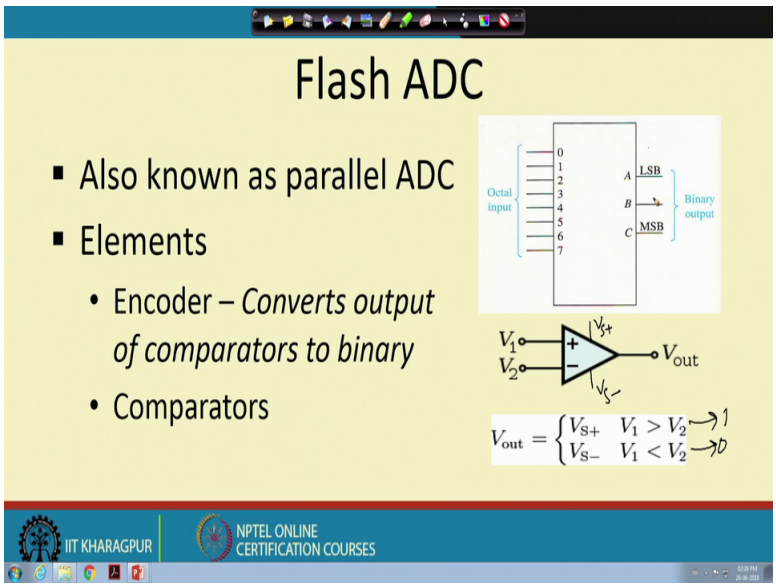

So, next we will be looking into flash type ADC. So, in flash type ADC so, as the name suggests the conversion is done in a flash. So, so all the all the bits are set simultaneously and this is a parallel type of ADC.

So, the elements that we have here is encoder that will convert output to of comparators to binary, and we have got a set of comparators. So, any comparator is like this. So, the if this is a comparator circuit, so, you see this V 1 and V 2 so, these 2 are input to the comparator and so, it has got VS plus and VS minus as the supply voltages. So, this is VS plus and a Vsaturation plus and V saturation minus we tell that way.

So, if this V 1 is greater than V 2 then this v out is equal to V s plus if V 1 is less than V 2 then v out is equal to Vs minus. So, that is this is basically logic high and this is logic low. So, these are the 2 things now what is done? We apply some. So, this is the encoder circuit; so encoder circuit. So, it is an 8 is to 3 8 by 3 encoder. So, if you give an 8 bit pattern here. So, it will be converted into 3 bit binary output.

So, we will see how it operates.

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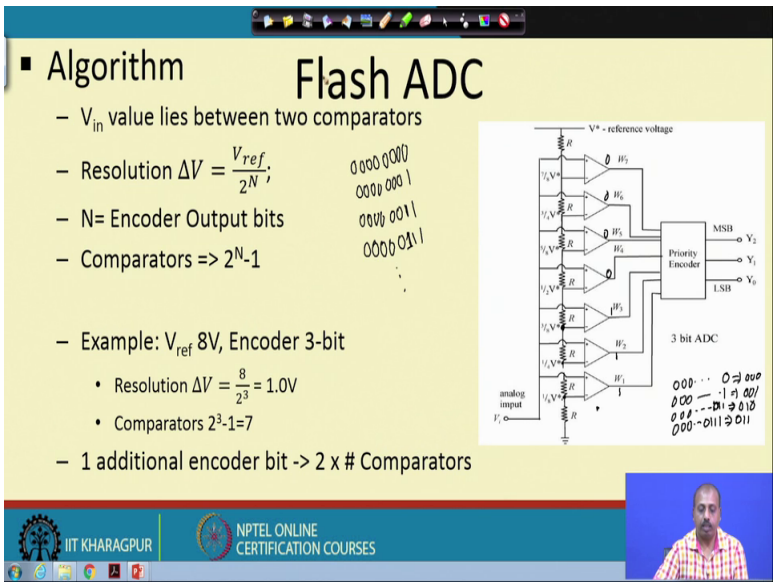

So, in case of flash type ADC what is done? We have got s number of comparators ok. So, this is an 8 bit ADC. So, this V in value lies bit; so V in. So, if you look into the circuit so, this is the reference voltage V star and from this. So, we have got a series of resistance so, we have we have connected 8 such resistances 1 2 3 4 5 6 7 8 resistances.

So, if you try to measure the voltage at this point. So, this is equal to one eighth v one eighth of this V star similarly at this point. So, this is 2 eighth of V star that is one fourth of V star. So, this point is three eighth of V star like that. So, this V star voltage the reference voltage we have divided into a number of intermediary values one eighth V 1 fourth V 3 eighth V up to seven eighth v.

And the input voltage is applied to all this comparator simultaneously and this voltage is also applied. So, this first this comparator this is for the LSB so, this will be doing a comparison. So, it depending upon the voltage value that you have given V i value that you have given. So, this comparator output may be 0 or 1 depending upon the voltage the whether the voltage is more than that the voltage that we are getting here.

So, if the V i is greater than this one eighth V star, then this bit will be set to one similarly at this point if it is more than one fourth V star then this bit is also set to 1. So, it may so, happen that at this point it becomes low V in becomes low. So, this becomes 0 so, rest of the bits are 1 and all this bits will be 0 from that point onward.

So, then it goes into a priority encoder. So, priority encoder it will see that these three bits are 1. So, accordingly it will be during an encoding and it will be producing a 3 bit output. So, how many bits are 1? So, this least significant three bits are 1 so, you can say the count value that we have is basically. So, this is. So, if you if you think in terms of count values.

So, the first count value is 0 0 0 0 0 so, that is outputted as three zeros then 0 0 0 01. So, that will be outputted as 001 then 0 0 0 0 then. So, it the one will start at some point and then it will continue. So, if you get after that if you get the pattern which is 2 ones. So, this is 2 output will be 0 1 0 and it the example that we have taken.

So, here it is 111 so, this is then this bit is the bit before that is 0. So, this is coded as 3. So, it is it will be coded as 0 11. So, this basically counts. So, at this output of this comparators. So, we have got the count value, but in some unary number system you can say. So, it can produce all 0 to all 1, but the pattern that it can produce is 0 0 0 0 0 0 0 0 then 0 0 0 0 0 0 0 1then 0 0 0 0 0 0 1 1 then 0 0 0 0 0 11 1 so, it can go like this ok.

So, this 1 so, once a bit becomes one the bits towards the right of it must be 1 and the bits towards the left of it must be a 0. So, it is important to find out where how many ones are

there. So, accordingly this parity encoder circuit it can do a encoding and output the corresponding sequence number.

So, in this particular example we have got V ref equal to 8 volt and that the 3 bit encoder. So, resolution is given by 8 by 2 to the power 3 that is 1 volt ok. So, number of comparators needed is 2 to the power N minus 1 so, that is 2 to the power 3 minus 1 that is 7 so, we need 7 such comparators and. So, one additional encoder bit will be a. So, if we if we say that instead of a 3 bit instead of having 3 bit ADC, we will take a you will design a 4 bit ADC then the number of encoders will become 16.

So, every additional encoder bit number of comparators will double. So, that is the cost of flash ADC so, the number of comparators needed is pretty high, but this conversion is immediate. So, this whenever this input is given accordingly this unary pattern will be set here, and this priority encoder will encode it into one of the um binary pattern. So, that way this flash ADC works

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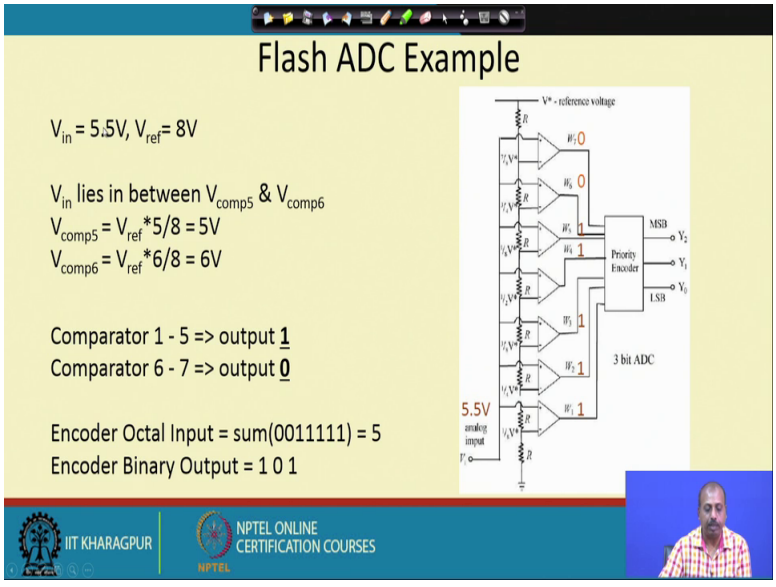

So, another example suppose V in equal to 5.5 volt and V ref equal to 8 volt; so V in lie so, 5.5 volt. So, V in will lie between V comp 5 and 6 ok. So, this is. So, the bit pattern will be like this. So, this is between 5 and 6 so, up to this. So, this a seventh and eighth bit so, there are sixth and seventh bits. So, they will be 0 and the up to bit number 5 they are all 1.

So, then because V comp 5 is V ref into 5 by 8 that is 5 volt and v comp 6 is V ref into 6 by 8 that is 6 volt. So, comparator 1 to 5 will be equal to 1 comparator 6 to 7 will be equal to 0. So, this is the unary coding that I get; so 0 0 111. So, that there are 5 ones in it. So, the binary output of this parity encoder is 101 so, that is the operation of the flash ADC.

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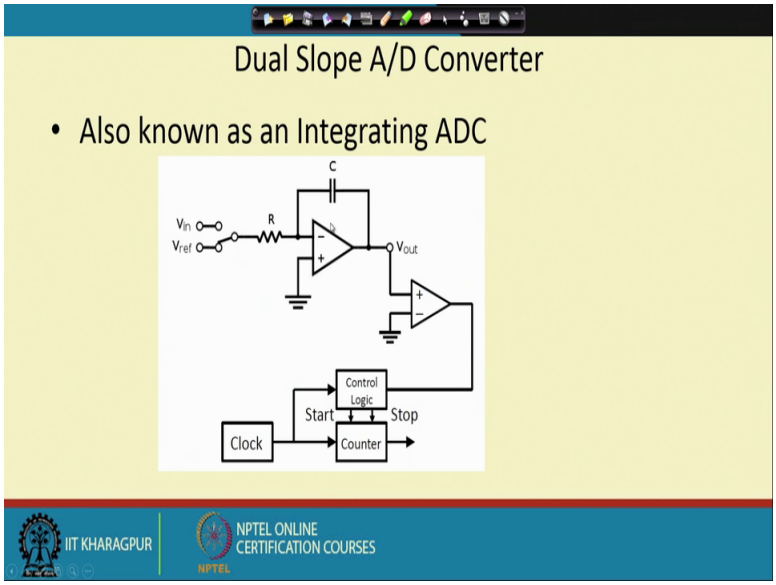

Now, next we will be looking into another analog to digital converter, which is known as dual slope analog to digital converter or dual slope ADC. So, basically the circuit is like this. So, there is a reference voltage and this um ADC is this capacitor is charged for some time. And then it is connected to this supply voltage and they this input signal and then we try to see in comparison to this how much time this capacitor needs to get discharged or charged so, like that.

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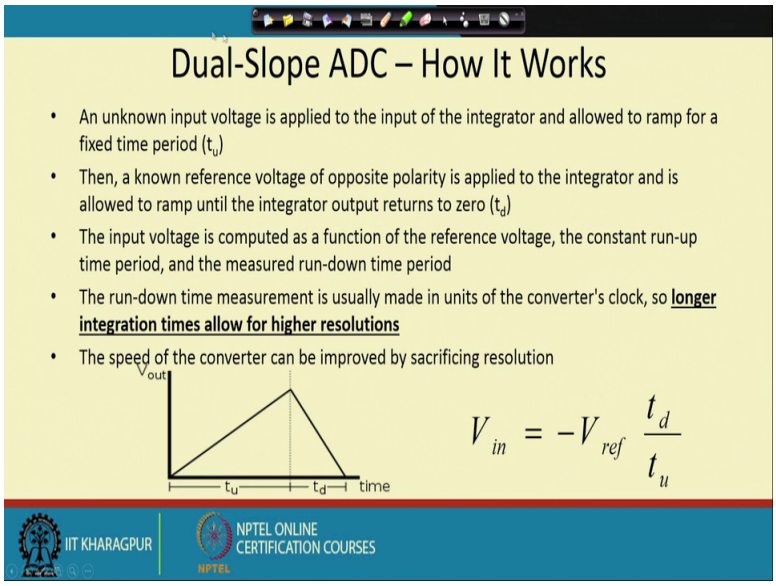

So, I will explain it how does it work. So, an unknown input voltage is applied to the input of the integrator and allowed to ramp for a fixed amount of time tu. So, initially sorry so, initially the input voltage the V in is the input voltage. So, it is connected to this, and this circuit is kept on for some amount of time. So, that is controlled by this control logic. So, this gives this start and stop pulses.

So, this control logic will be telling the will be noting down the time and for tu amount of time this which remains in this position, as a result this integrator output. So, this is an integrator configuration so, integrator output will be increasing like this. So, integrator output increases like this. So, it is charged it is allowed to ramp for a fixed amount of time tu. Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to 0.

So, at this point what is done? So, the sorry at this point this switch is taken down to the V ref position and it is ensured that the polarity of V ref is the inverse of polarity of V in then when you do this so, capacitor will start discharging ok. So, because this is a negative voltage so, it will if the V in is positive V ref is negative so, it will start discharging. So, we see the depending upon the value of V ref so, and the amount of charge this capacitor has. So, it will take some amount of time to get discharged.

So, this is happening here that a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to 0 so, this is

the time td. The input voltage is computed as a function of the reference voltage the constant run up time period and the measured run down time period. So, these values are. So, how is it computed. So, V in is then given by minus of V ref into td by tu.

So, minus comes because V in and V ref are of opposite polarity and this td by tu. So, this ratio will tell me; what is the ratio between v V ref and V in so, that is how we measure the input voltage. So, this run down time measurement is usually made in units of converter clocks. So, longer integration times will allow higher resolution. So, then what is what is happening is that we in this circuit we have got a counter. So, we count the amount of time for which it has to come down. So, the time needed for td; td time is fixed the counter value will be fixed the tu time will be computed by looking into this counter when this capacitor is discharging.

And then this td tu ratio will be computed by this control logic and it will be telling; what is the corresponding bit pattern. So, that part is not explicitly shown this control logic will finally, output the bit pattern depending upon this td tu ratio.

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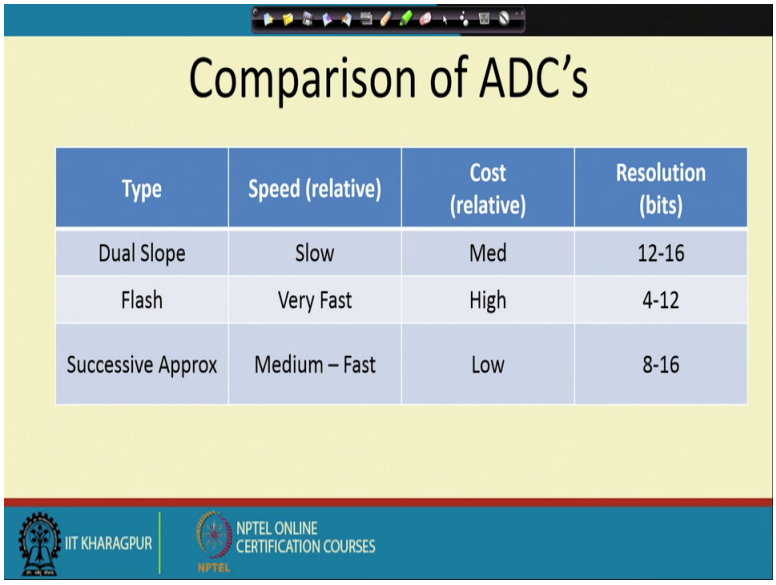

So, if you compare between the ADCs, then this dual slope ADCs are a bit slow flash ADCs are very fast and successive approximation are medium fast cost dual slope medium cost flash ADC high cost, and this successive approximation is low cost resolution dual slope is 12to 16 bit flash ADC is 4 to 12 bit and successive approximation 8 to 16 bit.