Digital Circuits
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Lecture – 39
Data Converters
(Contd.)

So, this ADC process, this analog to digital conversion process. So, as I said the first step is the Sampling and Hold part.

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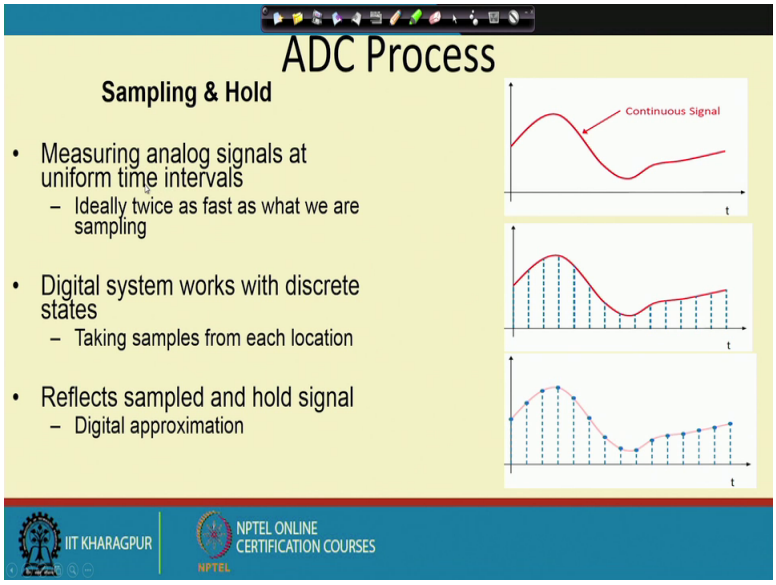

So, it is for measuring analog signal at uniform time intervals. So, ideally, it should be twice as fast as what we are sampling. So, this is, this comes from the Nyquist sampling theorem which says that if you are sampling some analog signal at to and later on you want to reconstruct it from the samples. Then, we need at least the sampling rate should be at least twice the frequency of the input signal.

So, you can look into that reference in the communication books the signal processing books. But anyway, so if we follow by following that property, so ideally, we should do this sampling twice as fast as what we are sampling. So, digital systems work with the discrete states. So, we it takes the samples of each location like this is the continuous signal that we have. So, if this is taking as samples at this steps so, we get the sampled,

we reflect the sampled and hold signal. So, this is the thing that we get. So, you get these values at these points. So, this blue dots, so these are the sampled values that you get

So, for reconstructing the signal, so we have to start with this and do the reconstruction, but reconstruction is not the objective of this particular course. So, we would like to see what is the, we would like to convert this values into some digital values may be at the receiving end. So, once it is digital values are received, it will be converted back on to analog and finally, it has to be it has to be converted into continuous signal to get back the original analog signal. So, that is why the cond this the sampling should be at least twice as fast as the input signal frequent, input signal frequency

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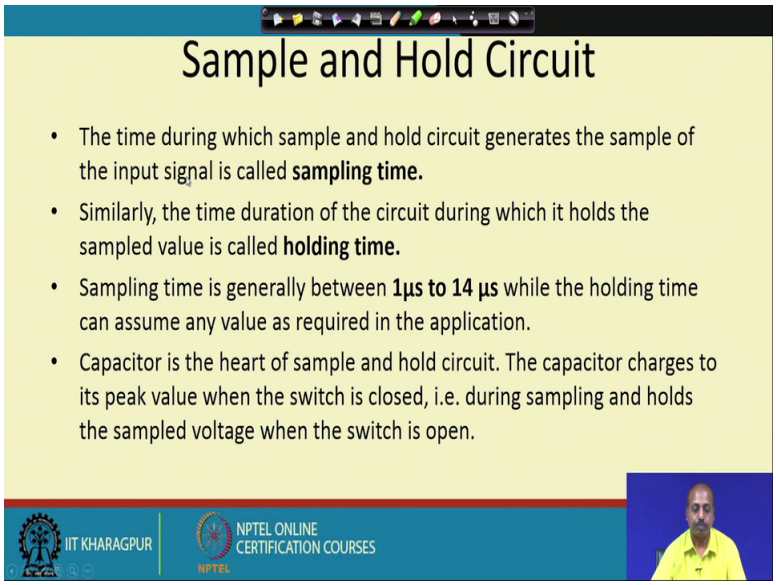

So, we will look into this sample and hold circuit. So, time during which the sample and hold circuit generates the sample of the input signal is called the sampling time. So, as the name as the, has got two parts sample and hold; so, naturally, so it has got two function; one is the sample, sample, function. So, the circuit gets the sample from the input signal and then there is a hold time the time duration of the circuit during which it holds the sampled value is called the holding time. So, we have got sampling time and holding time.

So, typically the sampling time varies between 1 microsecond to 14 microsecond and the holding time can assume any value as required in the application; So, normally, the samplers that we design, so they have got 1 microsecond to 14 microsecond sampling

time. So, capacitor is the heart of the sample and holds circuit because once you get the sample, after that the sample has to be held for some time and capacitor is the instrument that we have, capacitor is the device that we have that can hold the value electrical voltage or current value for some time. The capacitor charges to, it is peak when the switch is closed and during that is during the sampling period and holds a sampled voltage when the switch is open.

So, that is the behavior that we will explained that capacitor will be charge when the sample and switch is closed. So, it will sample the input. So, capacitor will charge to the value equal to the peak value that you get on the analog signal and then it will be not leaky. So, during the hold period should be the capacitor should be able to hold the charge for the hold period. So, that is how the sample and holds are it is expected to behave.

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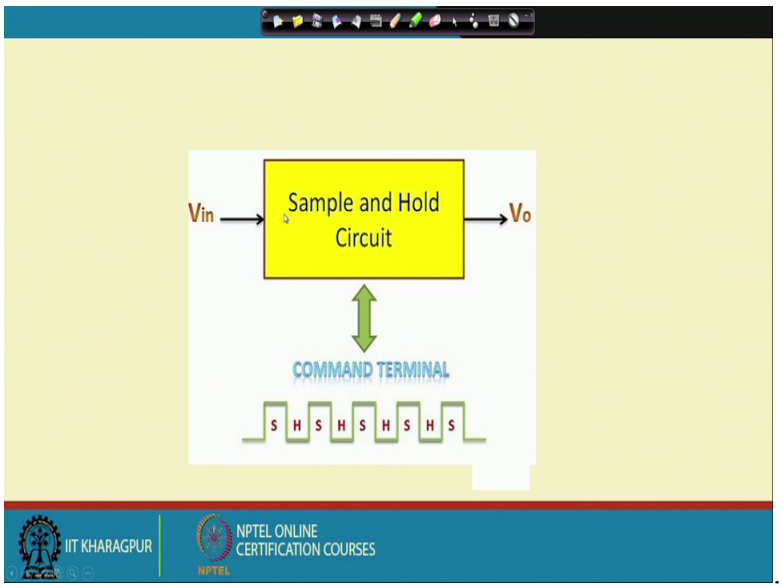

So, pictorially you can represent it like this. So, as if this input voltage V in is coming and there is a command terminal for the sample and hold circuit. So, it a so when this signal is high, so this is the sampling period and when the signal is low, this is the hold period. So, it alternate between sample and hold period, sample and hold like this. So, during the sample periods this V in value gets connected to this V o and during this hold time it is expected that the sample and hold circuit will be hold the V o value. So, it will not change ok. So, then by means of there has to be some capacitor here which will hold

the value when this sampling say when the sampling interval is on, then the capacitor gets charged, so that during this hold time the capacitor will can provide the last sample value in the V o line. Then again, the next sample period sampling period come. So, again the next sample value whatever is coming, so, accordingly the capacitor will get charged to up to that point. So, this way the sample and hold circuit is expected to behave.

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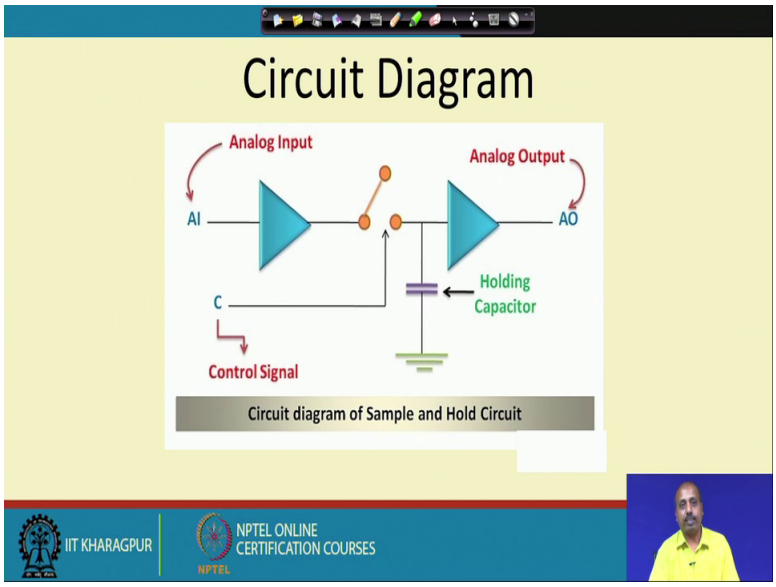

So, how do we make such a sample and hold circuit. So, the basically, we have got this analog input. So, that is amplified because of this, that will be ensuring that the noise and all those effects to be taken care of and there is a control signal C which will control the closing and opening this particular switch ok. So, this is the, so when this when the sampling period is on, so the switch will be taken to this position as a result this analog signal will be coming here. So, it will be charging this holding capacitor. And then, when this analog signal when the control signal is in the hold time, then sig switch will be open as a result this capacitor does not have any discharging path. So, it will hold this value for some time.

So, this, so this leakage of this capacitor should be large enough, so that it should be small enough, so that this charge does not change the significant the, voltage does not change significantly over the hold period. And then, this value will be available at the analog output. So, then this analog output value which is basically a sampled version of

this analog input, so, that will be used by the analog to digital converter circuit to convert to digital value.

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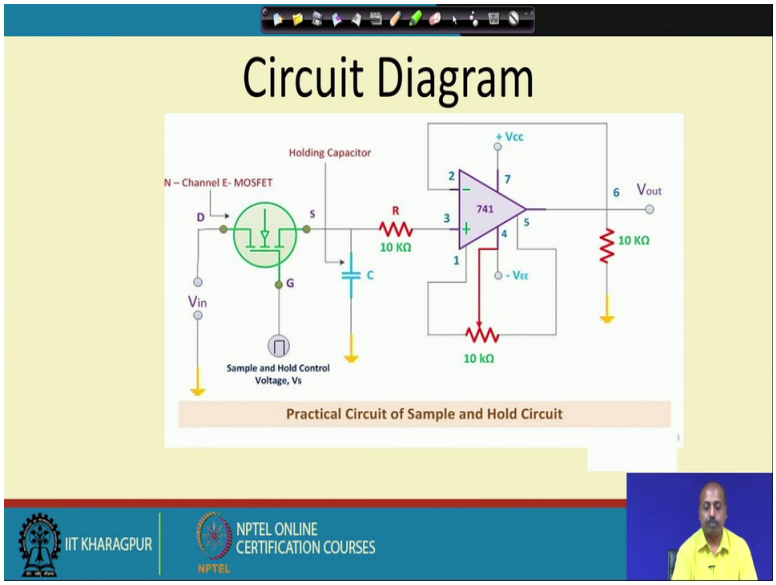

So, this is a typical circuit that we have. So, practice circuit, so we that uses one n channel MOSFET for this n channel enhancement mode MOSFET for this conversion. So, this gate of this MOSFET, so this is fed this sample and hold control voltage. So, this is basically a clock signal you can say that contains a during the on time of the clock period, the sample is the sample is collected and during the off time of the clock period, the sample the input is not disconnected from this sampled value. And, so that way this sample can input can reach the point s only when this gate is high

So, this, this transistor ensures that, so this is basically when this sampling period is on. So, this G is equal to 1, 1. So, this V in that you connected to the V d, the drain terminal of this n channel MOSFET. So, the voltage available at the s point or the source point and then that will be charging this capacitor, it will be charging this capacitor. So, it will be capacitor will get charged to the V in value.

And then, when this sampling hold period signal goes low then, this transistor is now open. So, this is the it is the, it is not connected we gets disabled. So, as a result this capacitor will not have, this capacitor will not be charged any more. Then it is connected to this voltage follower type of circuit where it will be it will be transferring this voltage

value to this point and the you will get the sampled value at V out. So, that is the operation of the circuit ok. So, this is the sample and hold circuit.

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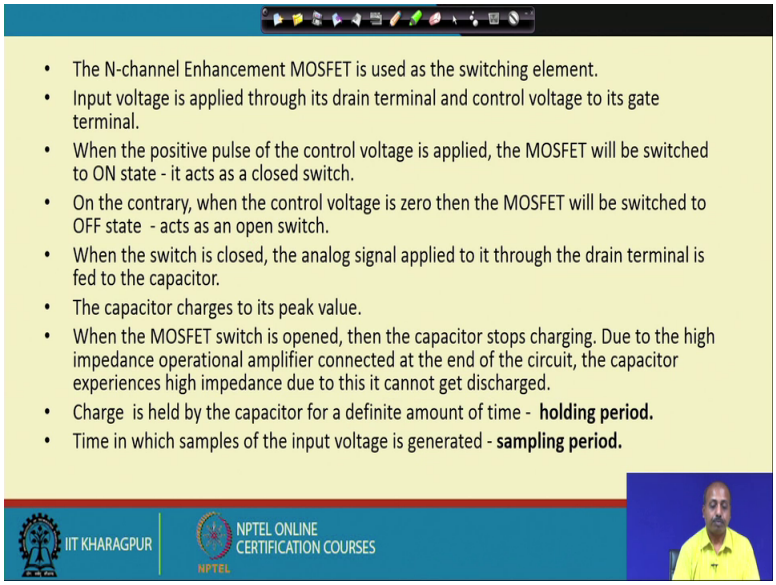

So, overall operation is like this, the n channel enhancement MOSFET is used as the switching element. Input voltage is applied through it is drain terminal and control voltage to it is gate terminal. When the positive pulse of the control voltage is applied the MOSFET will be switch the to on state and it acts like a closed switch. The on the contrary, when control voltage is 0 the MOSFET will be switched to off state and act as an open switch.

So, that is the behavior of the MOS switch that we have seen. And when the switch is closed, the analog signal applied to it through the drain terminal is fed to the capacitor. The capacitor charges to it is peak value whatever be the input voltage coming. So, it will charge to that and when the MOSFET switch is open, then the capacitor stops charging and due to the high impedance operational amplifier connected at the end of the circuits, the capacitor experiences high impedance due to this, it cannot get discharged.

So, the circuits, so you see that this is connected to this op amp and op amp resistance is, ideal op amp is infinity, so, practical op amp also this into resistance will be infinity. So, close to is will be very high. So, as a result, the capacitor will not get chance to discharge much excepting some amount of leakage.

So, charge is held by the capacitor for a definite period of time amount of time. So, that is called the holding period and time in which samples of the input voltage is generated is known as the sampling period. So, we have got a sample operation and a hold operation.

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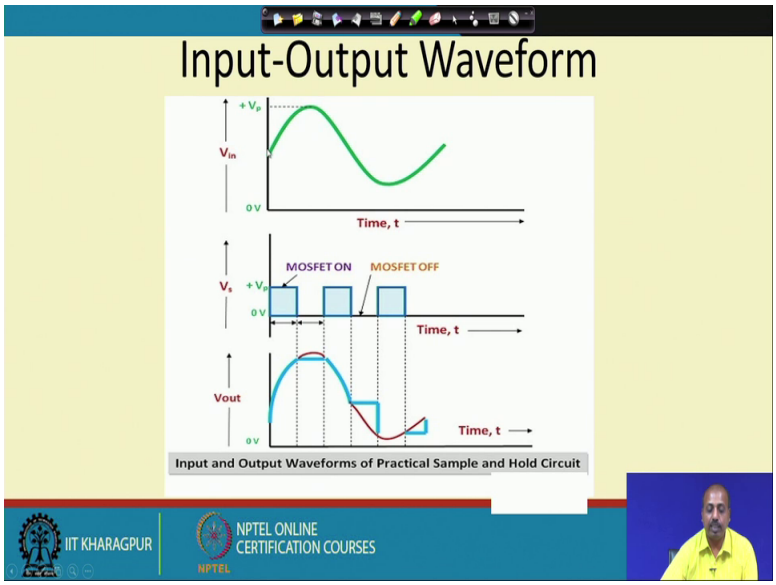

So, pictorially, if this is the input voltage that we have and this is the sampling control signal that we get, so the this is this time this MOSFET is on and this time it is off again, this time it is on this is off. So, during this time thus capacitor gets voltage like this. So, it charges to this value during hold time. So, it holds the value. So, it holds the value like this and then during this next on period of the MOSFET. So, this capacitor will get this input the capacitor will be getting this input signal connected as a result it will at the end of this sampling period, the capacitor will hold this value and it will hold this value till the next for the entire next holding period.

Then, the capacitor will again the next sampling period will come and capacitor will be looking into the next sample value next signal value. So, it will go like this. So, in this way, so again it since the, this portion and it holds the value. So, there is a problem in the mistake here actually, this portion of the diagram it should shift to this. So, this is this blue line, it should start form here and go like this; so, that that is not shown here correctly.

What I mean is that because at this point, it has got this part. So, it will be it should be like this. Then it should be after that it will be holding this value. So, it will be going like this. So, this part should be this part is missing. So, this should this should be there.

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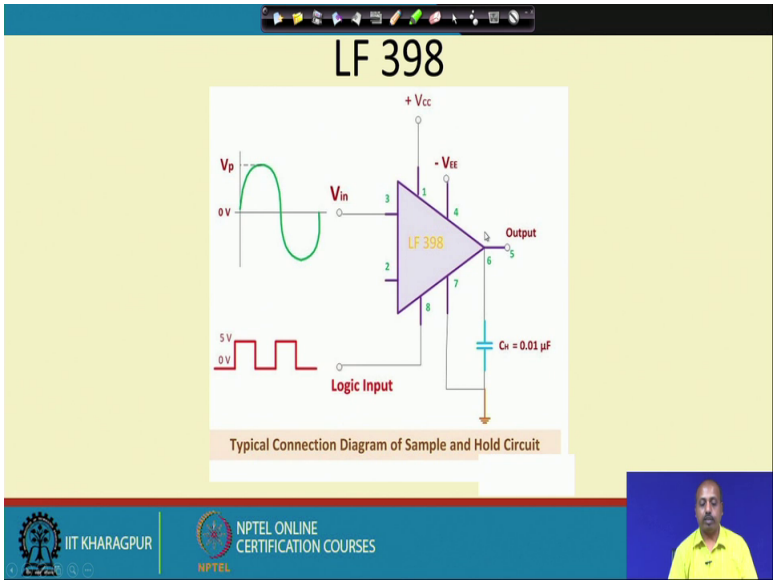

Anyway, so next will be looking into how the circuit can be made to operate it is a practical chip like LF 398. So, this is a chip that is available, we using op amp and the. So, where this is a sample and hold circuit. So, here this capacitor has to be connected externally, the holding capacitor has to be connected, but rest of the thing are already there. There is a terminal to give this logic input which is the sampling signal and then the samp, the samp signal to be sampled is applied to this pin number 3 and then VCC, VEE those connections are to be there and this capacitor has to be connected externally like this. So, this way we can have this LF 398 connection for this which is a sample and hold circuit.

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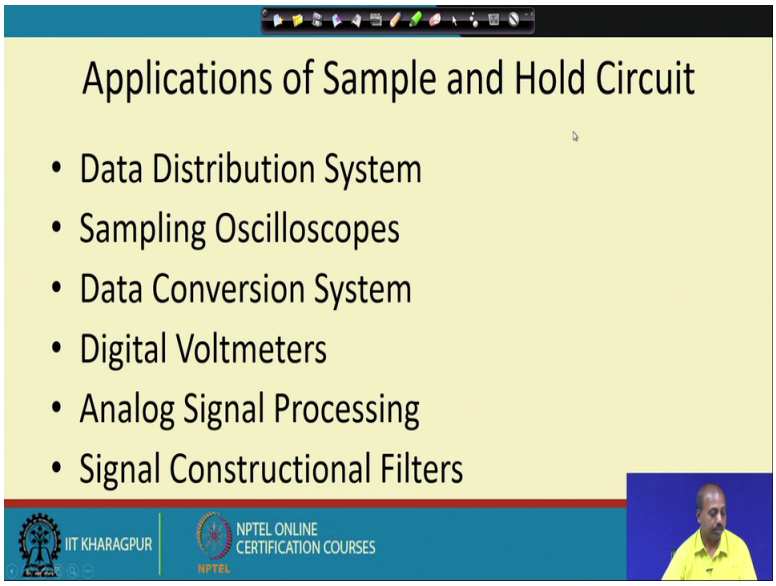

Now, where are you going to use this sample and hold circuit. One application is the data distribution system, so where you need to distribute some analog data to various places, so you first collect the analog data and for collecting the data. So, you have to go for a sampling and hold type of circuit, so that we get the analog signal samples collected then sampling oscilloscopes there are some oscilloscopes where we need to where the input signal is occurring only ones and we need to display that signal. So, for displaying that signal, so it has to collect the samples from the input signal; So, they, so this sampling oscilloscopes, so they collect the input signal samples and then reproduce it on the on the screen.

Then, the Data Conversion System, so this, so one format to another format or one level to another level if you want to change, then you have to do it. Then digital Voltmeters, so this is another case. So, you have got this analog values available from the from some circuit, the voltages have various nodes and that is converted to be to be that that is to be converted to digital value. So, you need a need an analog to digital converter. So, at the first stage of that conversion process we have got the sample and hold circuitry.

Analog Signal Processing will definitely need this ADC because this analog signal has to be converted into digital form and for doing the conversion at the very fast step you need a analog to digital converter. Then Signal Constructional Filters, there many we need to

construct many signal and accordingly some filters are necessary. So, these filter design, so they also use this sampling and hold circuitry.

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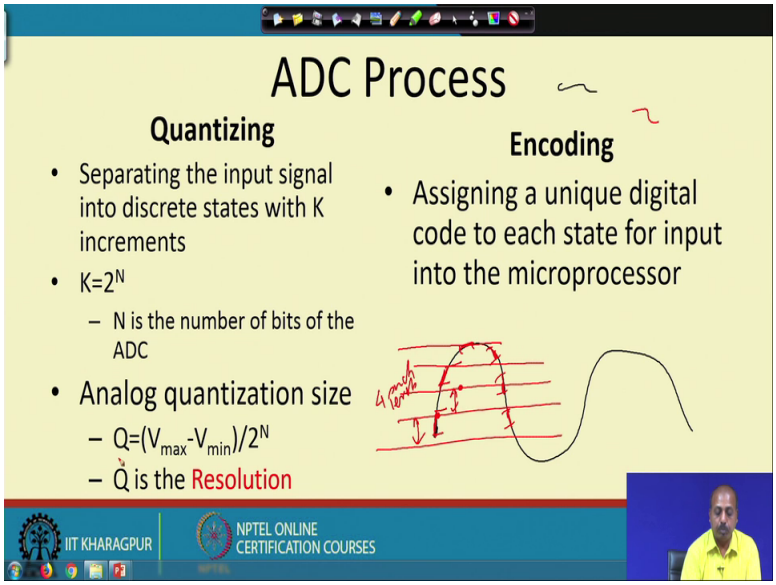

So, next once we have done this sampling and some this sampling and hold operation, so we have got the analog samples of data available now that is to be converted to digital value and that goes into goes through two stages; one is called quantization another is called encoding. So, what has happened is that, after you have sampled and analog signal. So, you might have, so if this is the sinusoidal signal that you have that is there may be you have got the samples like this. You have got samples, suppose after doing the sampling. So, we have got the samples like this. So, this portion I have sampled, again in this portion I have sampled, again this portion I have sampled. So, we have got so many voltages.

Now, this capacitor accordingly has got charge to say this value, this value, this value. So, it has got charge to all these values. Now, while outputting to while converting to digital, so my converter may not have so many levels, may not have the capacity to converts so many levels. So, it might have capacitor you convert only say, this is the maximum value may be in this range. So, it may it the converter may be able to produce only four such, may be able to consider only four such levels.

So, if it is that, then I can say that this whole thing is divided into four such levels. So, whatever falls in this region for that, it will be outputting this level. Similarly, whatever

false in this region it will be outputting this level. So, that way it goes ok. So, I can say that we can separate this input signal into discrete states with k increments. So, at k equal to 2 to the power n, n being the number of bits of the ADC, so this quantization size q is given by V max minus V min divided by 2 to the power n. So, and this is known as the resolution of the this is known as the resolution of the ADC, ok.

So, this is, so this is like this thing. So q, so this q is given by V max minus V min divided by 2 to the power n. So, if you change one if you want to if the, so this minimum change that it has to that it the that it can do is basically given by this q. So, if you want to get a digital change in the digital output for a voltage change less than this, so it is not possible. And then, comes encoding which will be giving some unique code to individual stages.

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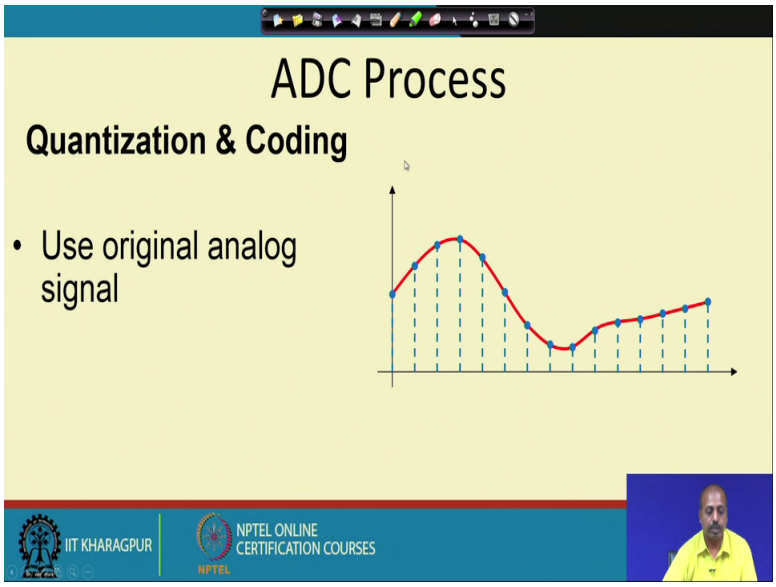

So, we will see some ah case then it will be more clear. So, quantization, so, what we have done in the ADC process. So, this red signal is the original analog signal that we have and then after the sampling and hold operation, so we have we have sample data at some periodic intervals of time and accordingly we have got these samples. So, at this point when I sampled, I got this value. At this point, I got this value. At this point, I got this value. So, these are the analog sample values that I have got at different time instants, fine.

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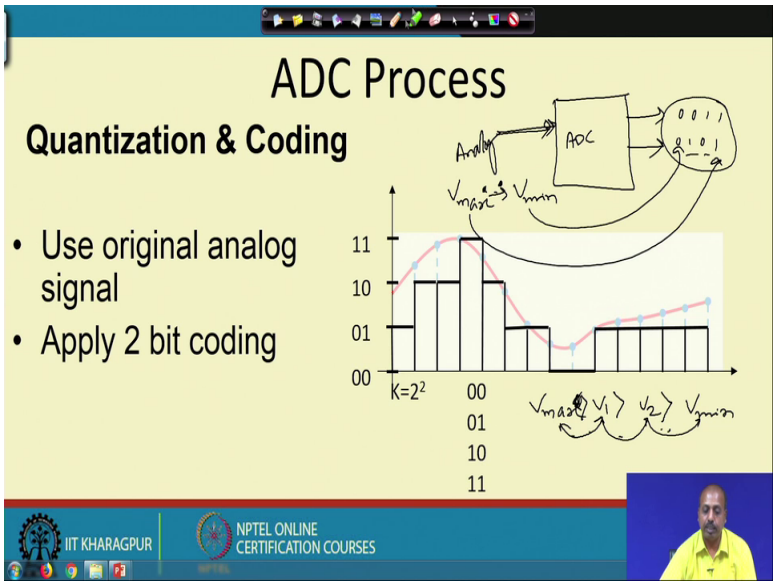

Now, next what is done is that this quantization is applied. Suppose, I have got this 2 bit coding, so 2 bit coding, so I have got four possible levels. So, if this see if this is my ADC, if this is my ADC and it has got 2 bit as output and if this is the analog voltage that I have, so this is the analog voltage that is coming. Then, depending upon analog voltage, so this ADC can either say 0 0, 0 1, 1 0 and 1 1. So, it cannot produce any other input combination. Had it been a 3 bit ADC, then it can produce 8 such situa 8 such alternatives. But with 2 bit ADC, so it can be only this 4 4 possible alternatives.

Now, if your analog input voltage is in the range say V max to V min, V max to V min, then for V min it can output a this 1, for V max, it can give this 1 1, but in between it cannot represent any arbitrary voltage now, all arbitrary voltages because there are only two more levels available. So, what I have to do is I have to decide two points in between which it will be representing. So, finally, I have got this V max, then value V 1 which is slightly less than V max, then we have got V 2 and then we have got V min with the relationship that sorry, with the relationship that V max is greater than V 1, V 1 greater than V 2, V 2 greater than V min.

Now, for all practical purposes what we would like to do is that this distance between this V max and V 1, similarly V 1 to V 2 and V 2 to V min, they should be same ok. So, this distances, so basically whatever input range I have, so, I need to distributed equally between all this points all this say 0 0 0 1 1 1 0 1 1 1, these outputs.

So, I can say that if this is my if this is my input range, then, so from, so this is my total input range the. So, this is the minimum value that the signal can produce and this is the maximum value that the signal can produce, accordingly I can I can say that ok I will be my digital output only 4 level. So, I divide this entire range into 4 levels. So, for 0 0, it will be outputting the minimum value; for 1 1, it will be outputting say this level. Now, in between, I put this 0 1 and 1 0 at some regular intervals. So now, if you consider the sample, so initially initial sample was somewhere here.

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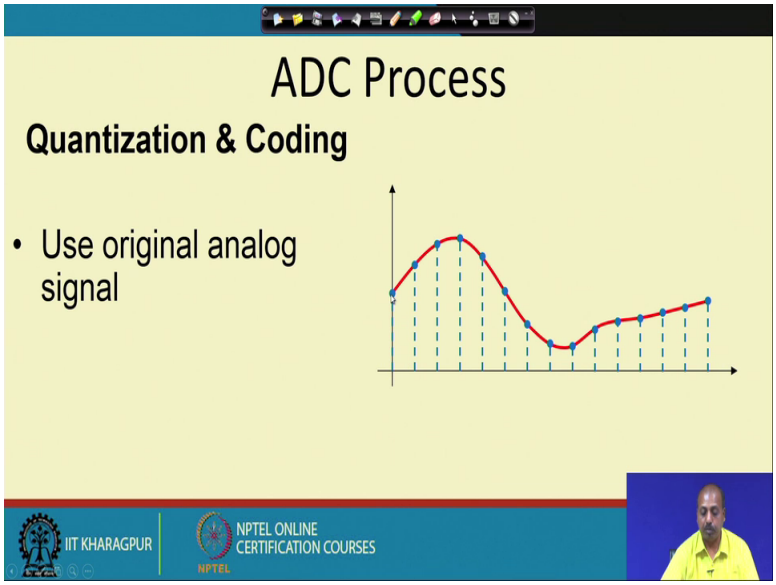

So, for that I can say that it is more than, so it was to the initially sample was here actually in this diagram. So, this is between 0 1 and 1 0. So, it has not reached 1 0. So, I output is 0 1. The second sample that I had is somewhere here. So, that is between 1 0 and 1 1. So, I output 1 0, similarly the third sample is also here. So, there I will show a output a 1 0 because it is not more than 1 1.

The next sample is more than 1 1. So, it is 1 1 is outputted, then the next one next sample is is between 1 1 and 1 0 as a result the output becomes some this level 1 0 and it goes like this. So, these are the voltage levels that I have corresponding to this four possible digital outputs. So, this is the original analog signal is used and accordingly, we have got we have produced like this. So, in reality what has happened is corresponding to this analog voltage we have outputted say this much. Similarly, for this analog voltage we have outputted this much. So, that way, so this quantization process, so it is dividing this,

it is dividing this range into a number of sub ranges and the this distance, so this distance between the actual value and the value outputted by the quantizer. So, this is called the quantization error. So, it introduce a some error into the conversion process. So, this is the 2 bit encoding that we can do for this analog to, so this is by the quantization process.

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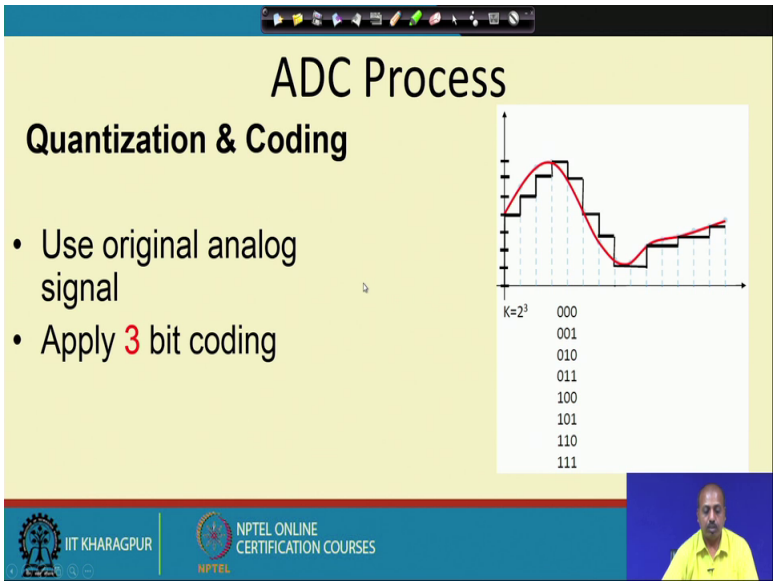

So, if I have got 3 bit encoding, then you see the same signal. So, now, I can have eight possible alternatives so, 0 0 0 to 1 1 1, now you see say. So, I can divide this range into 8 possible levels; now this 0 0. So, initial signal value was here. So, I can make it a more faithful representation. Similarly, second sample that I got is somewhere here. So, I make it this one. So, you see that this signal that I output by means of by the quantization process. So, this much more faithfully represents the situation compare to this.

So, that way if I have got more number of quantization levels, then the signal will be approximated better by the quantizer state naturally. So, if I increase the number of quantization levels, then the number of bits needed for encoding will also increase. So, this ADC's number of bits needed will also increase. So, in this case we have got this 3 bit ADC. So, we can we need eight possible steps. So, if you want to make it even more fine, then you have to go for say 16 number of levels. So, that will require 4 bit encoding. So, that way the cost of the ADC will go up as the quantization number of quantitation levels you are going for high.

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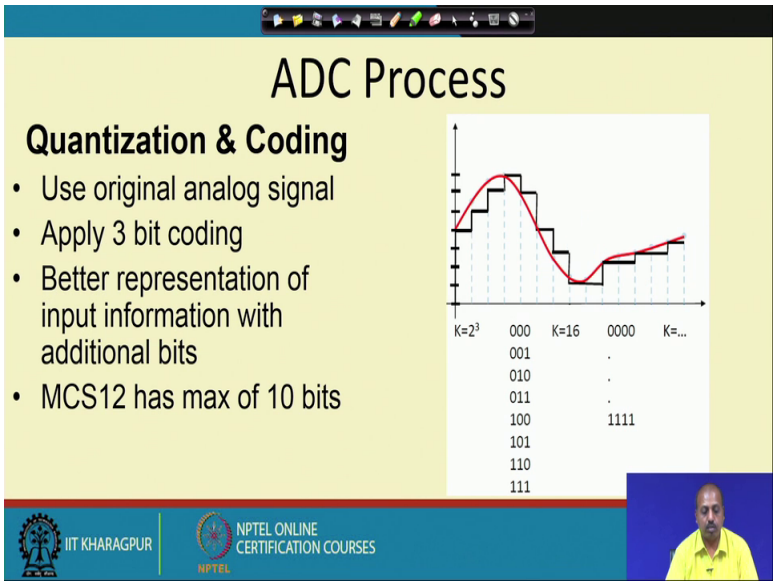

So, this is basically the thing that is we have got this K equal to 2 to the power 3. So, if we go for K equal to 2 to the power 4 then, we can go for even better approximation. So, like this. So, use original and analog signal apply 3 bit coding. So, better representation of input information with additional bit. So, MCS 12, so this is one ADC that has got a maximum of 10 bits, so that is quite fine; so, we have to it has got 2 power 10 possible steps. So, here actually in this case, we show the situation where K equal to 8 and it changes from this point to K equal to 16 as a result we got a better representation, so of the sample values.

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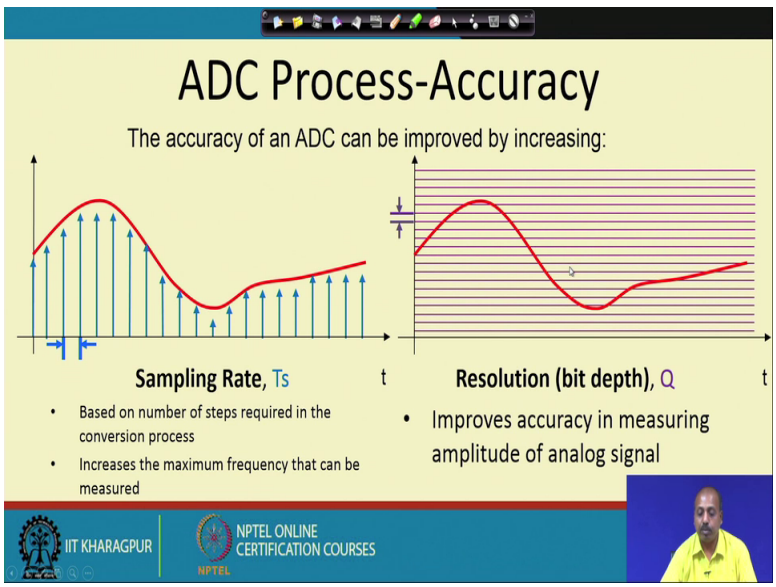

So, the accuracy of the ADC can be increased by increasing first of all the sampling rate. So, sampling rate if you increase, then it will be this distance between two successive samples will less. So, as a result you will be getting better, you will be get a better input as far as the input signal is concerned. So, like in the, so if you are sampling at this point and this point then in between whatever values are coming, so they are getting ignored. So, they are not faithfully, they are not faithfully produced that the output.

So, if you can reduce this sampling rate then we can make it better. So, that is by increasing the sampling rate. So, based on number of steps required in the conversion process, so that can be increased and increases the maximum frequency that can be measured. So, if you are doing it closer means you are, you are sampling at a higher rate. So, by Nyquist criteria, so, this is this is also going to improve the signal frequency that you can sample. Second possibility is by accuracy improvement is by improving the resolution. So, improving the resolution means you reduce the distance between two point to successive voltage levels that this quantizer can output.

So, so naturally, so, it as we have seen that giving a 8 level quantizer or 16 level qunatizer is doing much better than 4 level qunatizer. So, but the point is that as you are going for more and more levels of quantization the accuracy will improve, but this digital number of digital outputs will also increase. So, that is a that is another problem.

Anyway, so we can go for this resolution high resolution, so which is non as the bit depth that improves accuracy in measuring the amplitude of analog signals. So, if you are trying to go for a better ADC, so it may be better in terms of sampling rate, it may be better in terms of the resolution.

So, we will see this ADC designs as we proceed further and we will see that there are different types of ADCs giving raise to different sampling rates and resolution. As a result, cost of those ADCs will also vary and a high resolution high the sampling rate ADC will be very costly. So, that will also determine depending upon the applications. So, we can choose between the types of ADCs and accordingly you can come to some proper ADC that can be used for your purpose.