Digital Circuits
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Lecture - 28
Sequential Circuits

So, far we have seen combinational circuits in the in this course on Digital Circuits. Next we will be looking into sequential circuits. So, in sequential circuits what happens is that there is a sequence of events that can take place. Maybe you do not change the primary input, but still with the passage of time the situation in the circuit changes. So, typically if there is a moving display, then we get some characters on the display for some time, then after sometime some other character gets displayed.

So, that type of systems there is a sequence of events that are taking place. So, this type of devices or this type of systems they are known as sequential digital systems. So, for a circuit design behind that so, they will be coming under this broadening of sequential circuits.

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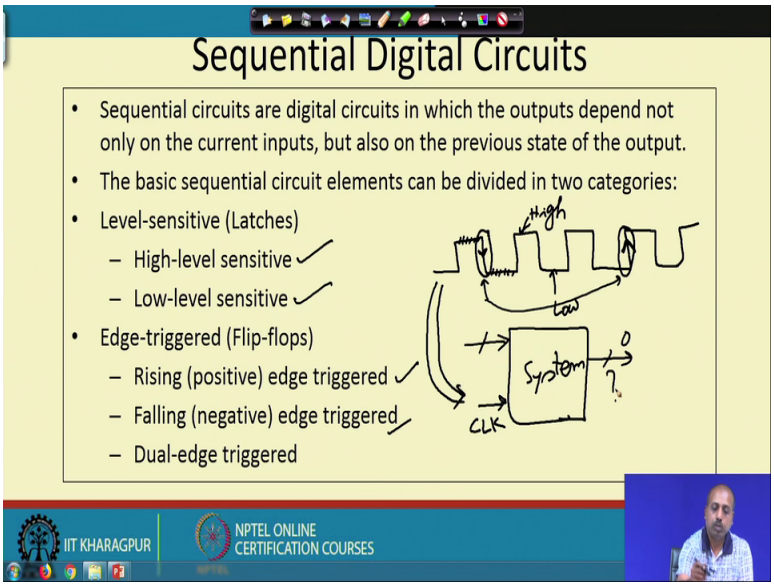

So, sequential circuits are digital circuits in which the output outputs will depend not only on the current input, but also on the previous state of the output. So, it is not only in case of combinational circuit like if we take one AND gate. So, the AND gate output is

determined by the in to the input combination that you feed at this point of time. So, it is not dependent on whether the AND gate was previously 0 or 1.

But if you gives a 0 0 then the AND gate will always produce a 0. Or if you give 1 1 irrespective of the previous output of the AND gate so, it will produce a one value; however, in case of sequential circuits. So, that may not happen because the output will also depend on the previous state of the output. So, this basic sequential circuits can be divided into 2 categories, one category is known as level sensitive, another category is known as edge triggered. So, level sensitive means like when we are looking at the operation of the circuit so, when are we expecting the circuit to change it is state.

So, it may be that we want during some interval of time, or you may want it at some precise instant of time. So, if I a for example, so, if I draw a signal so, which is in sequential circuits so, that is commonly known as clock signals. So, if I if I have got a signal like this ok, so, it has got a high period and a low period. So, you see this signal it has got some portion of the signal where the value is high.

And there are some portion where the value is low, and there are some other portions other points of interest may be, this is a point of interest when the signal is going from high to low. Similarly, say this is another point of interest, so, where the signal is going from low to high. Now if we say that we are interested about the system behavior when thus when this particular if this is the system if this is the system that we have designed.

So, this is the and it has got a number of inputs and number of outputs, and there is a special signal which is commonly known as the clock signal; where we feed an input pattern like this,. Now we may be interested in the behavior of the system when this clock signal value is high, or when the clock signal value is low.

So, when this thing happens so, when we have interested about the behavior of the system when the clock signal is high, we say the circuit is high level sensitive. Similarly, if we say that we are interested about the system behavior when the clock signal value is low so, we say it is a low level sensitive. And as I have said the other type of option is when this edges occurs. So, it maybe that we are bothered we are interested about the system behavior when the clock signal makes a low to high transition.

So, this is called a rising or positive edge triggering, and in case of this signal if you are interested about when the signal is falling down, see if you are interested in that type of situation, then will say that the system is a system is considering falling edge triggered. So, call the system is a falling on negative edge triggered system. Now depending upon our requirement so, we can we can design a system to be a level sensitive one or an edge triggered one. And between them also we can think about a high level sensitive low level sensitive or rising edge triggered falling edge triggered.

So, depending upon the requirement so, we can design the circuit. Now another possibility is that we are interested in both of these events; that is, this following edge as well as this rising edge. So, we are we are interested about the system behavior when the clock signal is rising or the clock signal is falling. So, this type of systems so, they will be known as dual edge triggered system. So, in a in this part of lecture so, will slowly look into all this different categories of a sequential circuits, and how to design those circuits.

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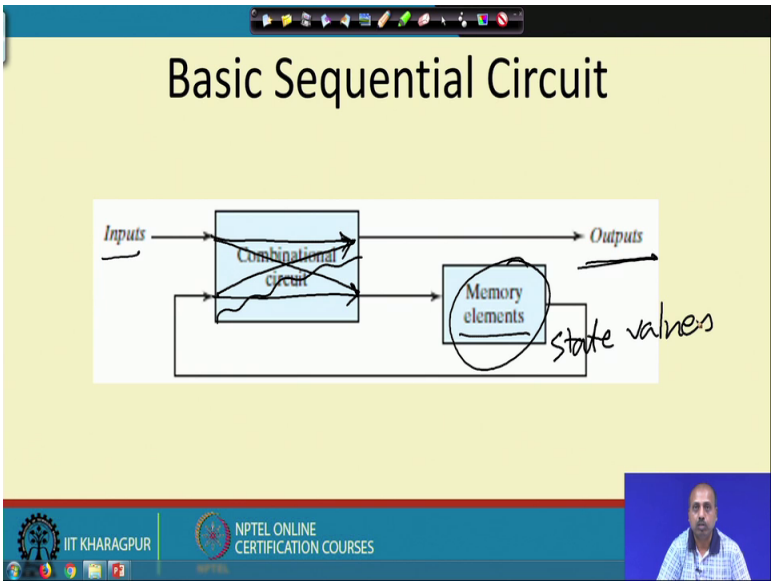

Now, coming to the basic sequential circuit so, this is a sequential circuits. So, it since it remembers the previous state of the signal of the system. So, there must be some memory element in it. So, you see that there are some memory elements in the system. So, if you forget about this part is memory element, then it has got some input and it has got some output so, that that part is a pure combinational circuit.

But as if this combinational circuit it has got some further input coming from the memory element. And this combinational circuit it can also be divided into for a into 2 parts for example. One part is determining this thing from input and this previous state from memory to memory element values. So, it determines the output, another part is from the input and this memory element value it determines the next value of the memory elements.

So, as a user of the system so, we are this memory elements are not of interest for us. So, we are bothered about this outputs only but since this memory element inputs are also coming to this combinational circuits. So, what will happen is that, this combinational circuit output will depend not only on this present input, but previously what was the content of the memory elements so, that will determine the output. So, that is the sequential behavior so, it remembers what was the previous state of the system.

So, this memory elements so, they are also known as the state values. They also known as the state values so, this state values of the signal of the system is remembered, and then when this next input comes this state values are also taken into account to determine the output. So, will so, that way we can think about this sequential circuits to be consisting of the basic combinational part, and a set of memory elements.

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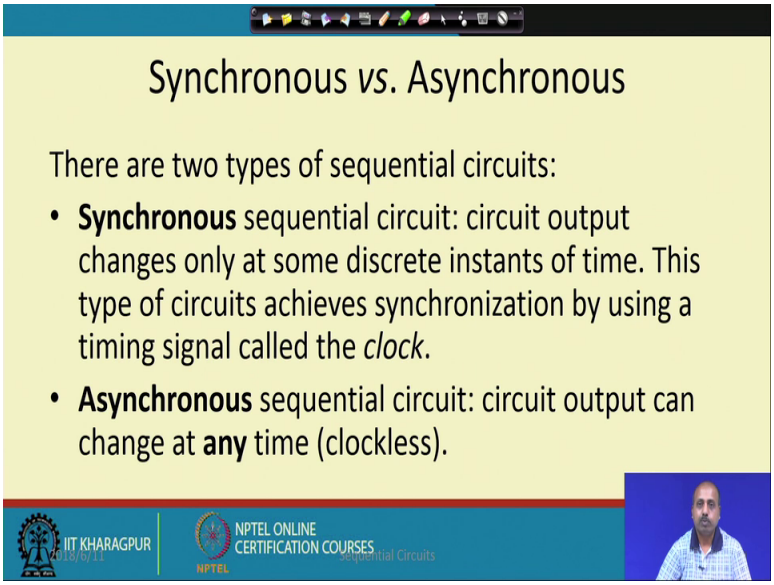

Another type of categorization that we can have in case of sequential circuit is synchronous sequential circuit versus asynchronous sequential circuit. So, in case of

synchronous sequential circuit, circuit output changes only at some discrete instance of time, and this type of circuit they achieve synchronization by using a timing signal called the clock. So, just sometime back I have already introduced the signal clock.

So, naturally the question comes can we have a sequential circuit that does not have any such timing signal like clock, ok, the answer is yes there can be. So, for the type of sequential circuits where we have such a distinct clock signal, so, they that is known they are known as synchronous sequential circuits. On the other hand, there is synchronous sequential circuit where there is no concept of a clock. So, it there is no clock and the output can change at any point of time.

In case of synchronous sequential circuits so, we have the output can change only at the clock boundaries, maybe for level triggering it may be at over all clock is high or clock is low, depending upon whether it is high level to high level triggered or low level high level sensitive or low level sensitive. On the other hand, if it is edge triggered so, if it is whether it is rising edge triggered or falling edge triggered.

So, based on that only at those points the circuit output can change. Whereas, for asynchronous circuit the output can change at any point of time. So, we will see some example.

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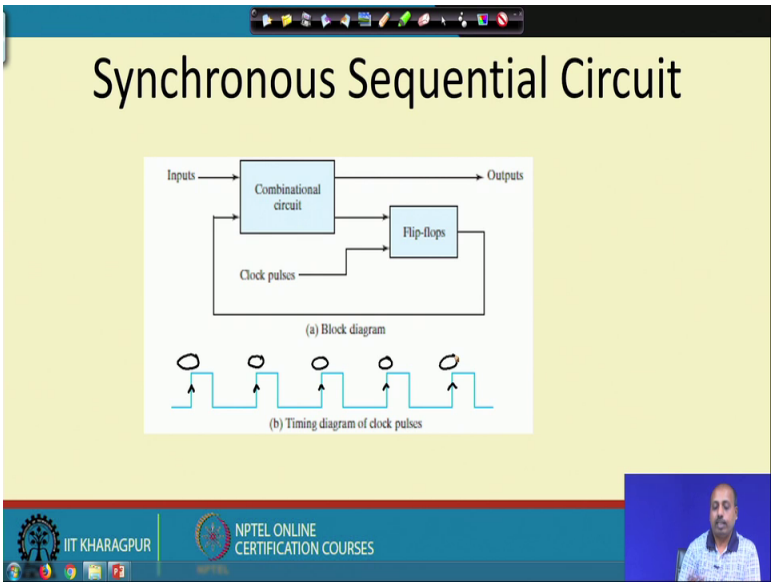

So, this is a typical structure of a synchronous sequential circuit. So, we have got this combinational input, the combination circuit that gets the input plus there are some memory elements, so, which are commonly known as flip flops.

So, will see this flip flops after sometime. So, this flip flops are there so, this clock pulses are actually feeding this flip flops. So, this flip flops are activated when the clock signal is activate. So, if we say it is the high level sensitive then when the clock signal is high that is at this point, then only the values that are coming from the combinational circuit to the flip flops will be stored in the flip flop.

Otherwise when the clock signal is low for example, during this period, whatever happens to this combinational circuit so, these lines, these lines will be changing, but that will not affect the flip flops. So, as a result the state of the state of the circuit will not change, state of the circuit will remain unaltered. Only if, when the clock signal is active then the input changes, then only this flip flops will change.

Similarly, if you are thinking about say edge triggering, then if we say that it is rising edge triggered so, the circuit which state will change only if the input changes around this. So, the input changes around this time, then only the circuit the state out whether the this flip flop contents will change, otherwise it will not. So, this gives us advantage because others are design becomes simpler as will see.

However, in some system so, we may not have this type of clock signal, and they are known as asynchronous circuits.

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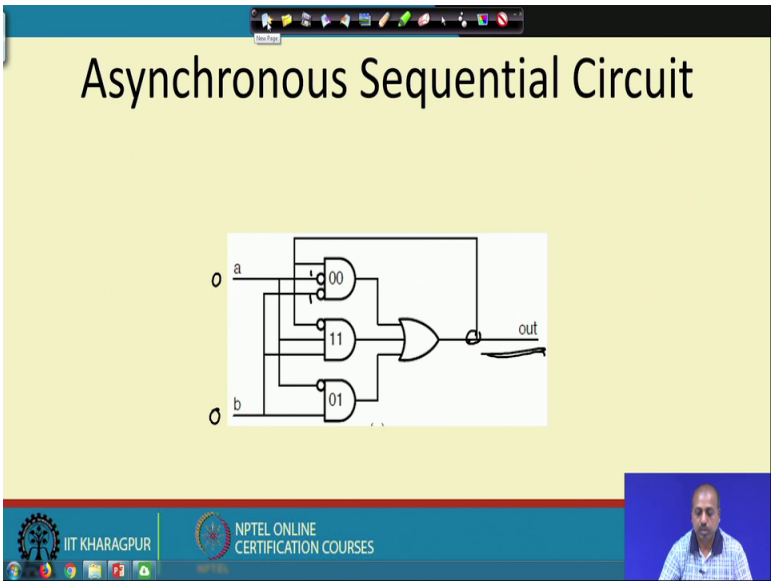

So, this asynchronous sequential circuits so, this is an example so, here you do not have any clock signal in the system; however, if you are if I ask you suppose I give a equal to say 0, and sorry if I give a equal to 0, and say b equal to 0, a equal to 0 and b equal to 0.

So, can you tell me, what is the value what is the output? So, it is difficult because a equal to 0, b equal to 0, means these 2 bits are getting 1 1. So it is dependent what was the previous value of this out, so, it is dependent on that. So, until and unless I tell you what is the previous vale of this out you cannot determine the next value of out. So naturally so, this type of circuits so, this is also a sequential circuit, because it depends on the previous value or previous output of the circuit.

However, it is there is no explicit clock signal in this system. So, it is not asynchronous circuits so, this is an asynchronous circuit. So, this asynchronous circuits are also used sometimes. So, we will see the relative advantages and disadvantages of these 2 types of systems.

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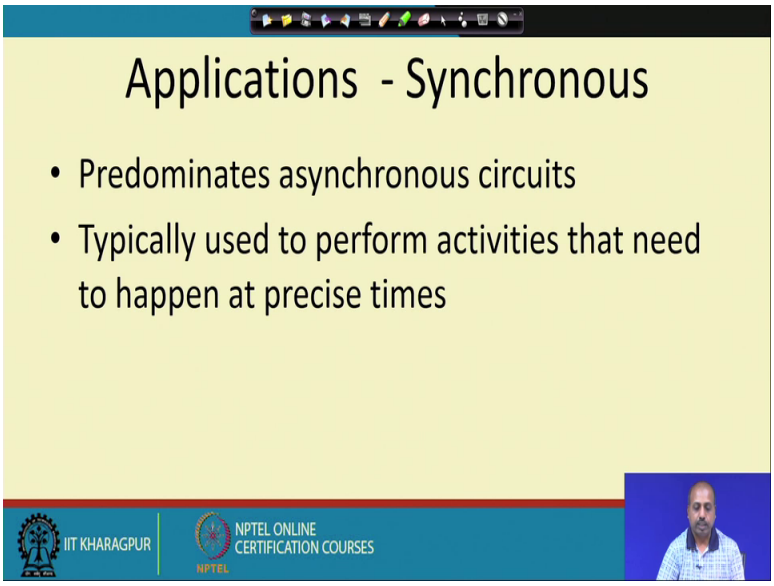

So, applications of synchronous so, this synchronous sequential circuit they predominate asynchronous sequential circuits. So, normally whatever sequential circuits we design so, they have a clock signal in them and then the so, most of the circuits are synchronous in nature. So, you will not find much asynchronous sequential circuit, because of several reasons that will see.

And this typically used to perform activities that need to happen at precise times. So, at some regular time interval something has to happen, that example that I to get the beginning like if there is a display then some character is displayed so, there is a fixed amount of time for which one character will be displayed after that the next character will be displayed.

So, this passage of timing so, when the character will change so, that is the space that is fixed. So, you can say that at fixed intervals of time, we are expecting something to happen I will something to happen in the system so, they are synchronous systems. So, they are typically used to perform activities that need to happen at some precise times, or if there is a conveyor built on which items are moving and at regular intervals of time, so, we can we there may be a robotic hand which is picking up the items from the from the belt.

So, that also happens at some regular intervals of time. So, all this examples so, they will be leading to synchronous sequential circuits.

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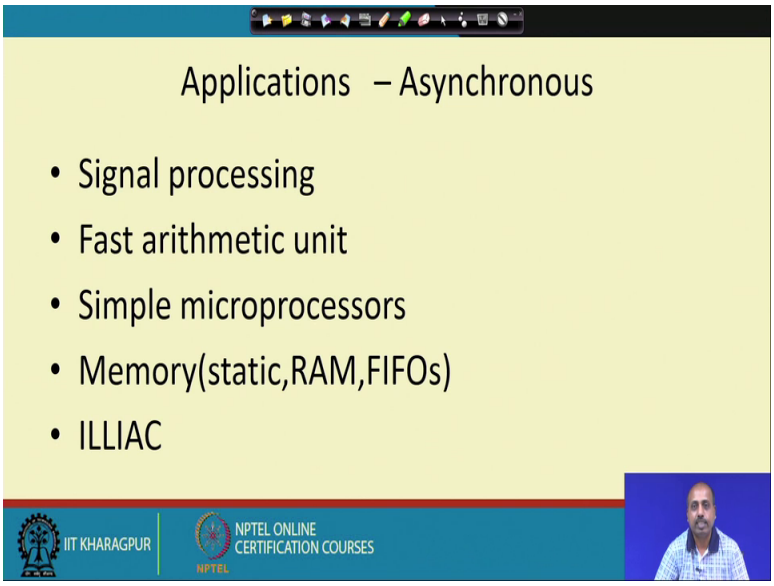

On the other hand, asynchronous sequential circuits so, they have got applications in signal processing because you do not know, when the exact signal will what is the clock of the clock period of the arrival of this signal so, that is not known.

So, we have to we have to do it in an asynchronous fashion, then one typical problem with the synchronous circuits is that so, you are your the speed of the circuit is bounded by the clock signal that you are feeding. So, this clock is a clock signal is not very high so, you cannot do you cannot do operations fast.

So, I may have different components in my in my system, so, they are operating at they are all of them are synchronous sequential circuit, then the delay of the slowest modules so, that will determine the maximum clock frequency that I can have for the system. Where as if this all the systems are asynchronous in nature, then what can happen is that all of all the systems they can operate at their own speed, and we may get a faster system.

So, maybe you can design an arithmetic unit which is much faster than this register and all in the system. So, that way we get a fast arithmetic unit, then simple microprocessors. So, they are made the asynchronous because of this speed achievement. So, we can do it like memory, the static memory then this ram FIFO first in first out buffer so, they are all made this they are made of asynchronous system.

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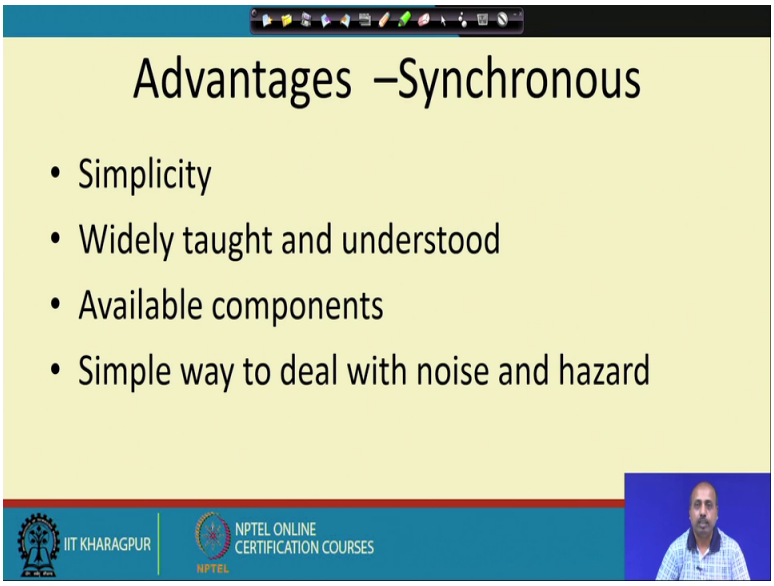

ILIAC 4 machines so, this is one of the computer LADLI computers so, they are made in asynchronous mode. The why do we go for synchronous? Asynchronous has got so many advantages; the major advantage is the simplicity. So, asynchronous system so, since we have to consider what is the previous value of the output at, whenever we are trying to determine like, what is the current value of the output, we are we are faced with the question the what is the previous value of the output.

Now, this previous value means before how many how much time? So, that question has to be answered. And in case of synchronous sequential circuits so, you can just say it is at the previous clock period what was the situation, or previous to previous clock period, what was the situation. So, we have got a fixed interval or fixed instant of time at which of which we are talking about.

But in case of asynchronous circuits we do not have this instants of time. So, that they are the time becomes a continuous value there. And then this previous time definition of this previous time becomes difficult. So, synchronous circuits are generally much simpler to design, and they are widely taught and understood ok, for digital circuits classes so, we normally do you normally go to the synchronous design only because that is that is much easily understood and can be easily thought.

And in our course also for most of the designs so, will be going to synchronous designs also available components. So, there are many chips which are synchronous in nature.

So, they are realizing some sequential circuits which are asynchronous in nature. So, that is why we go for that, then simple way to deal with noise and hazard.

So, if some noise signal comes so, that can change the state of the system. Now you see for synchronous sequential circuit we have the advantage that if the noise does not come when the clock is active, then that noise is will not be able to affect the system. So, we can be we can concentrate only for noise protection during the clock active time. Similarly, hazard that we discussed in our previous classes. So, that also is that affect will come only when we have got this clock signal active.

So, otherwise particularly for edge triggered system, so for very small amount of time we have to have the system noise and hazard free. Otherwise this noise and hazard so, they are unable to affect the system state. What is the disadvantage?

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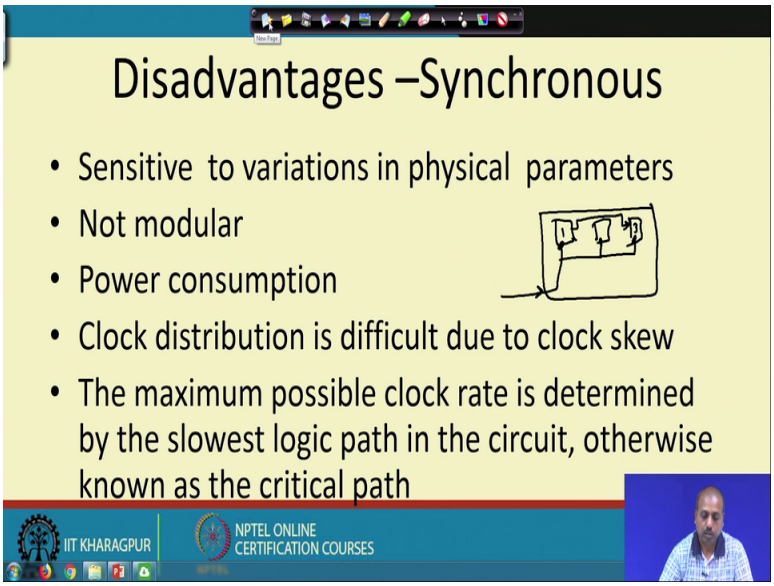

So, disadvantages of synchronous circuits are like this. Is sensitive to variations in physical parameters? Because physical parameters like say if I have got a big circuit, then this the various parts of if they are operating at a different speeds.

And then with the change of this temperature and particularly in this power consumption and temperature those values are also changing, the delay values are also changing. So, that makes it difficult. So, that becomes sensitive to variation in physical parameter. It is

not modular so, you cannot just add another module to this because that will determine the clock speed also.

Power consumption so, whenever the circuit is actives so, it will consume power. Now in case of sequential synchronous sequential circuit what is happening is at is that the at least the clock signal is changing at regular intervals of time. And we have seen that for CMOS type of technology, the power consumption occurs only when the input signals change is output to the input signals are changing the values.

As a result, the output is also changing, but in case of sequential circuit you know that even if you have got the inputs unchanged, input remain same. So, that output is also same, but the clock signal will always struggle. So, as a result the power consumption due to this clock signal will come into picture. So, the synchronous sequential circuit power consumption will be high.

Clock distribution is difficult due to clock skews. So, clock skew means so, if I have got a if I have got a board, on which I have got some systems smith, now the clock signal is entering here. So, I have got a chip here, I have got a chip here, I have got a chip here, and all of them are operating in a synchronous mode.

Now, this clock signal is a distributed like this, ok. If it is distributed like this, then you see that this delay of this paths so, they are proportional to the length. In fact, it is squarely proportional to the length. So, as the length increases the delay increases severely. So, this it is it is intended that when the when the clock signal reaches this module. At the same point of time the clock signal reaches here and also reaches there.

But the way I have laid out this clock line so, it will not be it is not possible to ensure that. So, there will be a skew, the time at which the clock reaches here. This third module will get the clock after sometime delay so, this is known as clock skew. And it is. So, this clock skew if it is there, when naturally my when this circuit is producing some outputs. So, it is to be used by this module, say functional output produced by the module one is to be used by module 3.

And if it is so then this module one it has produced the output when the clock signal was active, but at that time this module 3 was not getting the clocks it could not use the value.

By that time maybe some other thing has changed. So, that way there that is why this clock skew is a severe problem.

And for synchronous sequential design so, it is a challenge like how to distribute the clock signal through the, IC through the integrated circuit chip, ok. So, that is the VLSI layout problem. So, will not go further into that so, this clock distribution becomes difficult due to this clock skew, the maximum possible clock rate is determined by the slowest logic path in the circuit.

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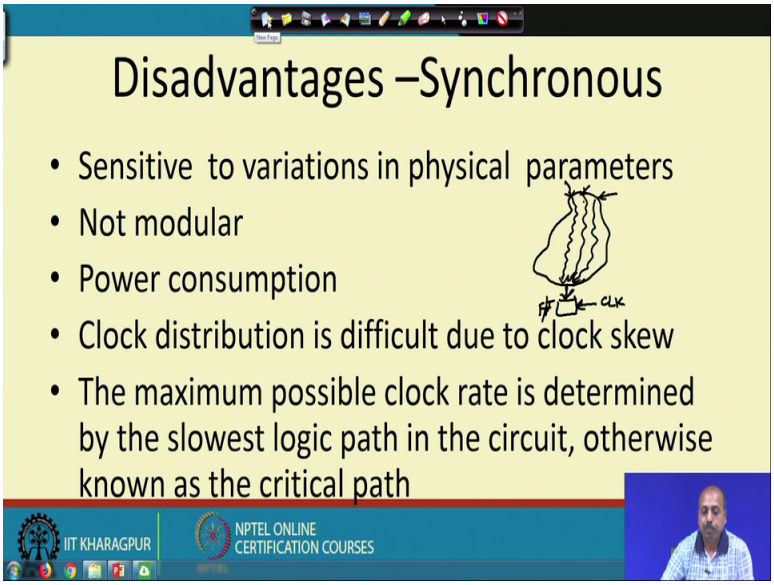

So, if I have got some if I have got some combinational circuits, suppose this is a combinational circuit, and this is feeding some flip flop, ok. So, this is feeding some flip flop, this output is stored like the way we have seen in the sequential circuit. Now what is the; what type of plot I can apply to this to this to this flip flop, ok. So, if this flip flop operates at a clock so, this combinational circuit it get some input from outside it does some computation, and accordingly it produces the value here.

So, the if this for clock is faster, then the delay of this combinational block then what will happen? This flip flop will get some wrong values. So, the values when I change this input values, the before the proper output has been computed the flip flop will get a to get the values.

So, as a result the value will be incorrect so, what is required is that this clock should be slower than the delay of this particular block. And there are several paths through this for through this network. So, one path may be like this going through several gates another path may be like this. Another path may be like this now among these 3 paths.

So, whichever path is the slowest so, that is the critical path. So, this critical path delay so, this will determine the clock frequency, the maximum clock frequency at which I can operate the system, ok. So, the slowest logic part in the circuit so, that will determine that is the critical path so, it will determine the clock period. So, that is another problem with the synchronous sequential circuits.

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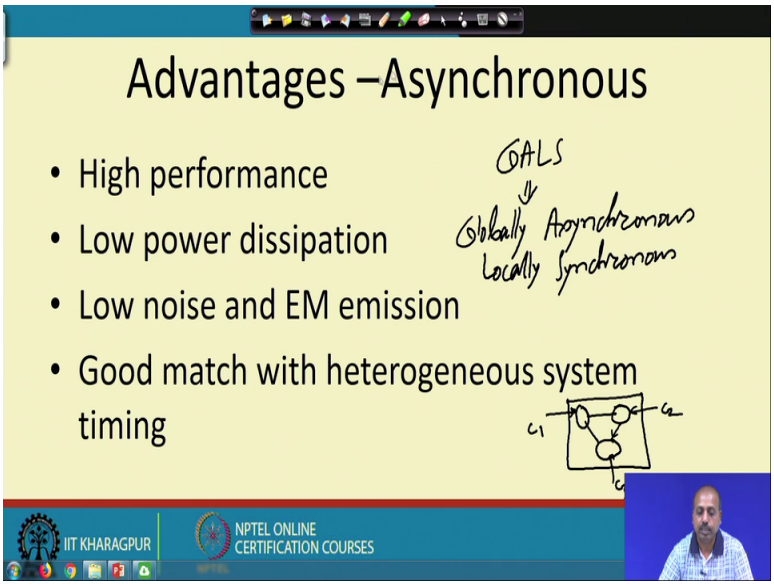

Asynchronous circuit is the major advantage that we get is the high performance because there is no clock signal. So, I am not limited by the clock. So, I can operate whichever module gets the data ready. So, it can start operating on the data and they reproduce the result fast.

Low power dissipation so, if the inputs do not change, then the output will also not change so, as a result there is nothing like at every clock interval. So, that the clock toggling will occur so, that that sort of thing is not there. So, this power dissipation is often much less compared to the synchronous sequential circuit. Low noise and a electromagnetic emission so, this is also another issue, like this generally it is seen that it

does not produce this high noise and electromagnetic radiations are also less, because there is no such toggling.

And good match with heterogeneous system timing, like even a system I have got a different types of components, and they are operating at different frequency, then also we can have this thing. So, in fact, for this a heterogeneous timing so, this leads to one particular type of structure which is known as GALS structure, which is globally asynchronous globally asynchronous locally synchronous type of structure.

So, that takes the advantage of both this synchronous and asynchronous design. What the idea is that so, suppose I have got a system like this, now in this system I have got several component so, this is one component so, this is another component, this is another component. So, they are interacting between them so, there are some signal lines running between them so, they are interacting.

Now, they have got they are running at their individual clock. So, this is running on clocks c 1. So, this is running at clock c 2, this is running at clock c 3, but the clocks are not same so, c 1, c 2, c 3 are not same. So, individually when you look at the systems so, they are synchronous in nature, but if you look into the overall system. So, that is asynchronous system, because there is no common clock synchronizing all the 3 subsystems.

So, this type of designs have become very popular, because it combines the advantages of synchronous design, that is the ease of design and all, and the advantages of this asynchronous design where you do not have to have this global clock signal, then this power consumption high power consumption like that so, they are not there, so that way this GALS style o r design have become quite common.

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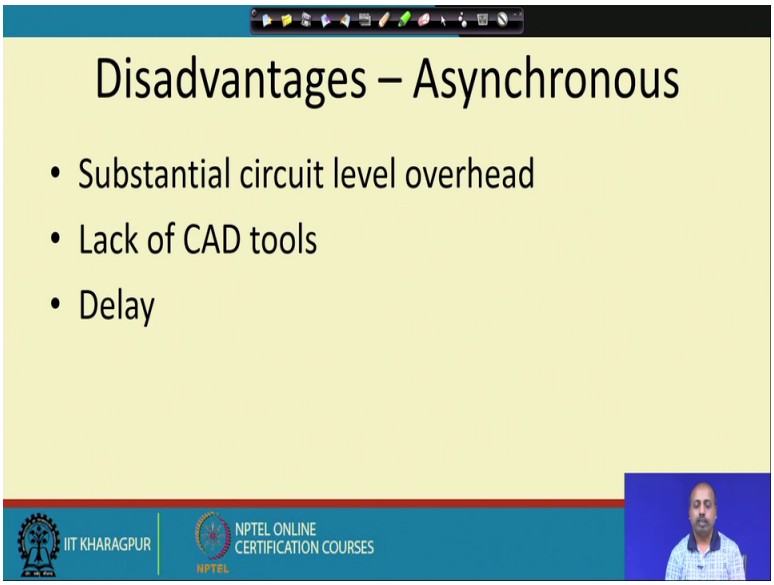

So, next at disadvantage of asynchronous system is the substantial circuit level overhead because of this lot of feedback lines will be running since the clock signal is not there, and this sequential elements are often realized by with other combinational elements.

So, as a result there will be a large number of lines running backwards so, that is the circuit level over it is high. And the set of cad tools so, that you for asynchronous design so, you do not have this very good cad tools available so far so, that is the other problem. And delay so, delay in the sense that you have to you have to match the delays between 2 stages, if both the stages that are asynchronous in nature so, you need to match the delay between the 2 stages.

And that also become a concern, so, delay becomes a concern.

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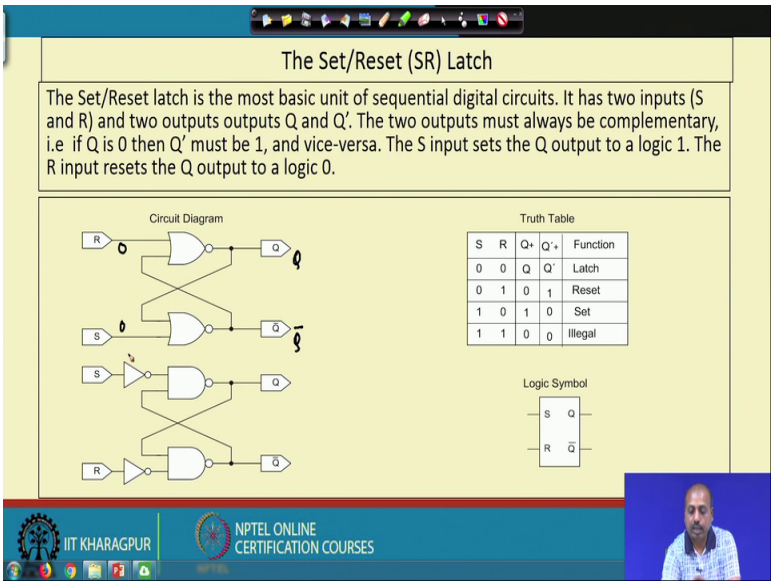

So, will start with some latch circuits, the first latch that will look into is known as the SR latch, the first sequential circuit that will look into is known as SR latch or set reset latch. So, this is the most basic unit of sequential circuit. It has got 2 inputs S and R, and 2 outputs Q and Q bar or Q dash, the 2 output must always be complemented; that is if Q is 0, Q bar is must be one and vice versa.

So, this is by the specification of the S R latch. So, it says that it is it has to be a sequential circuit, that will have 2 input set and reset. And there will be 2 outputs Q and Q bar, and by specification, Q bar should be complement of Q. It is further stated that the S input will set the Q output to logic one, and the R input resets the Q output to logic 0, that is why S is called the set input R is called the reset input.

So, the set input will set Q to 1, and reset input will set Q to 0. So, a basic circuit diagram for this can be like this. So, it can we can take 2 cross coupled nor gates, ok, now you can understand that if I set this, in this nor gates. So, if I set this S to be equal to 1, if this S is equal to 1, then this Q bar will be getting 0. And this so, so, it if it is 0 here then what ever be the Q bar so, it will be coming here so, this Q will be coming back to this.

So, this set and reset inputs so, let us look into this truth table and try to understand. Suppose S and R both are 0, 0, so, if both are 0, if say if both of them are 0, then what happens is, so this is 0, and this is 0 so, this is this Q is coming and this is a nor gate. So, what will happen is that this Q whatever be the Q value so, it will be coming at say Q

bar. So, this Q value will be coming and this is just a nor gate. So, it will be Q bar, and this is Q bar so, when it is when it is getting this so, this is equal to; this is the main equal to Q.

So, if you look into this truth table when this S and R so, Q plus and Q plus dash. So, Q plus means what I mean is that, at the next time you need what will be the value of Q. So, that is Q plus and whatever and Q, Q dash plus means what is the value of Q dash at the next time unit. Now you see that what happens is that if you give S and R as 0 0 then this Q remains at Q plus remains at Q and Q Q dash plus remains at Q dash.

That is whatever the value it was having previously so, that value remains there. Now let us take the other combination, let us take say this R S equal to 0 and R equal to 1.

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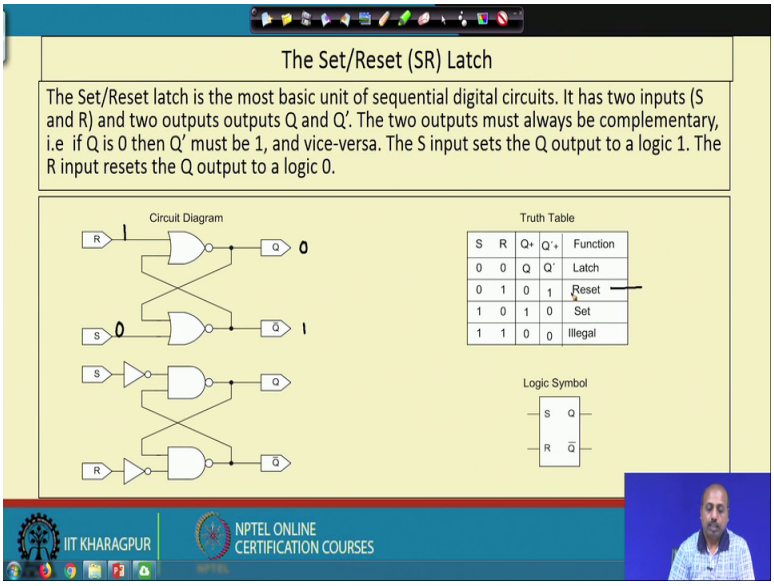

Then since this is a NOR gate irrespective of the value of Q bar, this Q will become equal to 0, and once this Q and this and this Q was coming here. So, this will be this 0 comes here so, this 0 will be making it 1. So, you see that when this S is equal to 0 and R equal to 1, we get the value Q plus equal to 0 and Q bar plus equal to 1. So, that is the reset so, as if the flip flop has been reset or the latch has been reset.

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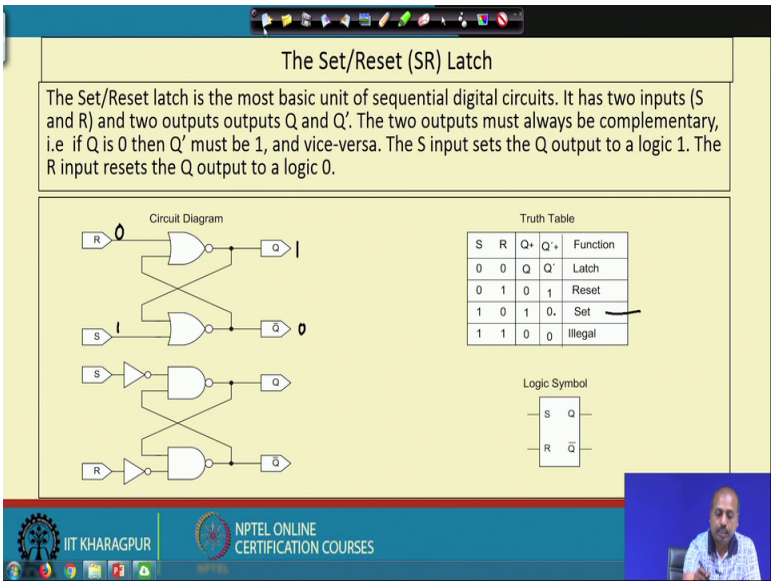

The other combination like say 1 0 so, if I give S equal to 1 and R equal to 0, then what will happen? This will be setting this by the similar logic. So, this Q bar output will be equal to 0, because this S input in 1, this NOR gate and this 0 0 going there so, this will make this thing to be equal to 1. So, what is happening is that Q plus is becoming one and Q bar Q dash plus is becoming 0 so, that is the value is set.

And if it is 1 1, then it is we say that if I give it 1 1, then both the outputs will become 0 0.

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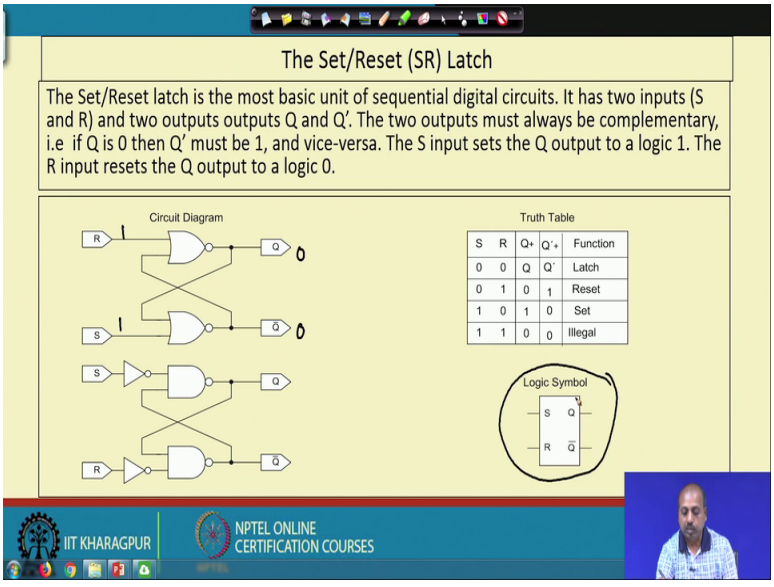

And by the specification so, this is called illegal so, this is illegal so, we should not apply this 1 1. Similarly, if we take the NAND gate based realization also. So, you will get you will see that if we do it take 2 cross coupled NAND gates and take 2 inverters before after S and R you get the similar type of truth table. So, this is the logical symbol for this S R latch, ok. So, we just we give it this is a shown like S and R being different values, if we put then Q and Q bar will be following this truth table value.