Digital Circuits
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Lecture - 23
Decoders, Multiplexers, PLA

So, we next look into a topic that includes of some more combinationals logic elements, Decoders Multiplexers and PLA's. So, these are slightly higher level than the gates logic gates that we have considers so for, they are essentially consist made up of logic gates only; but for so, they will have a good number of logic gates in them.

So, for our understanding. So for many a time we will find that the function that we want to realize is similar to one of these component decoder multiplexer and PLA. So, as a result so, there are many integrated circuit chips that have been developed for you that realizes this functions in them.

So, we can use those chips directly ok. So, we do not have to do in terms of basic logic gates. So, that way the design process become simpler ok. So, we will be looking into this one by one by one so, first we look into decoders.

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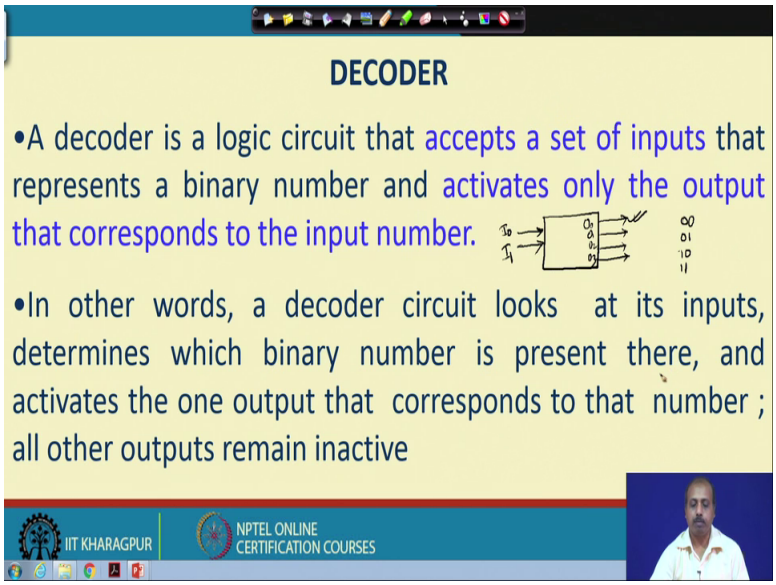

So, a decoder it is a logic circuits that accepts a set of inputs that represents a binary number and, activates only one of the output that corresponds to the input number. So,

what we mean is that it has got so, if this is the box corresponding to decoder, this is the logical block that realizes the decoder, then it has it accepts some input ok. So, suppose it accepts to input and so, this 2 bit 2 input that I have say I have say I input 0 and input 1.

Now, they correspond to some binary number binary number like say, if these two bits are 0 0; that means, it is in the it is represent in the number 0, if this is 0 1 it is representing the number 1, 1 0 is 2 and 1 1 is 3.

Accordingly this in the output side I will have four lines ok, I will have four lines and out of this four lines. So, if I give say pattern 0 0, then this line will be this line output will be high or and others will be 0 ok. So, if I write in terms of so, O 0 O 1 O 2 and O 3 so, depending upon the binary pattern that I am feeding. So, one of the four outputs will be active and others will be inactive. So, it active means it may be high were others are low, or it may be the reverse way that active means the output is low and while rest of the outputs are high. So, either way it can be done.

So, a decoder circuitry looks at it is inputs determines which binary number it repre is present, there and activates the one output that corresponds to the number, all other outputs they remain in active.

Now, you can very easily design some circuit using some basic logic gates and in fact, it is done that way only, but if your circuit is very function that you want to realizes quite complex, then it may be that a good number of gates. So, we are putting, we are replacing by a decoder to make the design simple to understand ok.

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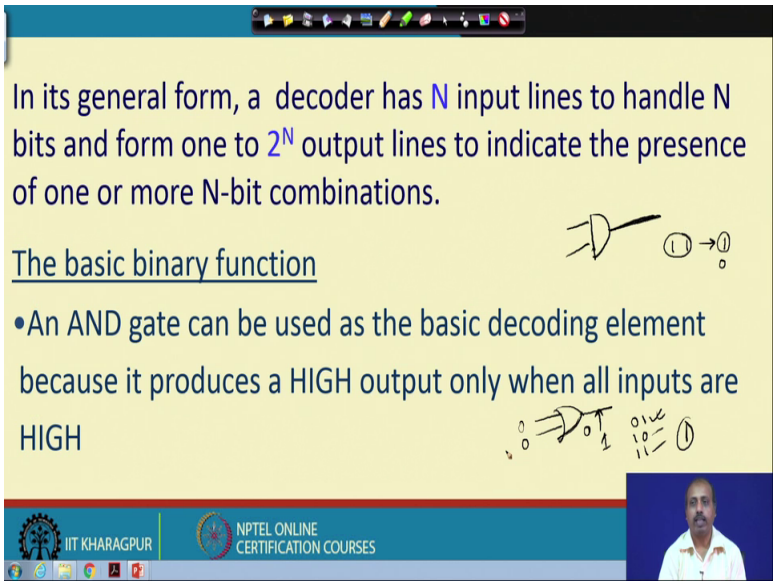

So, so, in a general form a decoder has got N input lines to handle N bits and form 1 to 2 power N output lines, to indicate the presence of one or more N bit combinations. So, this has this is the basic decoder. So, we will say it is 1 to 2 to the power N to 2 to the power N decoder. So, that way it is it is taking N input lines and depending upon the value of N one of the 2 power N outputs will be made active.

So, you can see that this basic AND gate. So, that acts as a decoding element because it produces high when all it is inputs are high. So, if I take one AND gate you see the if you the AND gate. So, this output it has got 1 output and 2 inputs. So, this is also in some sense decoder, because for when the input pattern is 1 1, then only it is giving 1 all the other cases it is giving 0 output is deactive. So, since it has got only 1 output and that 1 output is high, when 1 1 is high.

On the other hand if you say OR gate so, OR gate in that sense it is not a decoder because, it is it produces one at for 3 different combinations so, 0 1 1 0 and 1 1, for all the 3 combinations so, it is producing 1. So, by if I just look at this output and see that this is 1, I do not know I do not I can I cannot tell what was the corresponding input pattern, but for AND gate it is true that as soon as you look into the output and it is find a 1 there, you will know the input pattern is 1 1. So, AND gate in some sense can be said to be a decoder.

Of course you can tell that for OR gate also, if I get a 0 at the output, if I get a 0 at the output I definitely know that the input patterns are 0 0. So, if I am looking for AND active low decoder circuit ok that is it lowers the output when the corresponding input pattern is applied, in that situation OR gate will act as a decoder whereas, AND gate will not act as a decoder. So, that is very rudimentary type of decoder that we are talking about.

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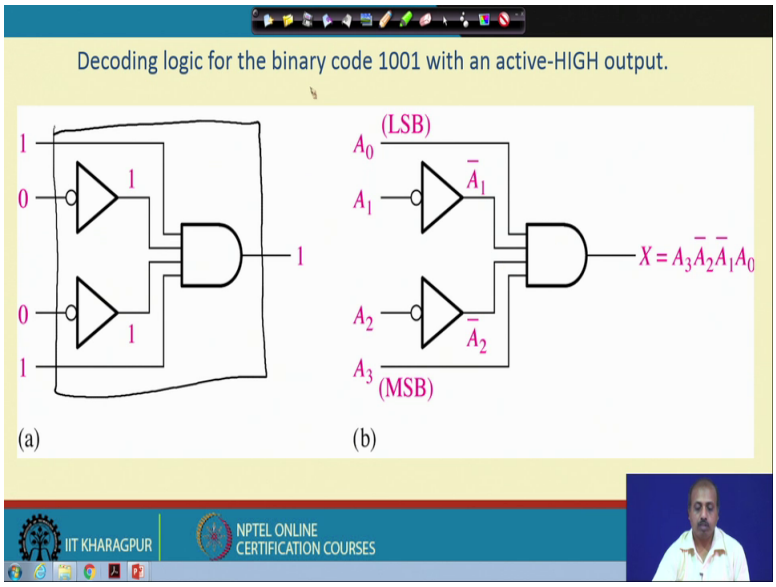

Now, so, this is the decoding logic for the binary code 1 0 0 1, with an active high input. So, this so, if you get if I have to design a black box, or some logic circuit such that for 1 0 0 1 it will give the high output. So, I can do it like this so, the I can put I can design a circuit, where all this things is put inside the box and, this box takes 4 bit input and so, only when this 4 bit input is 1 0 0 1 as per the design of the circuit you see that the output is 1.

Similarly, if you are if you are talking in terms of this value so, A 0 A 1 A 2 A 3. So, here I am getting A 1 bar here I am getting A 2 bar so, they are anded. So, we get A 3 A 2 bar A 1 bar A 0. So, when this particular input combination comes at the block input, then only this output will be made active.

So, this way we can realize circuits to get the decoders.

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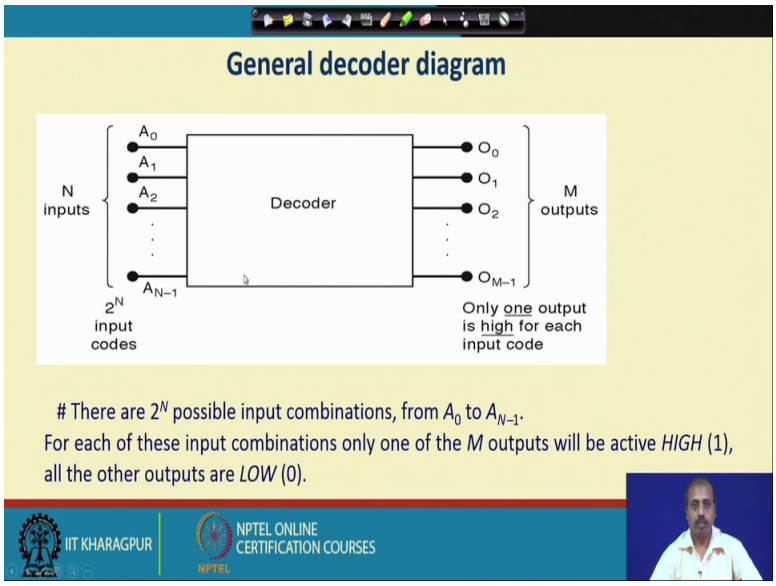

In a general form so, we have got this A 0 to A N minus 2 so, N inputs are given to a decoder and, there are M outputs O 0 to O M minus 1.

Now, this N outputs N inputs so, they can correspond they can give values, which may be any one of this 2 power N input code set ok. So, this is 2 power N input codes are coming and, then it is producing output which is one of this M outputs will be made high. So, 0 0 to O M minus 1 1 of the outputs will be made high.

So, there are 2 power N possible input combinations from A 0 to A N minus 1 and for each of this input combinations only one of the M outputs will be active high all others will be are low all others will be low. So, there will be so, if high is 1 and low is 0. So, you can say it is 1 and 0. So, this is the basic decoder definition ok. So, we represent it by square like this.

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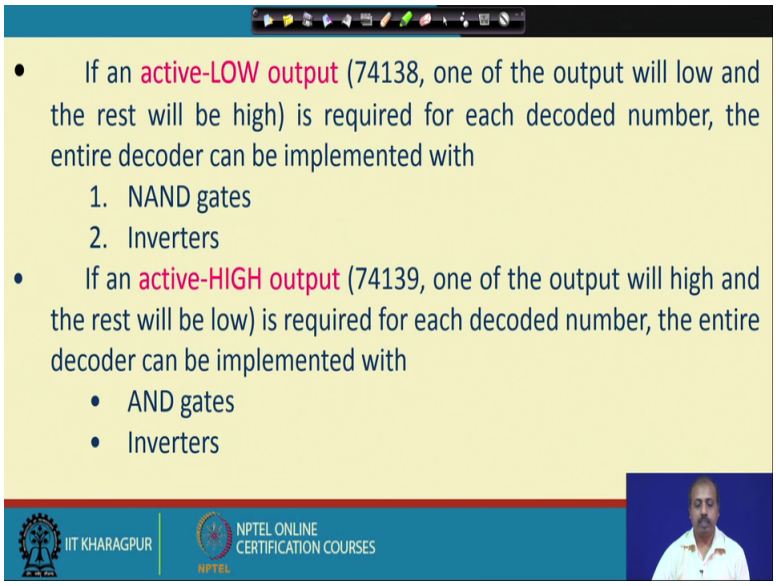

As I said that there can be two variants of the decoder one decoder is active low output, where the whichever output is active. So, that output will be 0 and the rest will be 1. And other category is active high output, where I have got this decoder who the active output will be 1 and the rest will be 0.

And there are IC chips that have been designed for both categories like 7 4 1 3 8 is an IC chip, which has got which is a decoder function with active low output and, 7 4 1 3 9 is again a decoder, but it has got active high output.

So, this in case of active low output type of decoder, the entire decoder can be implemented with NAND gates and inverters whereas, this active high output the decoder can be realized using and gates and inverter. So, as we have seen previously like in this diagram.

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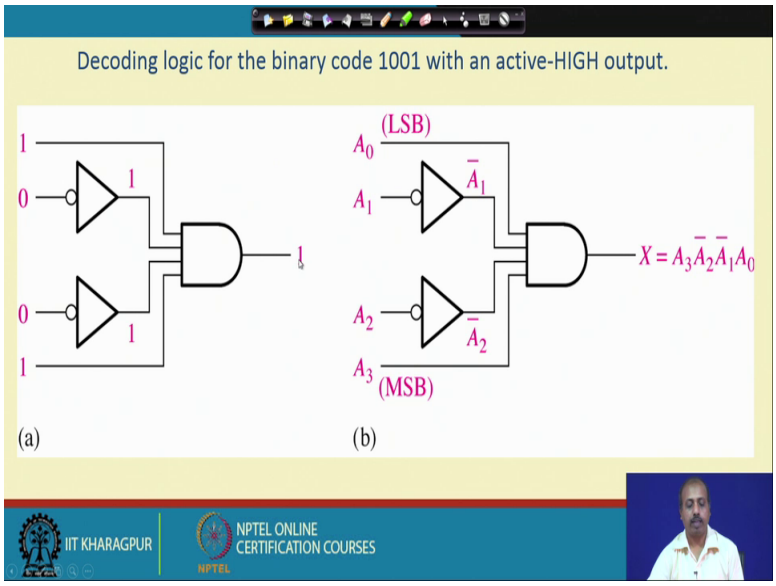

So, here I was look for active high output, so, I could do that using inverters and AND gate. So, if I was looking for active low output, then I have to use inverters and NAND gates.

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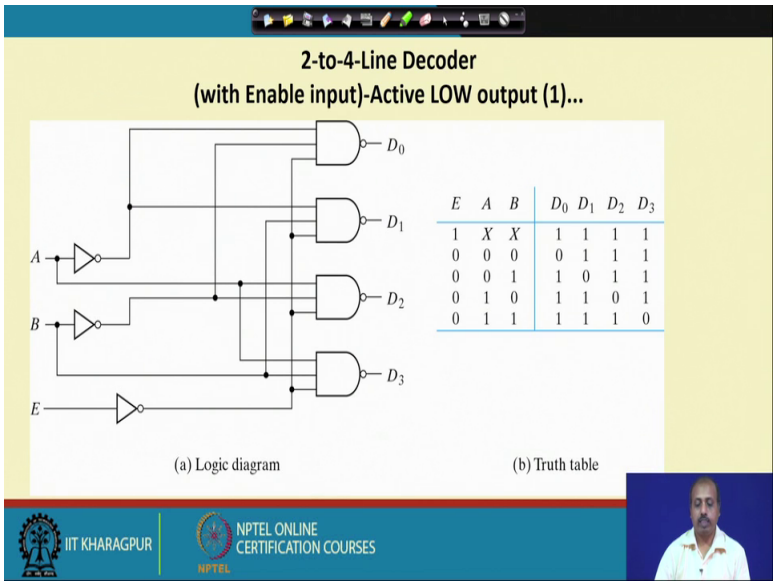

So, the first one we will be considering is a 2 to 4 line decoder with enable input. So, what is there so, so here, this is the 2 input A and B that are the, that gives us to the output number that should be made active ok.

So, this is active low. So, corresponding to A and B whichever output is getting selected that output will be low and, the rest of the outputs will be high. So, for example, when A B is 0 0, then D 0 is 0 and rest of the D 1 D 2 D 3, they are 1. Similarly for 0 1 D 1 is 0 and the rest of the outputs are one like that and, there is one additional input called enable or E and, this the outputs will be coming properly only when this E is equal to 0.

If E is equal to 1, then all this D 0 D 1 D 2 D 3 so, they will be giving with the value 1 so, none of the outputs are active because, we have taken 1 as active is 1 is the non active state and 0 is the active state. So, if this E is equal to 1, then all the outputs are 1. So, the all of them are non active node non active mode. So, this way we can augment the decoder to have an enable input as well.

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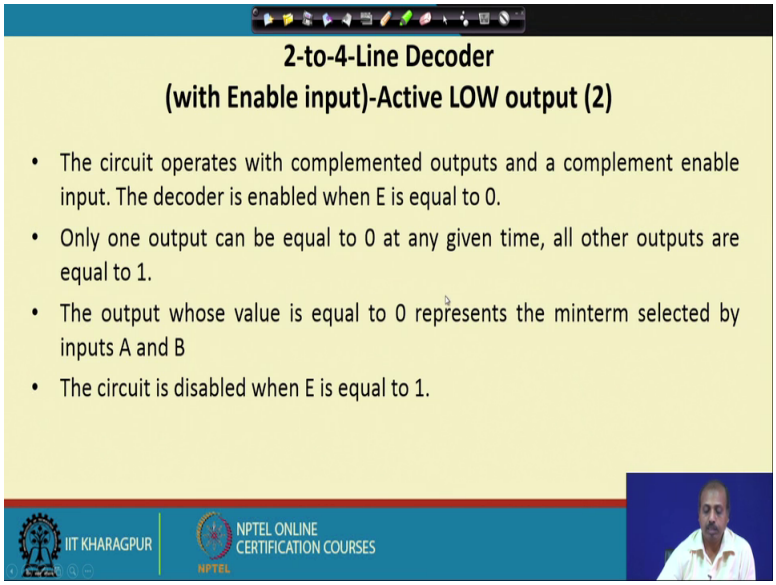

So, next we will look into so, this the circuit operates with complemented outputs and, a complement enable input as we have said. So, the output active output is 0 and, decoder gets enabled when E is equal to 0. Only one of the can be equal to 0 at any given time all other outputs are equal to 1, output whose value is equal to 0 represent some min term selected by inputs A and B.

So, A and B they will they it can select 4 min terms, 2 input functions. So, it has got 4 min terms and in this so, so this is a D 0, D 1, D 2, D 3 they are actually corresponding to min term 0 1 2 and 3. So, based on this A B value the corresponding min term is getting

selected and corresponding D bit is made equal to 0 and, circuit is disabled when E is equal to 1, for getting the proper operation of the circuit E should be set to 0.

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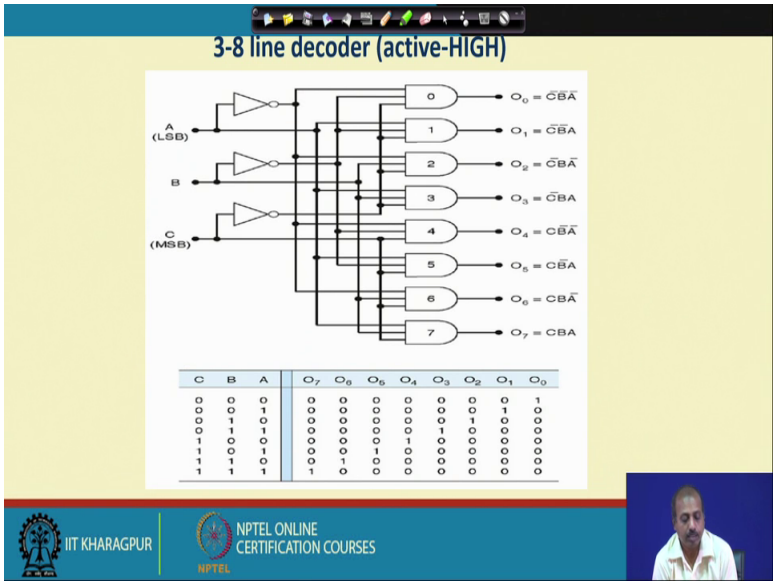

We look into another example so, it say 3 to 8 line decoder. So, 3 bit input so, if the N equal to 3. So, naturally I can have 2 power N that is 8 as the M value or the number of outputs that I can that it can have.

Now, here you see that what do you need is for O 0 O 0 output will be will be equal to 1, when all this A B C bits are 0. So, how have we represented it? So, this is an AND gate here and you see the inputs are coming from A bar, then the, this is coming from this is coming from this B bar ok. So, this is this is this is the line B bar. So, inverted B so, this is the B bar and also C bar, when A bar B bar C bar. So, these two values are equal to 1, then this output O 0 will be equal to 1 and all other outputs will be equal to 0.

So, this is the truth table that we have so, when this A B C is 0 0 0 O 0 is getting selected O 0 is make becoming equal to 1 and rest of the outputs are 0. So, for any other combination one of these outputs will be made equal to 1. So, this way we can have 3 to 8 line decoder.

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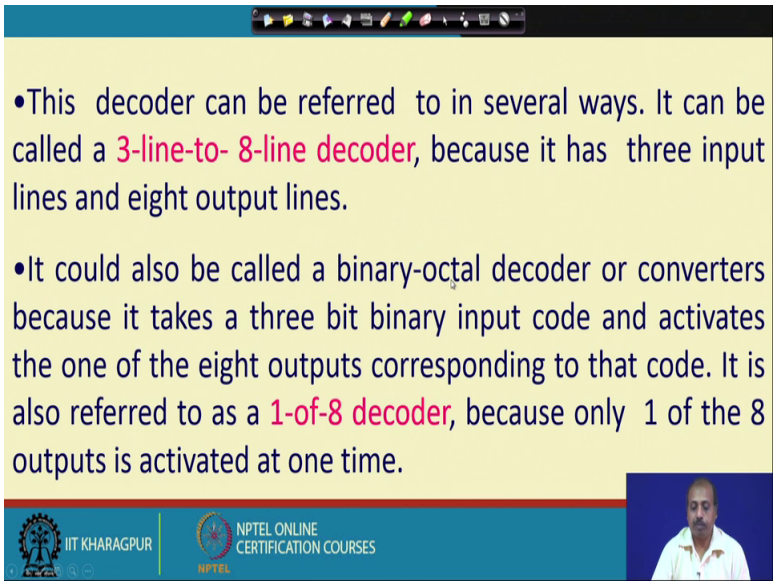

This decoder can be referred to in several ways; first of all it can be called a 3 line to 8 line decoder. As there are 3 input lines and 8 output lines. So, it has it is called 3 line to 8 line decoder. Now see this 3 and 8 so, these information they are redundant like as soon as I say the 3 are the input lines. So, 8 are the output lines.

Similarly if I say 8 as the output line, then 3 is the input line. So, it is also it can also be called a binary to octal decoder ok, or converter because it takes a 3 bit binary input code and activates the 1 of 8 outputs corresponding to that code, it is sometimes calls ones it is also sometimes called 1 of 8 decoder.

So, these are varies terminologies that we have 3 line to 8 line decoder 1 of 8 decoder. So, 1 of 8 decoder means that out of 8 only one of them will be made active. So, it is called 1 of 8 decoder. So, naturally since output there are 8 outputs. So, we must have the input as 3 3 bit the 3 input lines should be there. So, this way there are varies names for the circuit.

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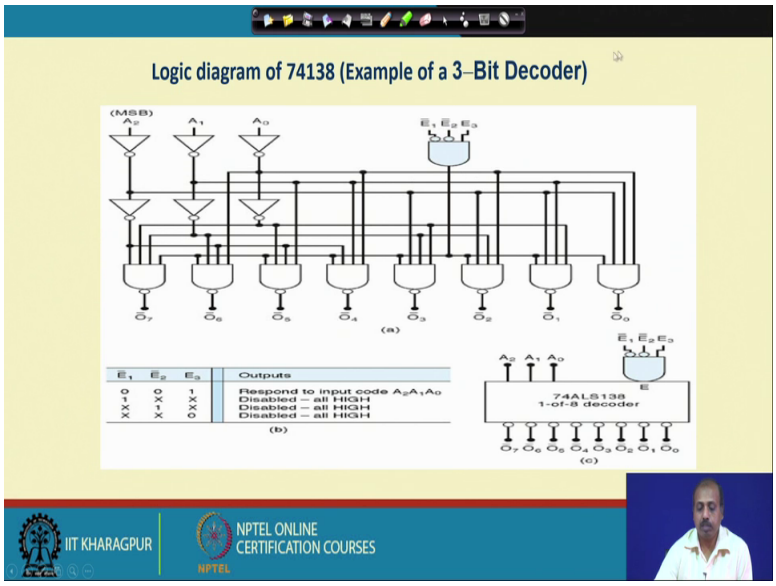

So, next we will look into the logic diagram of this integrated circuit chip 7 4 1 3 8. So, this 7 4 1 3 8 is a 3 bit decoder. So, we have got A 0 A 1 A 2 as the input and, it is when this so, it has got a number of enable line. So, this E 1 E 2 and E 3, there are 3 enable lines out of that the circuit is active when E 1 bar is E 1 equal to 0 that is E 1 bar equal to 1 E 2 equal to 0 that is E 2 bar equal to 1 and E 3 equal to 1.

In that case this AND gate output will be 1 and only when this AND gate output is 1. So, this NAND gates are there and their output can be made equal to the proper value. If this if this AND gate output is 0, then this all the outputs are tied to 1 ok. So, all this 8 outputs are tied to 1. So, for getting the operation from the circuit I should set E 1 equal to 0 E 2 equal to 0 and E 3 equal to 1, then only this will have.

So, apparently it seems why do we need so, many enable line. So, E 0 E 1 E 2 and E 3 so, this helps in the logic design many time. So, may be in a minimize circuit I have got several decoders and, the same input combination is going to a number of decoders and, but I do not want or them to be active simultaneously.

So, this availability of this multiple enable line so, it helps in the process ok. So, that is why the 7 4 1 3 8 has got a structure like this.

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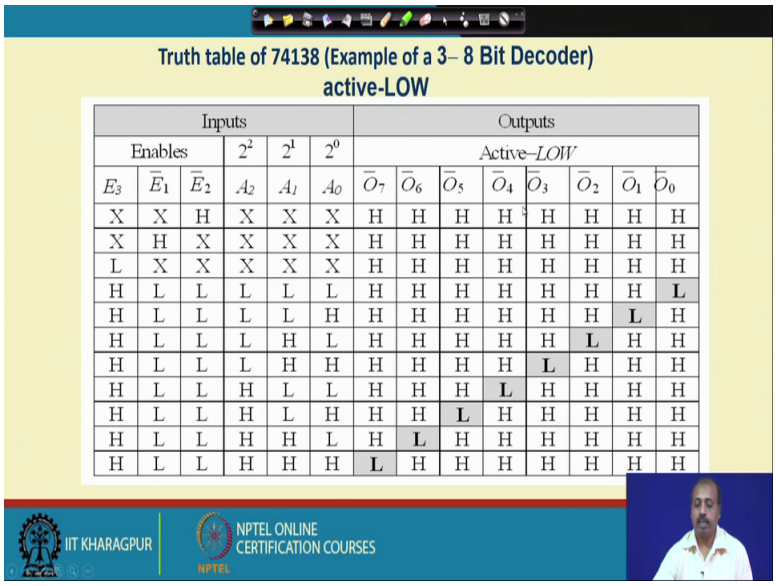

Inputs						Outputs							
Enables			2^2	2^1	2^0	Active–*LOW*							
E_3	$\overline{E}_1$	$\overline{E}_2$	A_2	A_1	A_0	$\overline{O}_7$	$\overline{O}_6$	$\overline{O}_5$	$\overline{O}_4$	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H	**L**
H	L	L	L	L	H	H	H	H	H	H	H	**L**	H
H	L	L	L	H	L	H	H	H	H	H	**L**	H	H
H	L	L	L	H	H	H	H	H	H	**L**	H	H	H
H	L	L	H	L	L	H	H	H	**L**	H	H	H	H
H	L	L	H	L	H	H	H	**L**	H	H	H	H	H
H	L	L	H	H	L	H	**L**	H	H	H	H	H	H
H	L	L	H	H	H	**L**	H	H	H	H	H	H	H

So, this is the truth table for 7 4 1 3 8. So, this is when this E 3 is so, when whenever this is a E 2 is high. So, E 2 bar becomes low so, this your decoder is disable. So, all the outputs are high, or if E 1 is high whatever be the value of E 3 and E 2, then also all the outputs are high. And if E 3 is low whatever be the value of E 1 and E 2 so, again all the values are all the all the outputs are high.

So, there is no priority between E 1 E 2 E 3 so, say for correct operation of the circuit E 3 should be high E 1 should be low and E 2 should be low. Once I have put this values so, rest of the bits A 0 A 1 A 2, if it is if the all of them are low, then O 0 bar will be low and rest will be high. Similarly if this is if I put this A A 1 and A 2 as 0 and A 0 as 1 so, this will be putting O 1 bar to be O 1 line to low and rest of the lines to high. So, this is the 7 4 1 3 8 3 to 8 bit decoder which is an active low 1 of 8 decoder.

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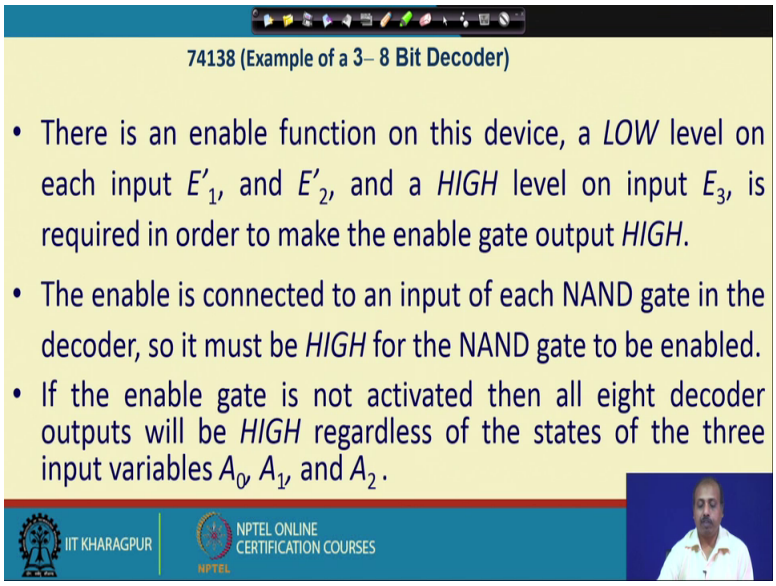

So, there is an enable function on this device a low level on each of the E 1 dash, E 2 dash, and E 2 dash and a high level on input E 3 is required to make the enable gate output high and the enable is connected to an input of each NAND gate in the decoder. So, it must be high for the NAND gate to be enabled, if the enable gate is not activated, then all the 8 decoder outputs will be high, regard less of the states of the 3 input variables A 0, A 1, A 2. So, that is for the enable part.

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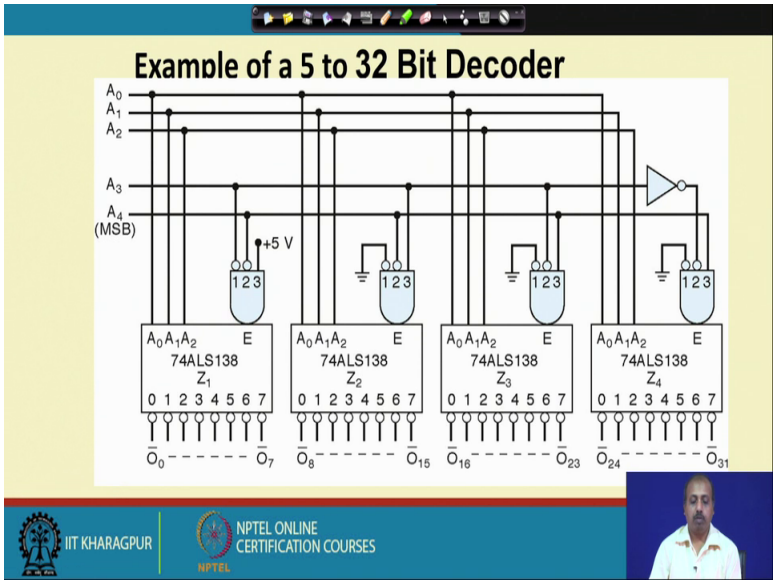

Next we will look into how can I make a five to 32 bit decoder using this 3 to 8 decoders ok. So, so, I want to make a hierarchical structure so, in my application I need a 5 to 32 decoder whereas, in my library I do not have this 5 to 32 decoders available as a chip, what I have are only 3 to 8 decoders 7 4 1 3 8.

So, what we can do? So, since there are 32 outputs. So, I will need four such 7 4 1 3 8 chips. So, these are the 4 such 7 4 1 3 8 chips. Now, since there are 5 input lines. So, this A 0 to A 4 so, these are the input lines that I have. Now, this A 0, A 1, A 2 so, they are fade to A 0, A 1, A 2 of all the 3 all the 4 decoders all the 4 7 4 1 3 8's.

Now, using this A 3 and A 4 we select between the 7 4 1 3 8 that we want for example, the first the first 7 4 1 3 8 chip that I have put. So, that controls the outputs O 0 to O 7 second 7 4 1 3 8 controls the outputs O 8 to O 15 so, third one O 16 to O 20 3 and a forth one O 24 to O 21.

Now, what is required is if all this A 0, A 1, A 2, A 3, A 4 are 0, in that case only this O 0 bar should be low and all the all these output still O 3 1 bar they should be high. Now, how to do that so, this A 0, A 1, A 2 is fade here. So, these enable line so, we connect A 3, A 4 and this the other the E 3 line. So, E 3 line will tied to high and this E 1 and E 2 so, we connect this A 3 and A 4 so, when this so this enable E is active A 3 equal to 0 A 4 equal to 0 and this is already 1. So, this is so this, the decoder will be active, when A 3 equal to 0 and A 4 equal to 0.

For the second decoder what we have done, we have connected the line A 3 to E 3 and then and A 4 to E 2 and the E 1 line we have grounded so this is so, E 1 is always there but if I give A 4 equal to 0 and A 3 equal to 1 ok. If I give A 3 equal to 1 and A 4 equal to 0. Then this decoder will get selected. So, this enable will be active and all the enables will be deactive. So, as a result all other outputs will be high, but depending upon the value of A 0, A 1, A 2 one of the outputs from this set will be low.

So, you see that I do not need any extra I do not need any extra gate, only thing is that we can just apply this E 3, E 1, E 2 properly ok. So, E 3, E 3, E 2, E 1 properly so, that this decoders will be this 4 to 8 decoders, they can be used to construct 5 to 32 decoder. So, that is why we have got this multiple number of enable lines.

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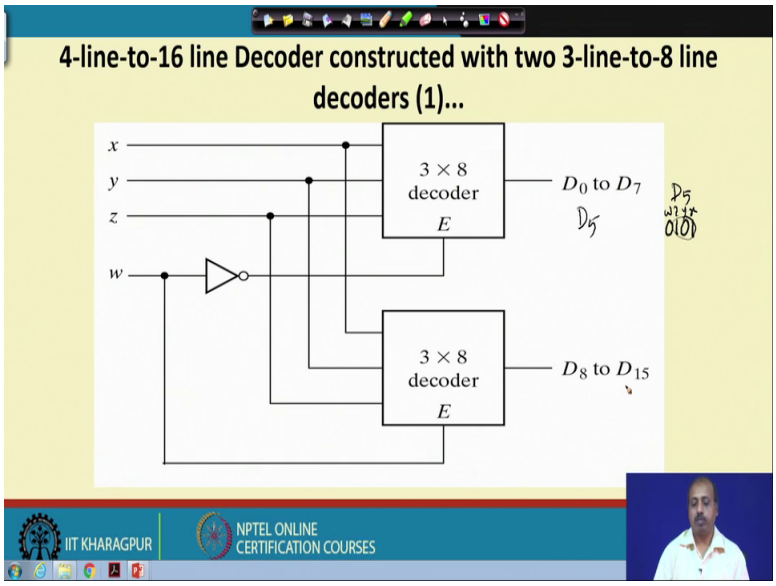

A simpler example how to construct a 4 line to 16 line decoder using 2 3 line to 8 line decoders so, we have got two 3 to 8 decoders and we use them to get a 4 to 16 line decoder. So, we assume that each of this decoders they have got one enable line and, for the decoder to operate this enable line should be equal to 1 ok.

So, this x y z so, these are the 3 inputs coming, now there is another input w so, w is the most significant bit. So, and x is the least significant bit so this x y z line. So, they are fade to both the decoders and this w lines is so line is fade to the enable of the lower decoder and this inverted w is fade to this upper decoder.

So, this upper decoder is so, is enabled when w equal to 0 and, when w equal to one the lower decoder will be enabled. So, this I can say that for D 0 to D 7's the for 4 bit patterns that we have say for say D 5.

In 4 bit so, it is coded as 0 1 0 1 so, this x y z and w so, this is x this is y this is z and this is w ok. So, this w is equal to 0; that means, the lower decoder is disabled only the upper decoder is enabled and the upper decoder in the line x y z is getting 1 0 1 as a result the D 5 output will be made high and all other outputs will be made low.

And since this lower decoder is disabled by making E equal to 0 ok. So, all the outputs will be low. So, ultimately if you look into this entire set of 16 outputs D 0 to D 15, only the D 5 output will be high and all other outputs will be low. So, in this way you can use

3 to 8 decoders to make 4 to 16 decoder, or even higher like we are previously we have said we have seen the 3 to 8 decoder used for getting 5 to 32 decoders. So, that way also we can be done.

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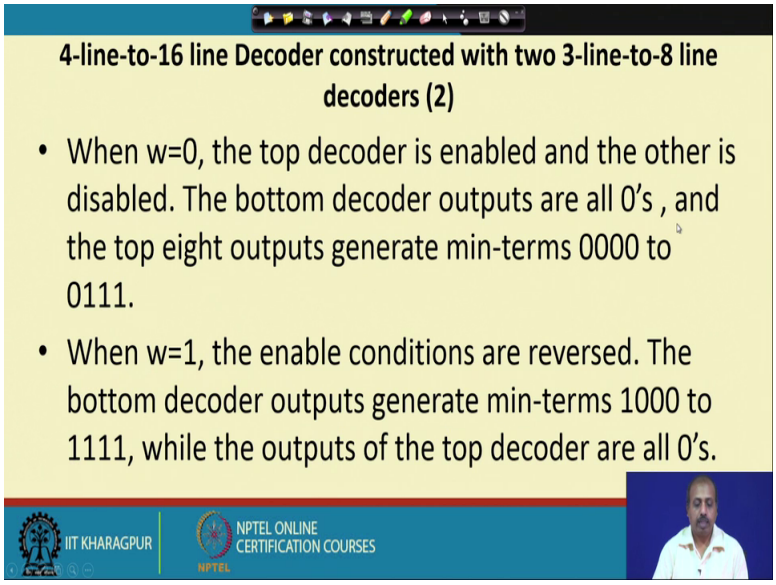

Next we will be looking into how can I get 4. So, this is the description of that 4 to 16 line decoder. So, when w equal to 0 top decoder is enabled and the other is disabled and, the bottom decoder outputs are all 0's because, the EB the enable input is 0 and, the top a and top 8 outputs generate min terms 0 0 0 0 to 0 1 1 1.

So, that is corresponding to those min terms the outputs. So, the 8 outputs will there and, when w equal to 1 the enable conditions are reversed that is the upper decoder is now disabled and the bottom decoder is now enabled. So, it will realize the functions 1 min terms 1 0 0 0 to 1 1 1 1 and upper decoder will be outputting all 0's.

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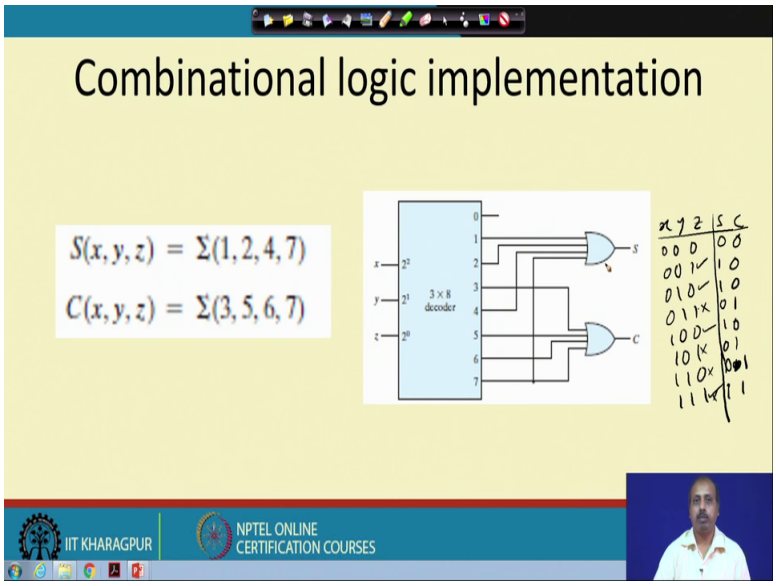

Now, this decoders they can be used for realizing combinational functions directly for example, suppose we look into that adder function ok. So, in case of adder you know that the sum is given by sigma 1 2 4 7. So, this x y z it is a full adder.

So, so if I have got full adder. So, this is the truth table so, x y and z and sum and carry. So, this is so 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 and 1 1 1. So, when this so, this is come in 0 0 1 0 1 0 0 1 1 0 0 1 1 0 and sorry sorry.

So, this is 0 1 and this is 1 1 now, first sum is 1 for this combination this combination that is 1 2 4 and 7 for this cases some is equal to 1 and the carry is equal to 1 for 3 5 6 and 7 so this. So, this is the 3 then 5 6 and 7 for this cases carry is equal to 1. So, this is the min term based representation. So, if you are trying to realize some circuit using decoder. So, first we have to come to the min term representation of the function, where it lists down the min terms corresponding to the function.

Now, so, now we use a decoder so this is a 3 to 8 decoder. So, this x y z so, they are connected to the input side. Now, output sum will be equal to 1 if the combination 1 2 4 or 7 are chosen such that is if this x y z value is such that this output 1 3 4 or 7 so, the so any of them will be equal to 1 in that case sum output will be equal to 1. And we have got this carry output. So, this will be equal to 1 if this 3 5 6 and 7 any of this outputs are 1 so, this 3 5 6 and 7 so, they are outputs are 1.

So, from the min terms, we can figure out the lines that are that are important for the function and, we or them to get the corresponding function. So, this way we can realize any combinational function by means of decoders. So, the point is that you have to convert it into min term representation and from the min term representation. So, we have to go it is not from the Karnuagh map it is from the min term representation of the function.

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So, next we will be looking into encoders. So, encoders just the reverse of decoders so, in case of encoder decoder from less number of line so, you are going to more number of lines, for the encode will do just the reverse, we will start with the more number of lines and from there we will come to less number of lines.

So, that is also useful in many cases particularly, when we are trying to reduce the amount of information that we need to said from one place to another ok. So, number of bits used for transmission and all. So, we use encoders so, that we can said more amount of information using lesser number of bits. So, we will see that in successive class.