Digital Circuits
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Lecture - 18
Logic Gates (Contd.)

Next, we will look into a more complex example of CMOS gate based combination circuit realization.

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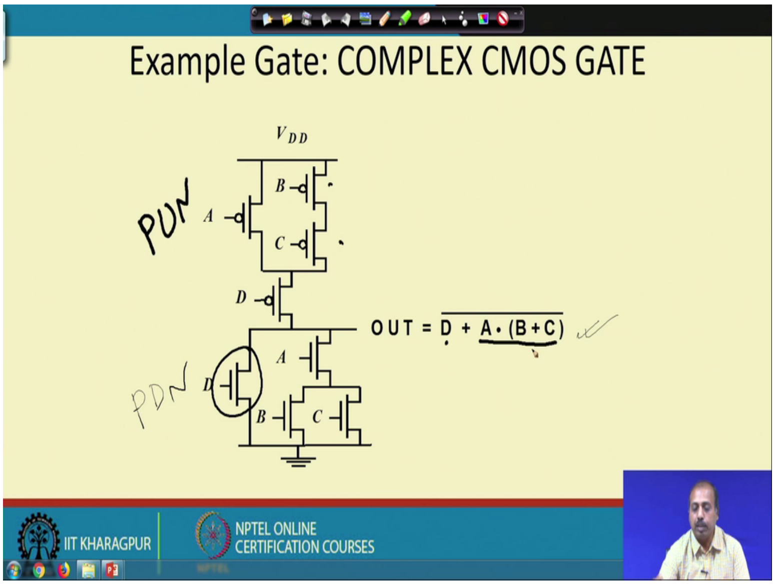

Example Gate: COMPLEX CMOS GATE

$OUT = \overline{D + \underline{A \cdot (B+C)}}$

So, let us considered the example where it is given by output is D plus D plus B into A into B plus C; say this example. Now what is said is that when you are doing it; so, we should have a N network and a P network. So, N network consists of the N type transistors which constitutes the pull down network and we have got this P type network which is which is corresponding to the pull up network. So, this is the pull up network; so, this part upper part is the pull up network lower part is the pull down network.

Now how do we realize the circuit? Now as a rule what we do is that in from the expression, we find out the some of the parallel terms like say in these expressions if you look into. So, D is one term and this A plus A into B plus C is another term. So, these 2 terms are in parallel.

So, in the N network we will have this D into D and this A into B plus C as 2 parallel branches. Like here, you see the D is one branch and that A into B plus C is in parallel with that and in A into B plus C; A A N these dot is there. So, after A the remaining part B plus C will be in series with A. So, that is what is happening; so, A is there and after that this B plus C. So, that is in series with A and B since there is a plus between B and C; so, this B and C these 2 transistors will be in parallel.

So, given any logic expression; so, you can directly draw the pull down network for every plus symbol. So, you can you can think that the corresponding portion of the circuit circuits will be in parallel to each other and whenever we have got the dot or, and so those portions will be in series with each others. Now once we have completed the pull down network now we have to draw the pull up network and for the pull up network; so, it is just the complement of the pull down network. So, whatever is in series in pull up pull down network will be in parallel in pull up network and whatever is in parallel in the pull down network will be in series in pull up network.

So, if you look into the example; so, D is in parallel with this part in the pull down network. So, in the pull up network D will be in series with the remaining part. So, that was that is what is happening similarly B and C are in parallel in the pull down network; so, in pull up network they are in series. Similarly with this B and C; A is in series in the pull up network. So, in the pull down network I will have this A in parallel with this B and C portion. So, this way we can very easily draw the CMOS transistor level diagram of any combination and logic circuit combination logic function.

So, what is required of course? The output should be in complemented form. So, output is not in a complemented form; so, you can put another inverter after this to get the function. Now to just to understand that just to get the confidence that this circuit really realizes the function that we are looking for example, in this case if D is equal to 1 then the output will be equal to 0.

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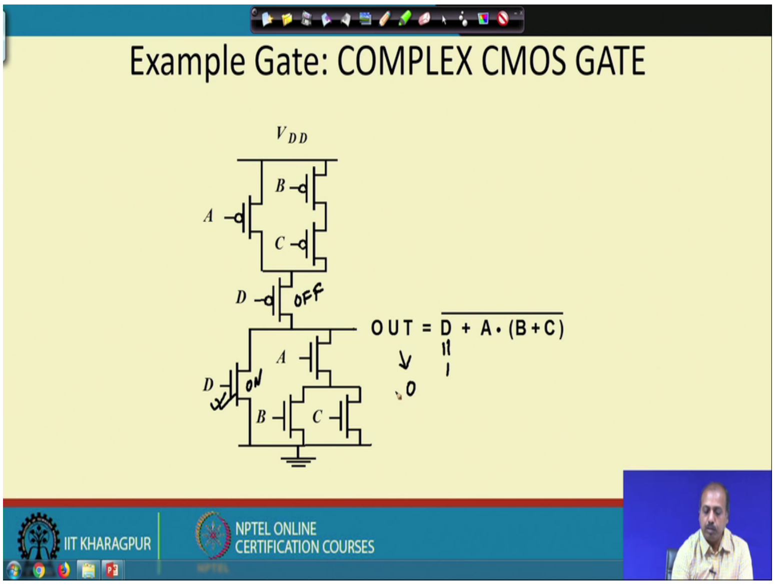
Example Gate: COMPLEX CMOS GATE

V_{DD}
A
B
C
D
off
OUT = $\overline{D + A \cdot (B+C)}$
0
1
D
on
A
B
C
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So, let us see whether this happens or not. So, you D equal to 1; so, this transistor is on ok. So, irrespective of other transistors and since D equal to 1 this transistor is off. So, this transistor is on and this transistor is off; as a result we do we cannot have a current flow path from VDD to VDD the supply voltage to the output; whereas, from output to ground there is a connection via this transistor. So, the output will become equal to 0.

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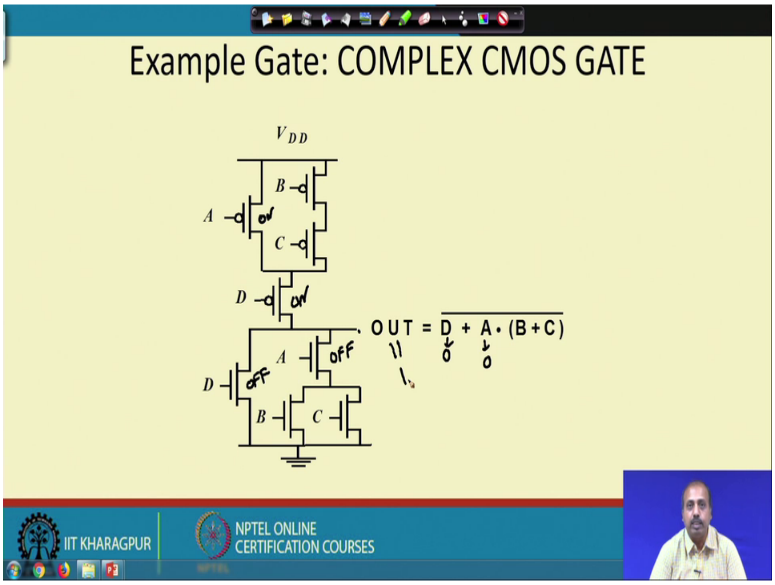
Example Gate: COMPLEX CMOS GATE

V_{DD}
A
on
B
C
D
on
OUT = $\overline{D + A \cdot (B+C)}$
1
0
0
D
off
A
off
B
C
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So, if D equal to 1 we will get a 0 here; for getting output equal to 1 what is required is these term should be equal to 0 and this whole term should be equal to 0 and for that purpose it is sufficient to put a equal to 0. So, if we put D equal to 0 and A equal to 0 output should be equal to 1.

Now, you see look into this circuit if D equal to 0 and A equal to 0; so, this transistor is off and this transistor is also off this transistor is also off. Now naturally there is no current flow path from the output to the ground; so, that part it is connected. Upper side; so this A is getting a 0. So, this transistor is on and D is 0; so, this transistor is also on. So, we have got a current flow path from VDD to the output. So, naturally you will get a high at the output point. So, this will give output equal to 1.

So, in this way using complex CMOS gates; so, we can realize combinational functions very easily.

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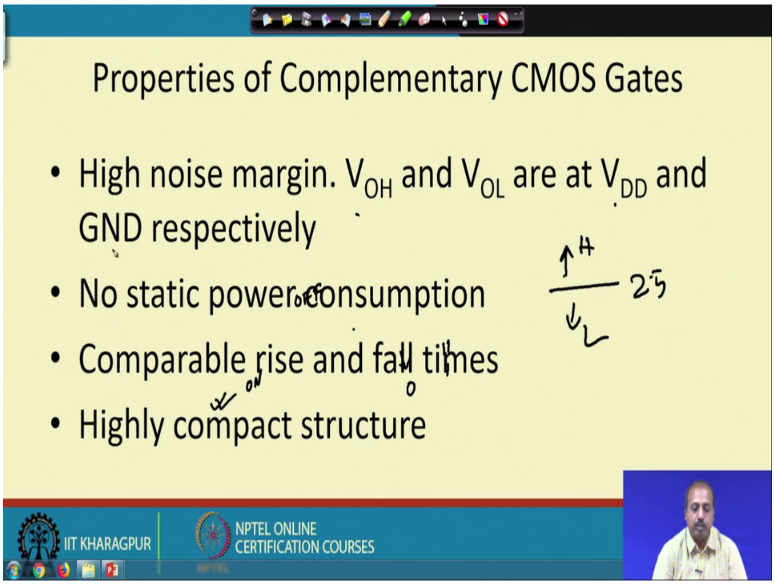

Properties of Complementary CMOS Gates

- High noise margin. V_{OH} and V_{OL} are at V_{DD} and GND respectively
- No static power consumption
- Comparable rise and fall times
- Highly compact structure

So, next we will look in to the properties of this complementary CMOS gates why is it so popular? So, it has got high noise margin we will explain this term in the next few slides VOH. So, VOH means what is the output voltage level when we have which we are considering to be high.

So, we have got VDD that is the supply voltage which may be close to say 5 volts and VSS or ground which is say equal to 0 volt. Now you may say that anything above 2.5 is considered as logic high and any anything below set 2.5 is the logic low. So, if we put a boundary like that; so, this is 2.5 volt above this is high and above below this is low. So, the problem is that there may be noise coming into the signal lines; as a result some low may be misinterpreted as high or high may be misinterpreted as low.

So, normally what we have is this VOH is the voltage level above which we will consider the output to be high. And VOL is the voltage level below which we will consider the output to be low and in case of CMOS. This VOH is at VDD and VOL is at ground. So, they are at they are maximum values, ok. So, VOH can at most go up to VDD and VOL can be a minimum be ground. So, both the things are satisfied; so, this has got a very high noise margin.

So, we will explain noise margin in the next slide; there is no static power consumption there is no static power consumption as we are said that when this CMOS gates are in work, then there is never a current flowing path from VDD to ground. So, at any point of time either the pull up network is on either the pull up network is off or the pull down network is off. So, it is never simultaneously both the networks are on; so, naturally there is never a current flow path from VDD to ground in the static condition. So, there is no static power consumption CMOS consumes very less power.

Comparable rise and fall times so rise time means that if you apply if you are input changes from say 0 to 1 how much time the outputs takes to rise from 0 to 1; so, that is the rise time. Similarly fall time means when the input changes from say input makes a change and the output should go from 1 to 0. So, how much time it takes to go to go from 1 to 0? So, these times are pretty small in case of CMOS gates. So, that is why this is also one of the important feature and highly compact structures.

So, you can make in a less area or less silicon area; so, you can put large number of CMOS gates that makes it area efficient.

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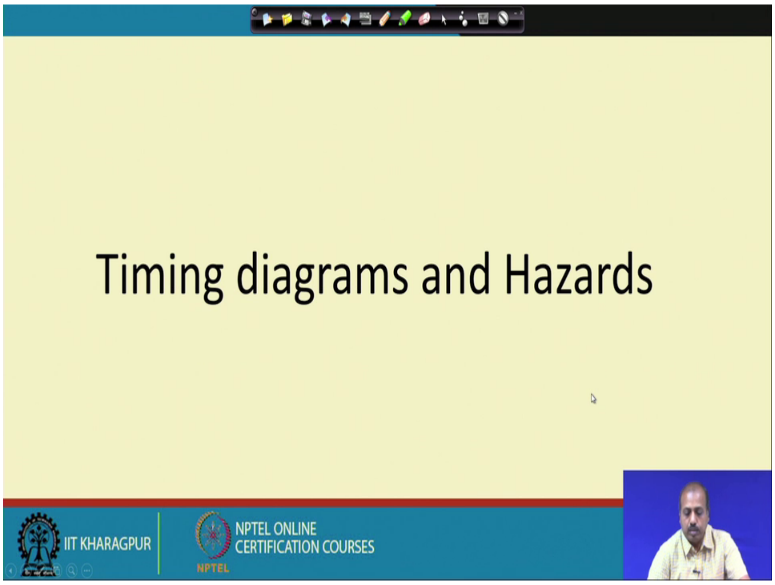

Timing diagrams and Hazards

So, next we will be looking into some timing diagrams and hazards. So, these are the two important concept that will be required for understanding the operation of this um combinational circuits.

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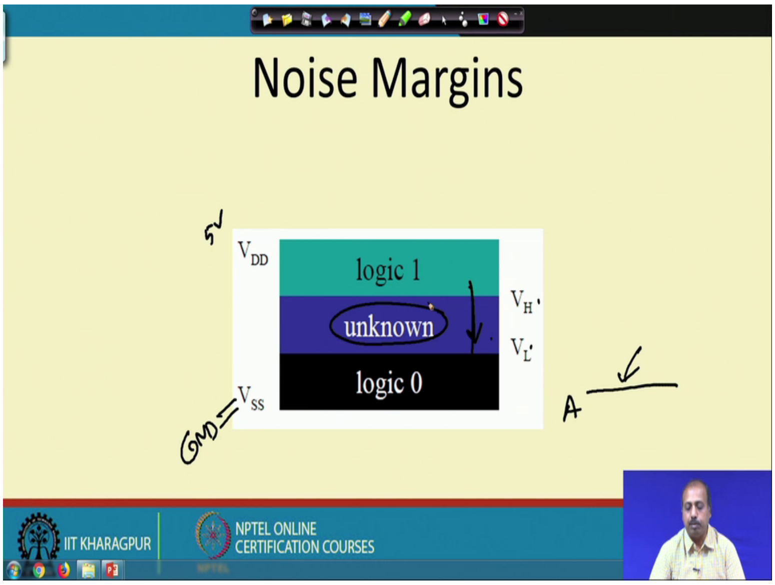

Noise Margins

So, as I was talking about noise margins see suppose this is my total range ok. So, for any gate whatever be the technology say in particular say CMOS. So, VSS; so, VSS is generally equal to ground and VDD is the maximum supply voltage that we can have DC supply voltage that we have.

So, VDD may be say equal to say 5 volt or depending upon the technology. So, this voltage will be coming down. So, for example, if we are going to say 90 nanometer technology then this will be around 1 volt and so; so that way the volt VDD value will be coming down and this is continually coming down. So, as technology is progressing; so, VDD value is continually coming down. Now my total range of voltage level that a gate output can have is from VSS to VDD.

So, out of that to keep some margin in the operation of it; so, what we do? So, we mark this 2 voltages VL and VH ok. So, anything below VL is taken as logic 0 and anything above VH is taken as logic high. If a singles state is between VL and VH; so, that is taken as an unknown level. The idea is very simple it is because of the fact that a due to noise. So, if some suppose a signal line A is at logic 0, but due to some noise coming into it; so it increases slightly.

Now if it goes beyond VL; then it will be difficult to understand like what it is. Similarly if something is VH; so, if due to noise margin it decreases further. So, if it crosses this barrier and comes to this VL region then it will be misinterpreted as a low ok.

So, this barrier or is this margin is kept so that noise cannot take a take a VH value down to VL or cannot take a VL value up to VH ok. So, that way it is it will help us in understanding the logic level sorry.

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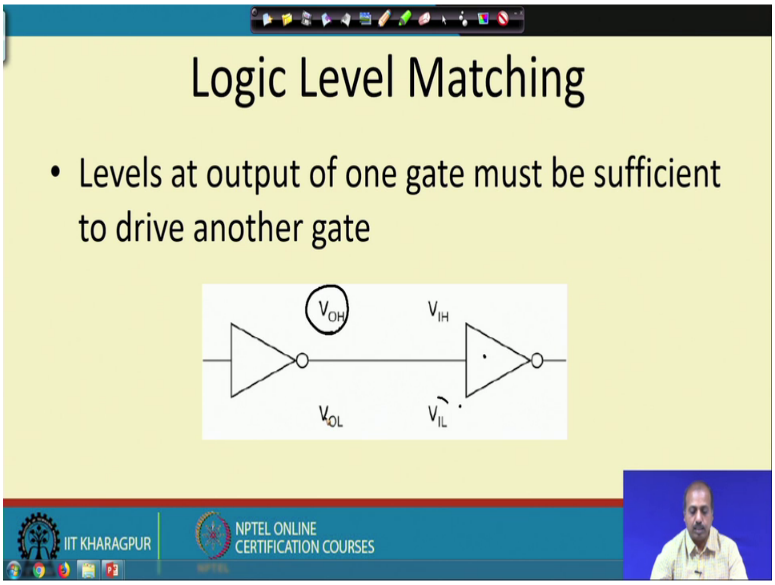

Logic Level Matching

- Levels at output of one gate must be sufficient to drive another gate

So, consider this situation like we have we have got 2 gates ok. So, both are inverters in this case, but it need not be inverter. So, output of one gate is feeding input of another gate. Now, when this gate output say high ok; this gate output say high and their voltage level is VOH these VOH should be sufficient to for the second gate to take it as high. So, if the second gate takes anything above V IH as high; so VOH must be above that.

Similarly if this second gate takes anything below V IL as low this VOL value of the first gate should be lesser then that other though otherwise there will be a misinterpretation. So, this is explained in the diagram here.

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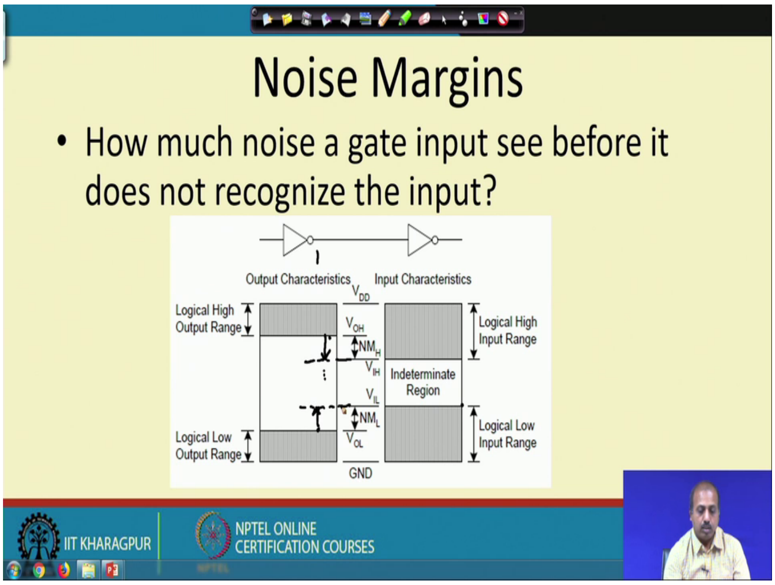

Noise Margins

- How much noise a gate input see before it does not recognize the input?

So, say for this second gate; so this is the situation. So, it takes from ground to it takes from ground to this voltage level as the logic low input range. So, that is the V IL; so, this much is the V IL for the; so, any signal coming between whose value is between 0 and V IL is taken as low by the second gate. And anything between this VDD and this V IH; so, this voltage level, so anything between these 2 voltage level that signal value is taken as logic high by the second gate.

Now, what is the condition on the first gate? So, first gate if it wants to a make an output low ok. So, it should produce a value less than V IL; similarly if it wants to produce something high it should produce voltage level which is at least equal to which is which is at least equal which is more than this V IH value; so to be on the safe site. So, what we do for the output high and low levels of the first gates. So, they are kept appropriately;

so, this output low level is kept to be lesser then this input low level of the next gate and this output high level of the first gate is kept as the as the more then the input high level of the second gate.

So, if there is a noise suppose this first gate has a output at a 1 ok. So, first gate has a output at a 1 and the voltage value is some voltage value is equal to VOH. Now if there is a noise and that noise takes this value lower than say this. So, it takes the value lower than this; so, in this region in that case in that case it will be the second gate will not be able to understand the that a it has a logic high.

Similarly, if the first gate has output at a low; so, it has output at this and due to some noise if it goes beyond this level if it goes beyond this level, but then the second gate will not be able to understand it has logic low fine.

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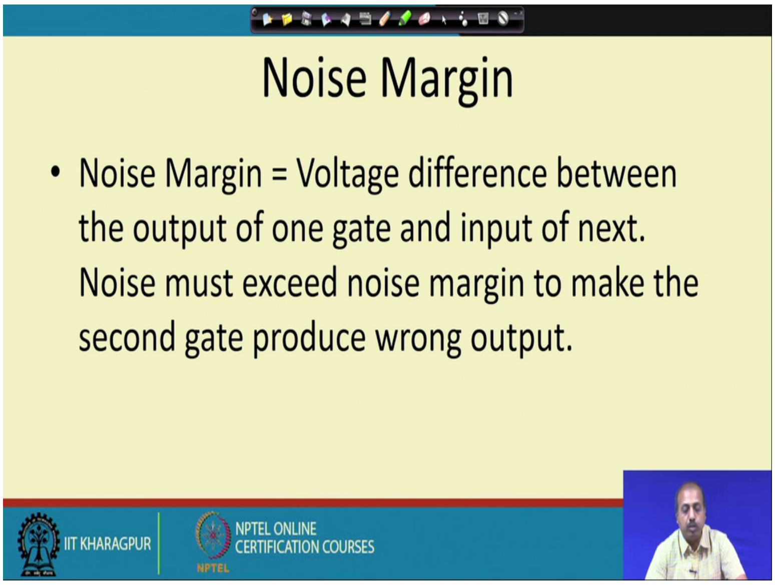
Noise Margin

- Noise Margin = Voltage difference between the output of one gate and input of next. Noise must exceed noise margin to make the second gate produce wrong output.

So, we have got this noise margin which of voltage difference between output of one gate and input of next and so, in this case; so, noise margin this noise margin high is equal to VOH minus V IH. Similarly noise margin low is V IL minus VOL. So, this way we can define this noise margins low and high and this if this noise margin is high; that means, will be more protected against the noise noisy in the noisy environment.

On the other hand if some logic family has got this noise margin low then there is a high chance of corruption in the operation of the circuit realized by in that logic family. So, noise must exceed the noise margin to make the second gate produce wrong output. So, that is the condition.

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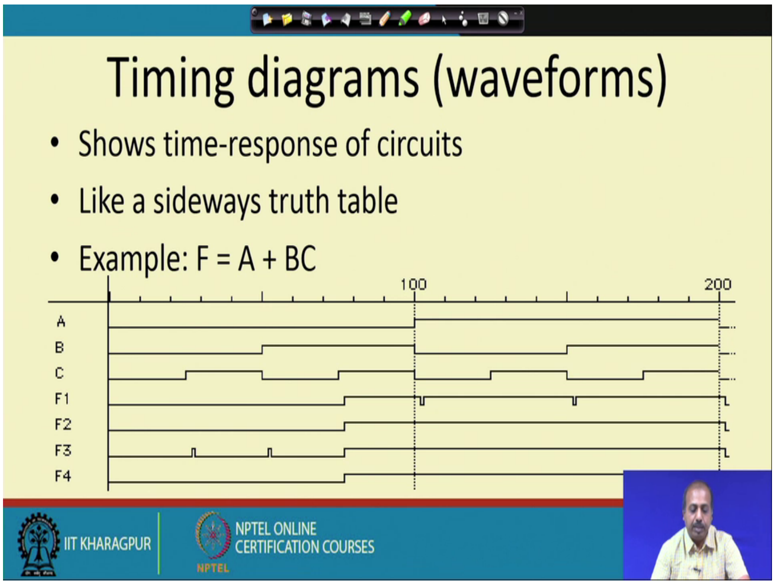

Timing diagrams (waveforms)

- Shows time-response of circuits
- Like a sideways truth table
- Example: F = A + BC

Next we look into timing diagrams; so, timing diagram this refers to the time response of the circuit. So, if you take if you take the circuit over a period of time and this input symbol, the input signals like say in this case if the function F equal to A plus B C; suppose this A B C they are changing their values in some form ok. So, in this diagram; so we have drawn the time instance and these signals A B C they are changing they are values at different times; then what happens to the output ok.

So, here this F 1, F 2, F 3, F 4; so, these are corresponding to 4 different realizations of the function that we will see shortly. So, ideally whenever this A is equal to 1; the output should be 1 ok. So, this, but you see that it if this one of the realization. So, output is temporarily showing some 0 ok; so, these are known as the hazards ok.

So, there is there is a glitch in the output. So, output is otherwise 1, but at this point it is coming down similarly as this point it is coming down. So, it can happen how can it happen; so that we will see in successive slides; why does it happen? Is that the real gates they have delays.

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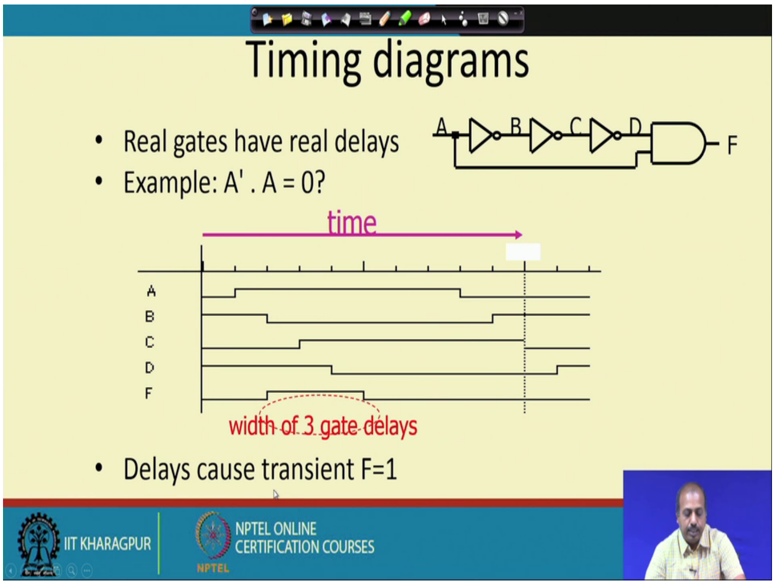

Timing diagrams

- Real gates have real delays
- Example: A' . A = 0?

- Delays cause transient F=1

So, if I have got an AND gate then the AND gate had certain delay. So, as soon as this inputs its input has a inputs are changed. So, it cannot be the output changes immediately; so, it takes some time to change. And because of that the circuit may show some intermediate behavior which is not expected. So, say in this case what we have done? We have taken an input A and it is inverted by 3 stages by 3 inverters where producing output B C and D and finally, they are ended.

So, this A; so here B equal to A bar, C equal to A, D equal to A bar; A bar and A. So, we are supposed to get F equal to 0, but due to this delay of this inverters. So, it may so happen that you get some other behavior how? See this A; suppose A is changing like this. So, A was initially low and now it is; now it is changing to high at this point it is being high this much and then it is again going low.

So, B. So, if this inverter has got some delay; so this status change of A will be reflected at output B after sometimes. So, this is the delay of one inverter if you assume like that. So, this much is the delay of one inverter; so after that time your B will be going low. Similarly at this point A is changing so after that inverter delay B will be high. Then the C output. So, this we will again this is a delayed version of delayed inverted version of B. So, this again shows the similar thing; so, as if B is delayed and inverted ok. So, we have got this symbol; this timing diagram.

D is again another delayed version like this; now, we are F is equal to D and A. So, D and A; so, in this part first part of the graph. So, A and D A is low and D is high. So, we get a 0 at this point after some time; so, after some time so, A has change the value to 1 and D is 1. So, it is expected that my output should become equal to 1.

So, it will happen after the delay of 1 AND gate; so, again this is taken as the gate delay. So, when A has become 1; so, after sometime D becomes F becomes equal to 1. So, the this is reflected at this point after the delay and then it remains high for this much of time and then D became low at this points; so after a gate delay after a gate delay; so where this F has come down.

So, we were expecting to get a constant 0 at the output F, but what you see is a in between F has become 1. So, this is called the hazard that we will see in more detail in successive slides. So, here this width of this pulse will be equal to 3 gate delays and delays they will cause a transient F equal to 1.

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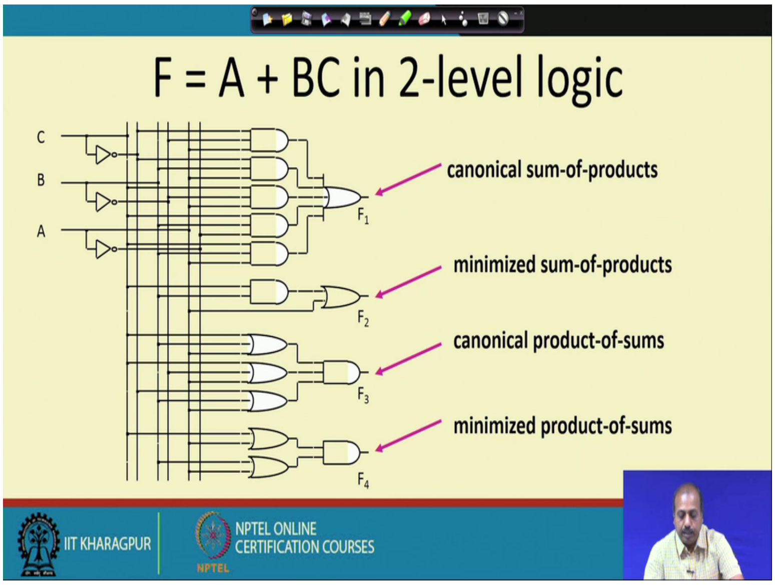

F = A + BC in 2-level logic

C
B
A
F_1
F_2
F_3
F_4
canonical sum-of-products
minimized sum-of-products
canonical product-of-sums
minimized product-of-sums
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Now, if we consider say F equal to A plus B C that function and we have got 4 different realizations of the function in the in F 1 is a canonical sum of products realization, F 2 is the minimum sum of products. So, here this A is coming; so, from this A line. So, A is connected to this OR gate and B C they are ended and that is fed to this OR gate.

So, F 2 is the minimized sum of products, F 3 is the canonical product of some form and F 4 is the minimized product of. So, these are various realizations of the function F equal to A plus B C.

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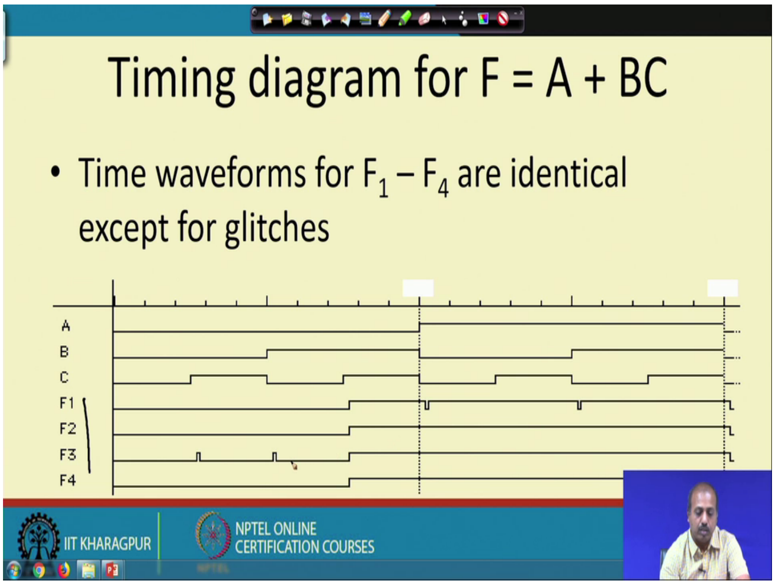

Timing diagram for F = A + BC

- Time waveforms for $F_1 - F_4$ are identical except for glitches

Now, ideally we expect that for all the realization F 1 to F 4 they should have identical waveform, because they are ultimately realizing the same function. So, we expect that they will give as the same waveform, but in reality it does not happen. So there are some glitches; so, if we look into this F 1, F 2, F 3, F 4; so, there are some there are some glitches in this F 1, F 2, F 3, F 4; there are some glitches otherwise they are same ok, otherwise all the waveforms are same.

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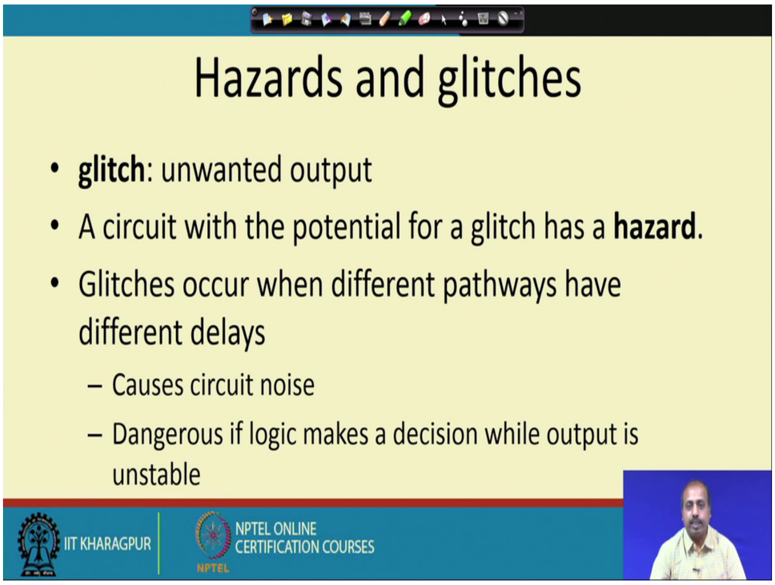

Hazards and glitches

- **glitch**: unwanted output
- A circuit with the potential for a glitch has a **hazard**.
- Glitches occur when different pathways have different delays
  - Causes circuit noise
  - Dangerous if logic makes a decision while output is unstable

So, we will go to the topic called hazards and glitches. So, glitch is unwanted output; so, output should be say steady one in between it becomes a 0 for a very small amount of time and again it goes to 1. So, a circuit that has got the potential to have potential for a glitch said to have a hazard; so, it is ideal it is expected that my circuit should be hazard free. Glitches will occur when different paths have different delays to the output if different paths have got different delays from the input; then the glitches may occur. And it causes circuit noise and dangerous if logic makes a decision while output is unstable. So, your say combinational circuit has got a hazard.

So, the output is not stable in between and at that time if we take a decision based on the output of the circuit so that is the incorrect. So, that creates some that creates the problem. So, that has to be; so, this glitches and are to be avoided as for as practical way. So, how do we do it?

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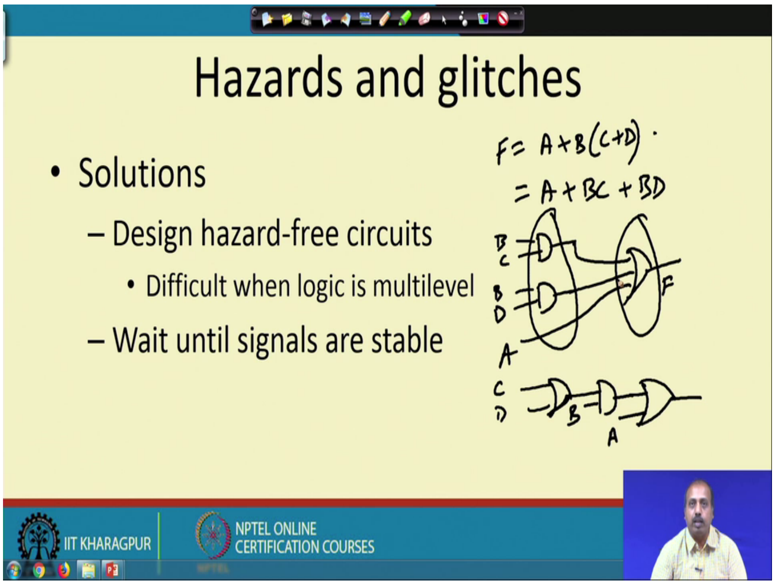

Hazards and glitches

- Solutions
  - Design hazard-free circuits
    - Difficult when logic is multilevel
  - Wait until signals are stable

$F = A + B(C+D)$

$= A + BC + BD$

So, we design hazard free circuits ok; so, this is one possibility somehow we do modify the circuit. So, that it becomes hazard free; however, it is difficult when we are doing a multi level realization. So, any combinational circuit they can be realized in 2 form one is called 2 level another is called multi level. In 2 level realization we have got only 2 level one AND level and one OR level or and one OR level and one AND level like that. So, I will whereas, for multi level circuits like say if I have got a function F equal to A plus B into C plus D ok. So, this is nothing, but the circuit a function A plus B C plus B D.

Now, if I realize it like this then what I do? I have got one AND gate which is B C another AND gate which is B D and then we have got an OR gate where we have got this line this line and A connected; so, this is F. So, this realization has got 2 level the first level consist of the AND gate gates second level consist of the OR gate. Now if you think about say this realization then it can also be realized like this. So, first we do an OR of C and D. So, this is C or D; so, this is anded with B and then it is finally, ored with A.

So, this circuit has got 3 levels ok; so, if you go by level by level. So, this circuit has got 3 levels perhaps the first circuit has got 2 level. So, these are multi level circuit; so, whatever we will discuss regard with respect to this hazard and glitches so, they are valid for 2 level circuits.

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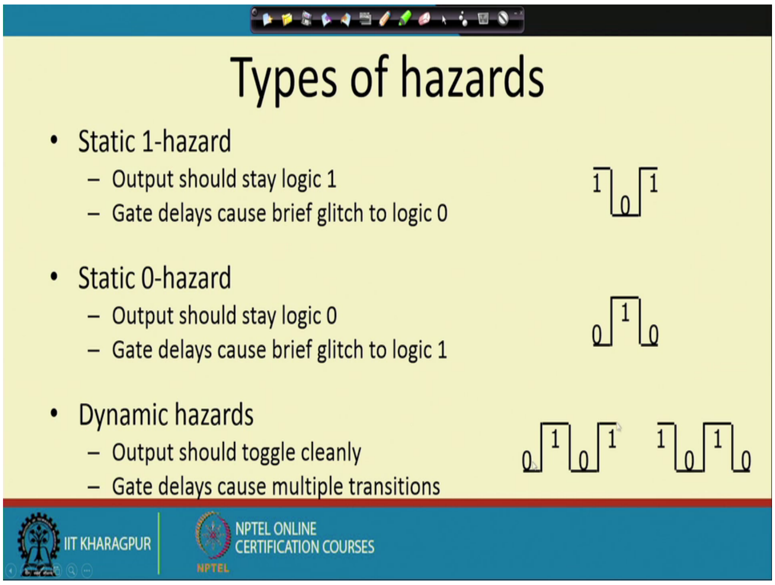

Types of hazards

- Static 1-hazard
  - Output should stay logic 1
  - Gate delays cause brief glitch to logic 0
- Static 0-hazard
  - Output should stay logic 0
  - Gate delays cause brief glitch to logic 1
- Dynamic hazards
  - Output should toggle cleanly
  - Gate delays cause multiple transitions

For multi level circuits, it is very difficult to have this hazard problem solved.

So, another possibilities that we wait till the signals have becomes stable. So, there are 2 types of hazard one is known as static 1 hazard static 1 hazard means that output ideally should remain 1, but in between there is a glitch and it goes to logic 0; for some small amount of time; so this is called static one hazard. Similarly, we can have a static 0 hazards; so, static 0 hazard means the output will remain output should ideally remain 0, but in between it goes to logic high and then again comes backs to 0. So, this is the static 0 hazard and there can be a dynamic hazard.

So, dynamic hazard means the output should toggle like it should go from 0 to 1, but what happens is that instead of going from 0 to 1 directly; it makes this types of toggles, it first goes to 0 to 1 then again comes down to 0 and then again goes to 1. Or it is one the circuit should go from 1 to 0, but in between it go make some toggle, so 1 to 0 then 0 to 1 then again 1 to 0. Finally, it settles to 0, but it in between it shows some transition. So, gate delays multiple transitions are created; so, this type of hazard, so they are known as dynamic hazards.

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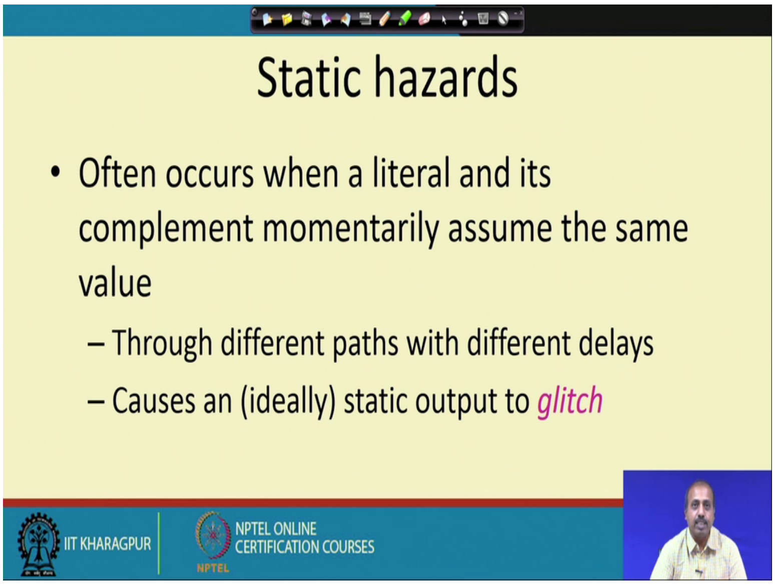

Static hazards

- Often occurs when a literal and its complement momentarily assume the same value
  - Through different paths with different delays
  - Causes an (ideally) static output to *glitch*

So, static hazards; so it often occurs when a literal and its complement momentarily assume the same value. This can happen due to the gate delays that circuit a one literal and its complement both of them are having the same value and through different paths with different delays and it cause the static output to glitch ok.

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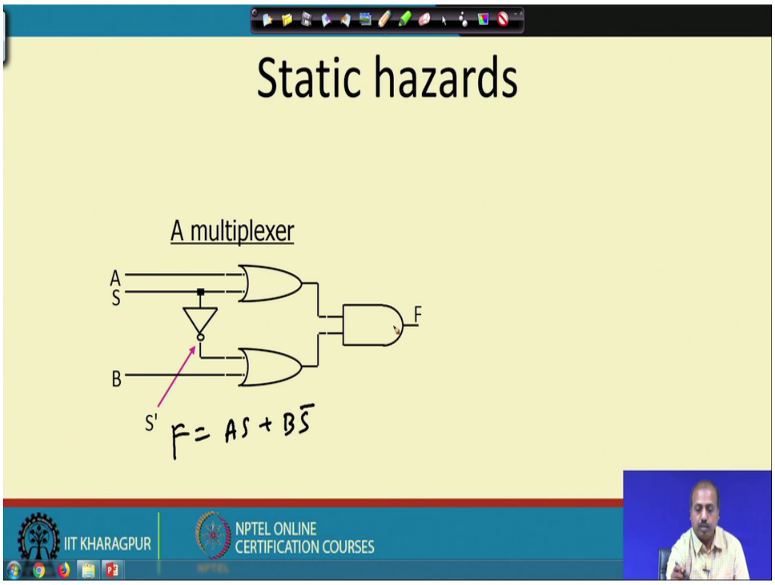

Static hazards

A multiplexer

$F = AS + B\bar{S}$

So, we will take an example suppose this is a circuit which is realizing some multiplexer.

So, here this function F is the function F is here the function F is equal to AS or BS bar. So, if S equal to 0 then this A will go to F and if S equal to 1, then this B will be then this B will be passing to F ok.

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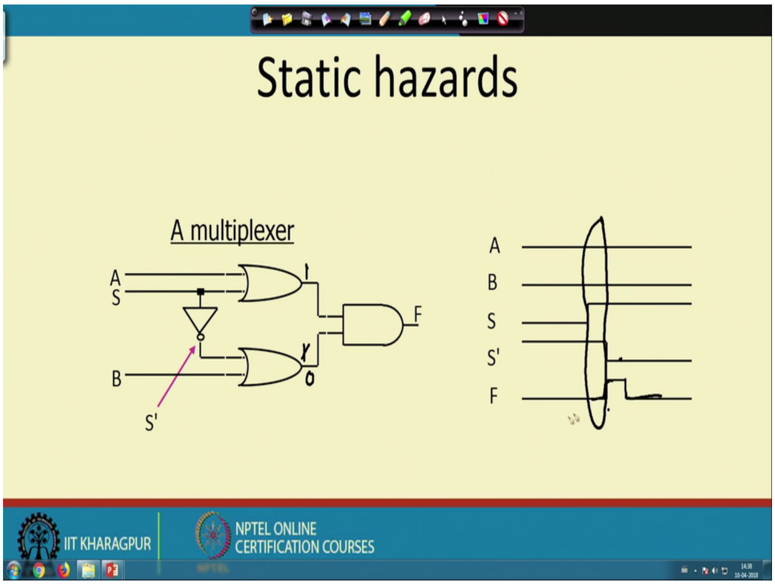

Static hazards

So,; so, if the if S, so the realization will be like this. that; so, this is the situation. But because of this because of the presence of inverter suppose A is A and B both are continually at ground and S changes its state from low to high.

Since A and B both are both are low then even if S changes its value output F should not change its status ok. Because the OR gates they should always produce 0 because A and B they are they are both at 0 and this S is selecting one of them. So, one of the OR gate output will be 0 always that that is the that is expected, but what happens you see due to the delay of this not gate. So, this S this S bar does not get the value immediately ok. So, it takes some delay and after that S; S does becomes one.

Now, for say this much for this range of time what is happening is that for the upper OR gate, we have got A is equal to 0 and S is equal to 1. So, this OR gate output is 1 in this region. So, in this region in this region A is 0 and S is 1. So, as a result it output say 1 and the lower OR gate; so it has got B equal to 0 and sorry not in this region sorry. So, if you if you take say this region, this region of operation. So, here A is 0 and S equal to 1; so, as a result output of this OR gate is 1 and for the lower OR gate B is 0 and S dash is also 1; so, here also you get a 1.

So, this AND gate inputs are 1; so, after the gate delay of this AND gate. So, you will get this signal will be going to high; after sometime this S will be becoming equal to 0. So, this lower OR gate will become equal to 0 and then after that AND gate delay. So, this will be coming down to 0; so, you see that ideally you should not have this glitch, but here in due to the presence of this glitch is appearing; so, this is a static hazard.

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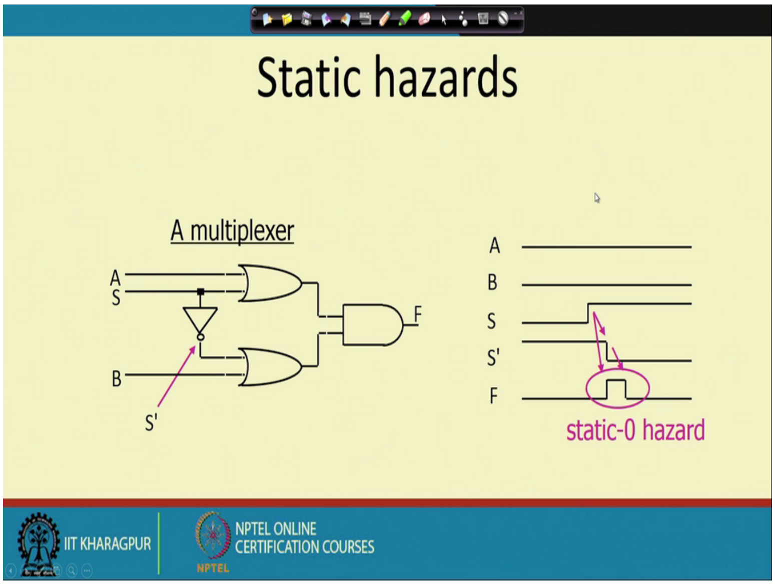

Static hazards

So, this is the static hazard that we have.

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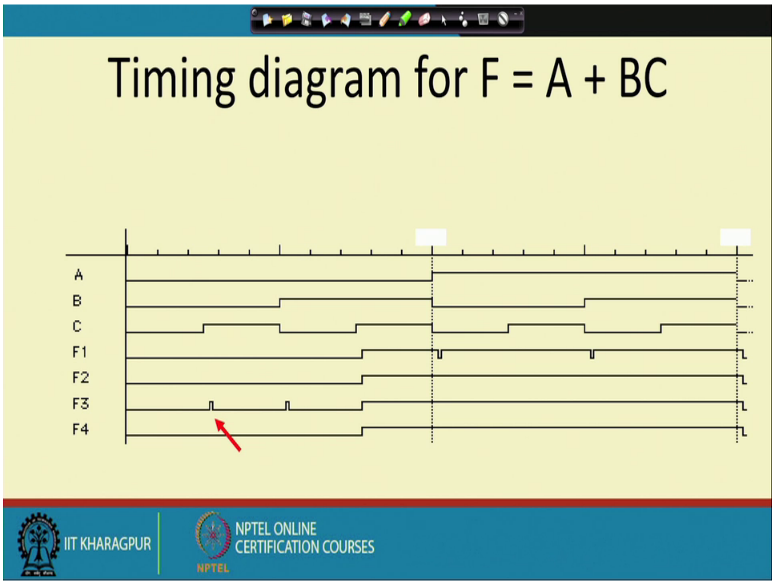

Timing diagram for F = A + BC

So, on the A plus B C function; so, there can be multiple hazard that can occur. So, we will see them for few cases.