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# Lecture - 12 The Graph Theory Approach for Electrical Circuits (Part-II)

(Refer Slide Time: 00:56)

Graph theory approach
· Identify the standard tree
All E + Max C + Max R + necessary L
• State variables : Tree capacitances + co-tree inductances.
<ul> <li>For tree capacitances, while kell for the basic cutset involving that branch.</li> </ul>
· For co-tree inductances, white KVL for the braic lost involving that branch.

In the last class we have seen that in the graph theory approach, you have a few very well defined steps one, the first step is to identify the standard tree, in any graph you can draw the trees in very, very different ways, very many different ways and out of that the one, would satisfy the requirements of being a standard tree. So, in it, what are the steps, first it should include all voltage sources, then max capacitances, plus maximum number of resistances, plus the necessary number of...

So, that is the logic of by which we go, in order to identify the standard tree, once we have identified the standard tree, then there will be a co-tree and immediately we can identify the state variables as the voltages across the tree capacitances and the currents through the co-tree inductances, so that is it. So, state variables, inductances, so we have identified the state variables, then we have to take each state variable and obtain it is differential equation.

So, if you are using if you are starting with, say a tree capacitance, so for tree capacitances, now for the tree capacitances will be in what, they will be placed in certain branches, that form the tree and you have to, for the capacitances you have to remember.

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That when we said we started with the circuit, where our the tree structure was, we started from here we took this one, we took this one, we took this one and any other thing will complete it. So, this was the tree structure and that was the co-tree structure and then when we started with this particular branch and tried to identify the equation for the tree capacitance V C 1 then what was the logic then at that time. Where do we start KCL at what?

Student: ((Refer Time: 05:23))

No.

Student: ((Refer Time: 05:26))

Yes, which cut set?

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Student: ((Refer Time: 05:30))
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The basic cut set, the basic cut set involving this particular branch, what is the basic cut set, it is a cut set that includes only one tree branch, so in this case, how would you cut it, you can cut it like this, even cut it like that, so there are various ways. So, you have no,

this is the only way to cut it, ((Refer Time: 06:48)) so for tree capacitances, write the Kirchhoff's current law for the basic cut set involving that branch and for co-tree inductances.

So, when we start with the co-tree inductance here, this one, how do we start, we start with the basic loop, involving this particular branch, what is the basic loop, the loop that contains this particular branch, but only one co-tree branch. In this case how do you write that, how do you identify that, this only one co-tree branch, a loop. For co-tree inductances, write KVL, can you see yes and that more or less completes the story.

If you start from these two premises, then you simply express the right hand sides, in terms of the state variable, that is all and that we have seen how to do. So, these are the four basic steps in obtaining the differential equations, when we write the KCL, the Kirchhoff's current law involves the currents and the current through a capacitor is C d V d t, that immediately identifies the differential part. In this case KVL will be the summation of the voltages.

Out of that one voltage will be the voltage across that inductor, where you will substitute it by L d i d t, that immediately writes the equation. So, that is the procedure and we had seen, application of this procedure in some very, simple circuits, but today let us try out on some relatively problematic cases. Say, suppose there is a circuit like this, the structure I am retaining, because that is a very good structure to illustrate things, but I am only changing the elements.

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Suppose, there is a voltage source here, there was an inductance here no problem, let it remain, there was a capacitor here, let it remain. Let us replace this resistor by a capacitor and here there was a resistor, let it remain and there was another capacitor here, let it remain. So, all that we have done is, that we have change this resistor by a capacitor, from the problem that we solved in the last class, now in this, obviously the graph will remain the same.

So, let us no, in order to draw the graph, let us first write the basic graph in thin lines and then we will go on by thick lines, as we identify the, this standard tree. Let us go ahead to identify the standard tree, now when we start, then the starting point should be the branch that contains the voltage source, so this is done include it, should include then maximum number of capacitors, so this, this. But, now the moment we try to include another branch, say this one, it completes the loop.

So, it no longer remains a tree, so we find that we are unable to include all the capacitances, so this one remains how. So, then this one becomes part of the co-tree, these are the co-tree branches, so far no problem let us go ahead with it, this was 0, 1, 2, 3 and you have the branches identified as a, b, c, d, e and f, we also have to give the directions of the currents, the assumed directions of the positivity and negativity, let us give it like this.

And as I told you in the last class, these are arbitrarily assigned directions and whenever the current actually flow in the opposite direction, it will have negative num sign. So, once we have identified this structure, how do we start, we start from, we start writing it by saying that my starting point will be say, I am writing the equation for V, this as this is my C 1, this is my C 2, this is my C 3, this is L, R, E. I am writing say for V C 1, then C 1 is here, here, I have to identify the?

Student: ((Refer Time: 13:25))

((Refer Time: 13:30)) the KCL equation with it basic cut set, so we have to identify the basic cut set that includes this, basic cut set, where is it?

Student: ((Refer Time: 13:37))

Here, so this is the basic cut set, the moment we have done that, we will write the equation as i b in going into i c minus i c minus i e is equal to 0. Notice the directions accordingly they have put, now i b, i b is what, i b is i L, i C, i C was that, c d V d t, c1 d V c 1 d t, i e this one, will we have a problem here. Nevertheless we can write it as, minus c 3 d V c 3 d t or V c 3 is not a state variable, so we need to do something about it.

Because, as we have defined it, this particular branch even though it is a capacitive branch, it was excluded from the standard tree, so it is not a state variable. So, we need to do something about this, so this is e, instead of V c 3 let us write V e because, otherwise we will may be led to believe that this state variable, so V e. Now, where do we get V e from, V e will be obtained V, is obtained from loops, so V e will be obtain from the basic loop containing this branch, where is the basic loop containing this particular branch?

Student: ((Refer Time: 15:55))

0, 2, 3, 1, 0 good, so we need to obtain V e, let us start from here, V e minus V f because it is in the opposite direction plus V a minus V c is equal to 0. So, this is the loop 2-3-1-0-2, we have written this, V e I will put in the left hand side, V e and we will shift other things in the right hand side, so is equal to V f, what is V f?

Student: ((Refer Time: 16:46))

V C 2, V a E and V c is.

Student: ((Refer Time: 16:59))

No, V C is...

Student: ((Refer Time: 17:04))

So, we now substitute it here, where do you what do we have, we are trying to write down the equations for this, so let us put that in the left hand side and the other things in the right hand side. So, this now becomes d V c 1 d t, let us keep the C 1 for now, here so is equal to i L remains minus C 3. Now, all these will be d d t of, this whole thing, we are substituting this term here from here, well expand it, i L minus C 3 d V c 2 d t plus C 3 d E d t minus, is it going out, let us take it like this here, C 3 d V c 1 d t, V c 1 is appearing in the left hand side as well in the right hand side, so we shift it here.

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 $(C_1 + C_3) \frac{d \mathcal{O}_{c_1}}{dk} = i_L - C_3 \frac{d \mathcal{O}_{c_2}}{dk} + C_3 \frac{d E}{dk} - \cdots$ For Vez if +ie-id=0  $C_2 \frac{dWe_2}{dt} + C_3 \frac{dWe}{dt} - \frac{Ud}{R} = 0$  $C_2 \frac{dU_{e2}}{dL} + C_3 \frac{d}{dL} \left( U_{e2} - E + U_{e1} \right) - \frac{1}{R} \left( U_a - U_f \right) = 0$  $(C_2 + C_3) \frac{dW_{c2}}{dt} - C_3 \frac{dE}{dt} + C_3 \frac{dW_{c1}}{dt} - \frac{1}{R}E + \frac{1}{R}W_{c2} = 0$ Using () and (), solve for dues and due

So, we get C 1 plus C 3, d V c 1 d t is equal to i L minus C 3 d V c 2 d t plus C 3 d E d t, keep it, because as at present we can do nothing about it, we wanted to obtain this, but apparently this also includes this term and this term, we are very unhappy about it, but let us proceed. So, now we write the equation for V c 2, where is Vc 2, ((Refer Time: 19:38)) here and where is the branch that takes it, it is here. So, in order to write the equation for this, we will have to obtain a cut set, that includes only this branch, so it is.

Student: ((Refer Time: 19:55))

Yes, so it is this cut set, now we will think in terms of cut set, not just the nodes, so it is this cut set. The moment you write it, we can write the equation as, it is V f going in, V f plus V e minus V d equal to 0, sorry i, cut set will be Kirchhoff's current law, i f plus i e minus i d equal to 0, i f plus i e minus i d equal to 0. What is i f, the thing that I wanted, C 2 d V C 2 d t i e, i e is what, this term plus C 3 d V e d t, you will not write it as V c 3, because it is not a state variable, V e and i d is this one, it is V d by R.

Now, we need to obtain V d, where do you should it be obtainable from V d, V d should be obtainable from the loop basic loop, including this fellow, which is this. So, we can easily write V d minus V a plus V f equal to 0, so we can simply substitute it here, again we will keep this one this side, so C 2 d V c 2 d t plus C 3, we know what V e is, we substitute it here, d d t of this whole thing, V c 2 minus E plus V c 1 minus 1 by R, V d is then V a minus V f.

Now, expand it, this appears twice, so C 2 plus C 3 d V c 2 d t minus C 3 d E d t plus C 3 d V c 1 d t minus, this 1 by R V a, E plus V f is V c 2. Again, we see that, we have arrived at a equation that includes both, so this was one equation and this was the other equation, these contains both this term and this term, this also contains this term as well as this term. So, you can use these two to eliminate, one to obtain the other, so it is two equation two unknown problems, you can easily solve to obtain this and that individually. So, that is how we obtain the equations, clear fine I am not going to do this, because you can always do that it is not a big deal, third equation there will be three things.

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For 2L 10 + 10 - 10 = 0 L diL + VeI - E =0  $= \frac{1}{L}E - \frac{1}{L}Vei$ 0

For i L, ((Refer Time: 24:58)) for i L how do you write it, it will be the KVL including this basic loop, where is it, it is...

Student: ((Refer Time: 25:07))

Yes, this one, so we will write V a, V b and V c only, so it will be V b plus V c, V b plus V c minus V a. Now, V b is L d i L d t plus V c is something that you already know, that is...

Student: ((Refer Time: 25:46))

V c 1 minus V a is minus E equal to 0, so this is simple, d i L d t is 1 by L E minus 1 by L V c 1, so this is the third equation. Notice one important aspect here, ((Refer Time: 26:15)) what did we do, because we had this particular situation where, let us physically understand why did this problem happen, that the one capacitor branch was excluded from the standard tree.

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It was because you can identify a loop, that has only capacitances and the voltage sources. When that happens, the KVL over this loop, tells you that all the capacitance voltages added together must be equal to this voltage, which is externally applied and therefore, all the capacitor voltages cannot be independent, at least one will be dependent, so which one, let us not argue about it, because any one could be. So, we in order in writing this particular standard tree, we have excluded this.

And therefore, made this as the dependent variable, notice again, that this is not the unique choice of the standard tree, we could have done it other ways. For example, instead of putting this, we could have put only these, in that case this would be the independent variable and that will become dependent variable. So, that is one thing, the other thing is that, when we ultimately went on to solve it, ((Refer Time: 27:53)) we had a couple of the equations, from which we had to algebraically solve to extract this.

This was not necessary in earlier cases, so this is the peculiarity of this situation that results from, this type of connection. Number 3, ultimately when you solve it, this term will remain in the equation, both E as well as this term, now this term says, that a equation will have to be solved ultimately by some means and that has the derivative of the externally applied force. This you might say that, it is not a big deal, yes it is a big deal, because this externally applied force could be anything.

Could be sinusoid, in which case you are happy, if you differentiate it you get a co sinusoid, but what if, it is a square wave, you can easily apply a square wave, because all that we need to do is, to connect that kind of a circuit and turn on a signal generator with a square wave input, then what. Then, this particular thing will have to be solved and when you write the program, obviously this will assume infinite values at the transition points.

So, at the transition points, this fellow will assume infinite values, your program will not be solvable and in fact, if you connect it like that, the circuit will have problems why, because this term will actually be applied across the voltages. So, there will be enormous stress, felt by the capacitances, so this tells you, that even though on the face of it, a circuit connected like this looks simple, there is no apparent reason why there is any difficulty with it, but there is a circuit theoretic difficulty with it.

If you connected really like that, then these elements will experience enormous stress, large current will flow through the capacitances and that is why, this gives us the education that we should never connect a circuit, so that anywhere in the circuit you can identify a loop, that contains only capacitances and voltage sources. If you do connect or if some way, this kind of circuit appears in some kind of a problem, then you have to do it this way. But, if you have a choice as an engineer, you should never connect the circuit like that, let us do a problem in which a similar problem occurs with inductances.

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+16+10=0

In this case, we have the circuit connected in the similar way, here in place of the resistor, let us substitute it by an inductor, here also by an inductor and here also, here a resistor and this one, let us replace it by a current source, not a voltage source, so far we have not solved a problem with a current source, so let us do this. So, this is the externally applied current I and here you have the C, here you have L 1, L 2 and L 3, here is your R.

So, 1, 2, 3, 0, it is graph is obviously the same, so let us identify the branches, again when we start the business, we have to start from, by including all the voltage sources there is no voltage source here. So, we do not bother about it, then we have to include all the or maximum number of capacitor there is only one, so we start from here. Then, we have to include the maximum number of resistors which is here, so we include this first and then the number of inductances necessary to complete it, complete the tree.

So, which one, say we could do it this way, we could do it this way, we could do it this way, but not both just one. So, let us say, we have done it this way, so the rest, then becomes the co-tree, let us put the numbers 0, 1, 2, 3 and the names a, b, c, d, e, f the directions. Now, let us start the business, we start writing it by identifying the places where we want to write down the differential equations, so differential equations at the state variables will be what, the co-tree inductances.

So, i L 1 here, is in co-tree, this one is in co-tree, so i L 3, but this one is not in the cotree, this one is not in the co-tree and therefore, the L 2 will be excluded and there is only one capacitor which is in the tree, so it will be V c only, there is no 1, 2, because there is only one capacitor. So, let us start by writing it, for i L 1, i L 1 is here, here, so we need to identify the identify what, the loop, basic loop involving this branch, where is it, it is here, so let us write it.

It is V b plus V d minus V f is equal to 0, V b is L 1 d i L 1 d t, V b is this, V d as yet we do not know, so let us take it this side, minus is equal to minus V d is L 2 d i I will write, because this not a state variable, d t and this one is plus V f is R i f. Now, at this stage, we need to identify what i f is and we need to identify what i d is, i d should be obtainable from the cut set, where only this one appear appears where is it, this whole thing here to cut.

So, we need to cut like this, in order to get this cut set out, the moment we have done that we can write, cut set a, b, d, e. So, we need we write i a plus i b minus i d minus i e is equal to 0, going from the upper sub graph to the lower sub graph is positive. So, this is plus, this is minus, this is minus, i a is I, i b is i L 1, which is a state variable we are happy, minus i d is something that we want to find out i e is.

#### Student: ((Refer Time: 38:07))

That is i L 3 is equal to 0, so we have got it, we extracted and substitute it here, we also need to find out this one i f, i f should be found from the basic cut set include, that includes this branch, where is the basic cut set, this one. So, that is obtainable as i f this way, plus i b plus i a is equal to 0, substitute these two, i b we know it is i L 1 and i a, we know it is this i, so we substitute it here.

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$$L_{1} \frac{di_{L_{1}}}{dt} = -L_{2} \frac{d}{dt} \left( I + i_{L_{1}} - i_{L_{3}} \right) + R \left( + I \overline{a} i_{L_{1}} \right)$$

$$\left( L_{1} + L_{2} \right) \frac{di_{U}}{dt} = R i_{L_{1}} - RI + L_{2} \frac{di_{D}}{dt} - L_{2} \frac{dI}{dt} - - 0$$

$$For \ i_{L_{3}} \quad U_{e} = -U_{e} + U_{d}$$

$$L_{3} \frac{du}{dt} \frac{di_{L_{3}}}{dt} = -U_{e} + L_{2} \frac{di_{d}}{dt}$$

$$= -U_{e} + L_{2} \frac{di_{d}}{dt} \left( -I + i_{L_{1}} - i_{L_{3}} \right)^{2}$$

$$\left( L_{2} + L_{3} \right) \frac{di_{L_{3}}}{dt} = -U_{e} + L_{2} \frac{di_{L_{1}}}{dt} - L_{1} \frac{dI}{dt} - 0$$

After the substitution we get, L 1 d i L 1 d t is equal to minus L 2 d d t of I plus i L 1 minus i L 3 plus R minus I plus i L 1, I will substituted. Now, expand it, you get R i L 1 minus R I, then the derivative terms plus, we can get one term this side, so it will become L 1 plus L 2 d i L 1 d t, this term goes here. So, the remaining terms are L 2 d i 3 d t minus L 2 d I d t, this is the externally applied current, again you see here we have the i L 1 d t appearing here, d i L 3 appearing here and d I d t also appearing.

In the same way, that happened for the last circuits, again we if you write down the equation for i L 3, that is a state variable.

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Let us see, i f plus i b plus i a is equal to 0, the last term we are talking about, so we wanted to find out i f, so both will be minus.

Student: ((Refer Time: 41:21))

I.

Student: ((Refer Time: 41:24))

This two will have opposite signs.

Student: ((Refer Time: 41:47))

But, this one goes to this side and it is here, so R times, minus i b, the i a is i, here, because I have given the sign, this way and here it is this way, so it is. So, for i L 3 what will you have, which i L 3 we need to identify a loop that contains this one, where is that loop, this loop, so we will write, V e is equal to minus V c plus V d. Then, we will write L 3 d i L 3 d t is equal to, what is V c, minus V c there is a state variable, so we are happy, plus V d is this term, which we can, we had the same problem here, we will extract it.

So, plus L 2 d i L 2 d t, but this term we need to substitute is exactly in the same way as you have done here. So, substituting this equation we have, I should have write written i d, when you substitute you get, is equal to minus V c plus L 2 d d t of this whole thing, which is minus I, because this minus I plus i L 1 minus i L 3. So, now you get this thing out in the same side, you have L 2 plus L 3 of d i L 3 d t is equal to minus V c plus L 2 d I d t.

Again we have this equation and this equation, we have two equation, two unknown problem, solve it and there will be another state variable which is V c, for it the equation will be trivial.

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for ve  $i_e = i_e - i_a$  $c \frac{dv_e}{v} = i_{LS} + I$ 

For V c, the equation will have to be obtained from where?

Student: ((Refer Time: 46:06))

Containing this and where is it?

Student: ((Refer Time: 46:13))

Here, this cut set, so quickly write the equation, you will write i c is equal to i e minus i a and then you will write the equation, I am not bothering about it, C d v c d t is equal to i L 3, i a it will be plus I. It is in the opposite direction, so you can easily this, get the C in the other side you get the equation well, so we have more or less understood that, in this case also you run into the same problem, ((Refer Time: 47:00)) we have the equation involving a couple of equations from which these two terms need to be extracted.

A algebraic problem can be solved, but what we end up with also will contain this and this term will mean, that the externally imposed current, will have to be differentiated in the equations, which will be difficult to solve in reality, in computer programs and in fact, when you actually connect the circuit in this way, this will cause actually a problem, because this cannot instantaneously vary. If it does, then d I d t will be applied as a voltage on this inductors.

Now, why this problem happen, can you identify why this problem happened.

#### Student: ((Refer Time: 47:55))

Yes, something forms that contains only with the current source and the inductors, this loop, current source and the inductors. Therefore all the currents in the inductors cannot remain independent variables and whenever that happens, there is a practical circuit problem and you should understand that, you should never connect the circuit like that. Further details of this kind of circuits we will come back, because these are something that is very rarely understood by electrical engineers. So, we have to understand it even more carefully, we will come back, but now let us give you a few problems to solve at home, before we go into the next kind of topic. Solve these problems.



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A source current, source voltage L R 1, R 2, C 1, C 2, number 2, there is a source here, then it is connected to resistance, to another resistance here. Here you have a resistance and then let us replace it by a capacitance, then you have another voltage source, an inductor, a resistor and may be let us connect a current source here, another voltage source, resistance. So, there are many resistances R 1, R 2, R, R 3, R 4 and this is L, this is E a, E b and E c, have you copied.

# (Refer Slide Time: 51:14)



Third problem.

Student: ((Refer Time: 51:16))

Copied, third problem you have got a voltage source connected with a capacitor, with an inductor, with another capacitor, with a resistor here and we have resistor coupling here, C 1, C 2, L, R 1, R 2, E. Have you copied, one important exercise is where, you identify the problem where, so let us first draw the circuit.

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Capacitor, supposing there is a resistor here, an inductor here, a resistor here and there is a capacitor here, will the mesh current method to be applicable to this?

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Student: ((Refer Time: 52:50))
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It will, no it will be applicable, because it is not actually a overlap, you can easily break it by moving it from there to, so whenever you has given a circuit first think, just because it shows with a overlap that does not mean it is a non planar circuit, you can it can be made a planar circuit. Sometimes, you also think about think in this line, but let us handle some truly non planar circuit, I will give you, first let us take another planar circuit.

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We have, because most circuits are actually planar, in VLSI too these days, we are starting to use non planar circuits, so you need to understand that also copied done.

Student: ((Refer Time: 54:17))

It is not visible, so this is the circuit, now I will give just one more problem to solve, which is a non planar circuit. So, this is a hopelessly non planar circuit, so by doing nothing you can get it to into a plane, so write down the graph of it and solve this problem; that is all about it today.