Course name- Analog VLSI Design (108104193)
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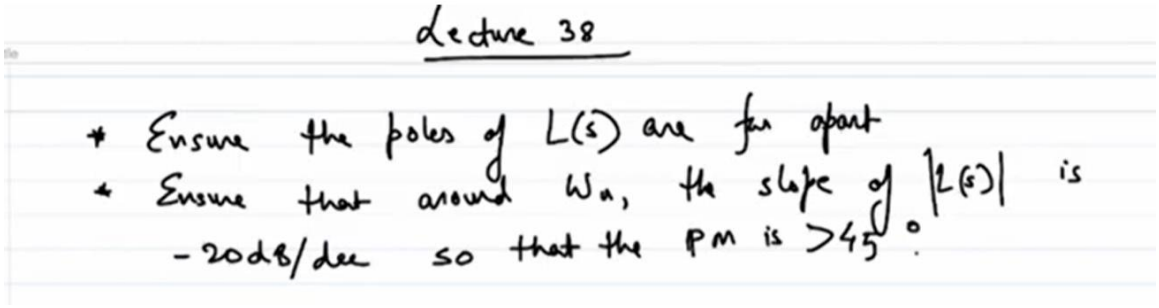
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 12
Lecture- 38, module-01

Welcome back, this is lecture 38. So, in the previous lecture we were, we, we, we dived into finding out the requirements of the loop gain to ensure that the closed-loop system is stable, not only stable, it is well-behaved right. So, so that if I if I give a step input, if I disturb it with a if I disturb the input with a step, the output does not go on ringing forever without we saw the requirements for which the output can settle smoothly right. And we then further saw that in we then further saw that if all the poles are all the poles are real right and then we further saw that the requirement was the poles could be part apart right in order to ensure that the phase margin is at least 45 degrees or above right for a second order system right. So and and we also further saw that in order to ensure that in to have a phase margin of 45 degree or above right, we had to ensure that the UGB omega U of the loop gain right fall fell under fell in that part of the curve of the loop gain where we had minus 20 dB per decade slope right. So so essentially we what we and the the the outcome of the previous lecture was ensure that the poles of L of S are far apart and second important outcome was ensure that around omega U, the slope of L of S, mod of L of S is minus 20 dB per decade so that the phase margin is greater than 45 degree right.

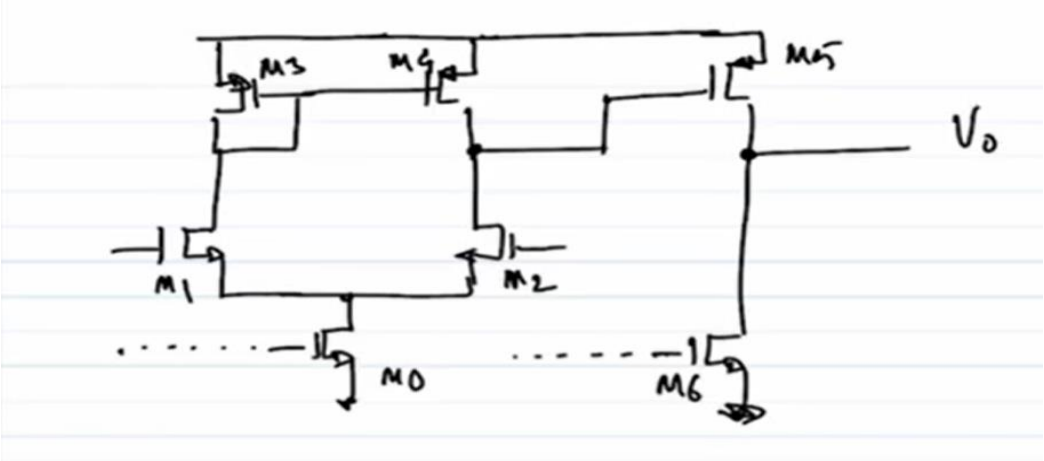
So these were the two, these were the two out two conclusions that we that, we ended up focusing on when we, when we concluded the previous lecture. So, so we will we what we will do in this lecture is we will use this and these two conclusions and we will try to see what happens in a differential amplifier



when I put the differential amplifier in a negative feedback loop right. So in other words what we are essentially saying is we have we have our differential amplifier, a two-stage differential amplifier. And we have this is biased and all those things we know.

Again this is biased I am not showing the biasing network it is in current meter for, for M0

and M6 let us say M1, M2, M3, M4, M5 let us say this is V out. Now a quick, quick refresher so let us say I want to put it put this in a unity gain negative feedback configuration where should we not connect?



V0 connect to the to the gate of M1 or gate of M2. So how do I know? So let us assume V0 is connected to the gate of M2 right. So let us assume the V0 is connected like this. So let us go about and let us go around and see whether it is indeed a negative feedback.

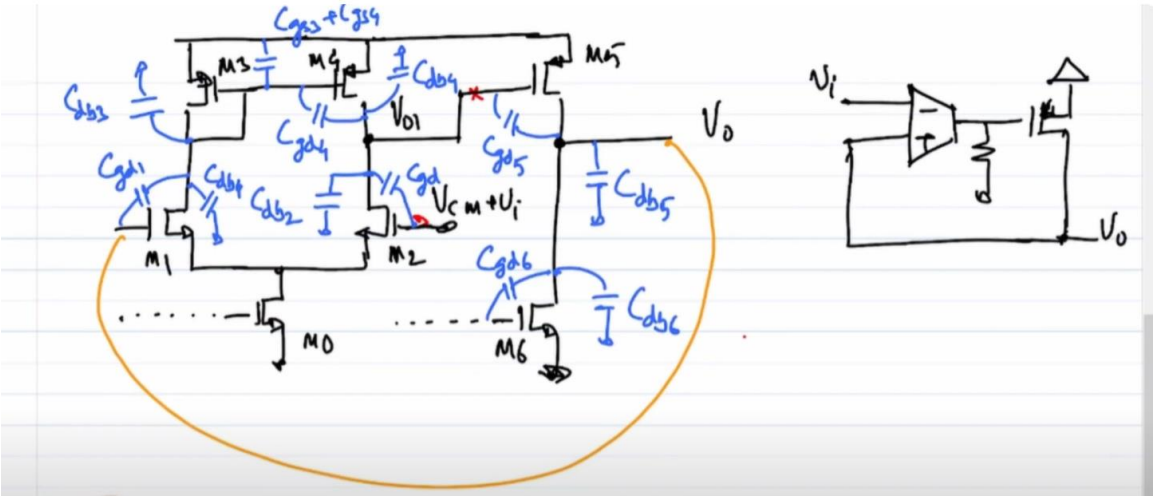
So you can break the loop anywhere. So let us say I break the loop here and apply a disturbance here. If the gate voltage of M5 goes up what is going to happen to V0? V0 is going to go down right V0 goes down this goes down which means if the gate of M2 goes down what is going to happen to the drain of M2 this guy will go up right. So clearly this is a positive feedback loop. So V0 should not be connected to the gate of M2 instead V0 should be connected to gate of M1 and we should use M2 to apply our input right Vcm plus Vi right.

So if everything works properly incremental V0 will be equal to incremental Vi because ultimately this is, this is similar to the case this is essentially incrementally this is what this loop looks like where plus this is minus this is here right. If I am going if I am talking about increment I can as well short the short the source because incrementally this is shorted and this is V0 right? If the loop gain is high Vi will be equal to V0 because the input of the error amplifier will go to 0 ok. So this is something that we that we know that we have spent time before to enhance our understanding ok. So now the question I am asking is now this is a negative feedback loop and whether the negative feedback loop is stable with adequate phase margin or not right?

So before to answer that question what we first need to find out is what are the capacitances associated with this negative feedback loop right then only we can answer that question right. So what are the capacitances associated these are all MOSFETs so all the capacitances are usual. So let us start off with which node let us start off with V0 1 this

node what all capacitances do you see here? So firstly the capacitance associated with M2 will be Cdb2 of M2 right? So there will be Cgd of M2 correct?

What about parasitic capacitance due to M4 so there will be capacitance of Cdb of 4 similarly we will have capacitance of Cgd of 4 right? What else what about the parasitic capacitance due to M3 right. So there will be a capacitance here there will be a capacitance between Cdb3 then there will be, there will be Cgs3 right because this node will have capacitance right of Cgs3 plus Cgs4 right because both the M3 and M4 are in parallel that capacitance is add up. What else you have a capacitance here to ground that is Cdb of 1 then you have capacitance Cgd1 right? What about the output side so the output side you have a capacitance here Cgd5 right then you have capacitance of Cdb5 right and maybe this is also driving a capacitive load so you will have a load resistance also associated with it right and there will be a capacitance here Cgd6 then you have a capacitance here Cgd6 right.



So this structure might seem a bit intimidating at a first sight but you will see that we can significantly simplify this structure for our benefit. So let us do that. So let us start off with the easier ones. So first let us assume that we will neglect the Cgd right that is what we have been doing till now. So let us assume we neglect Cgd.

So let us neglect Cgd for now. We will come back to Cgd later right? So let us neglect the Cgd capacitances. So let us keep this Cgd capacitance for the moment and I will try and make a point. So when we are doing a loop gain analysis what are we doing? We are breaking the loop we are applying a applying an input test input and finding out the return voltage right.

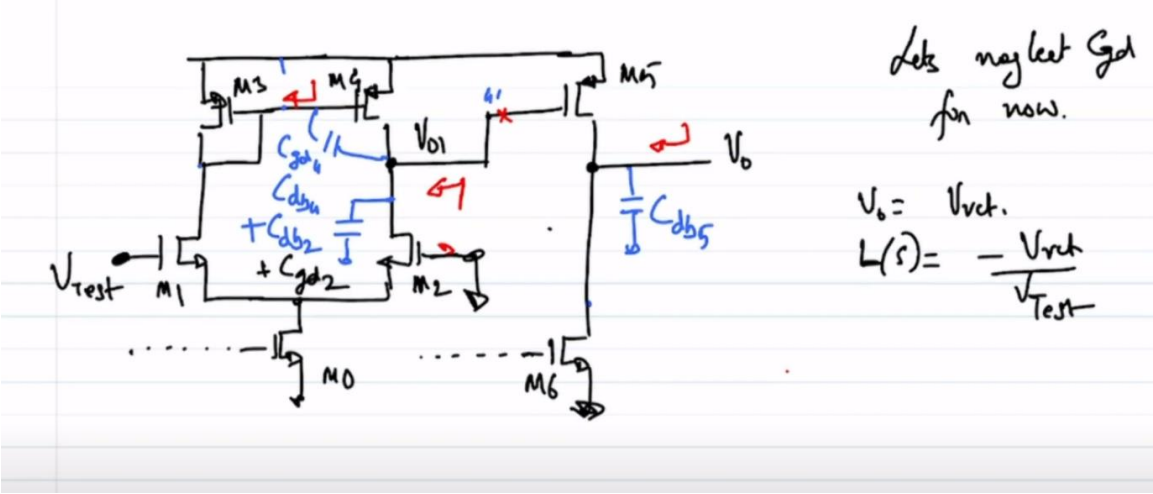
So where should I break the loop? I broke the loop here. So in the in this sense where should I break the loop? I can break I can break the loop here right? I can break the loop

there and add a test voltage test and observe the return voltage right. So that is what we are going to do. So we broke the loop right we shorted the incrementally shorted the input apply a test voltage test right and we will we are going to see what is our output because in this case V0 itself is Vreturn right in this case V0 is equal to Vreturn right.

So we are looking for minus loop gain is minus Vreturn over V dash ok fine. So if I if I concentrate on this on M2 and we saw that the Cgd I mean one of the inputs have gone the input of M2 has gotten to ground which means that Cgd capacitance is now grounded right which means it act comes in parallel to Cdb, Cdb2 right. So this let us take one at a time so that things become slightly more palatable. So this capacitance is now grounded so I can add it here Cgd2 and remove this capacitance here. The Cdb M4 right the Cdb of M4 which was here right.

So that capacitance is also to incremental ground. So I can club it with our existing capacitance Cdb4 right it gets clubbed into that existing capacitance what about what about this Cgd? Cgd4 right. So in order to understand what is going to happen to Cgd4 let us let us try to figure out what is the impedance looking in here. What is the impedance looking into the gate of M3? Note that I am looking into the gate of M3 where the M3 is diode connected right. So what is the impedance? The impedance is 1 over gm3 right?

Now what is the impedance at what is the what is the impedance or what is the resistance looking into V01? What is the order of the impedance? The order of the impedance looking into V01 is rds4 parallel rds2 right. So similarly what is the order of the impedance looking into the output node? Again it is rds5 parallel rds6 right. So you see that there are there are there are 2 high impedance 2 nodes where they are looking in impedance or the where the resistance the incremental resistance is that of the order of rds right which essentially means that they are going to dominate the poles because typically what are poles?



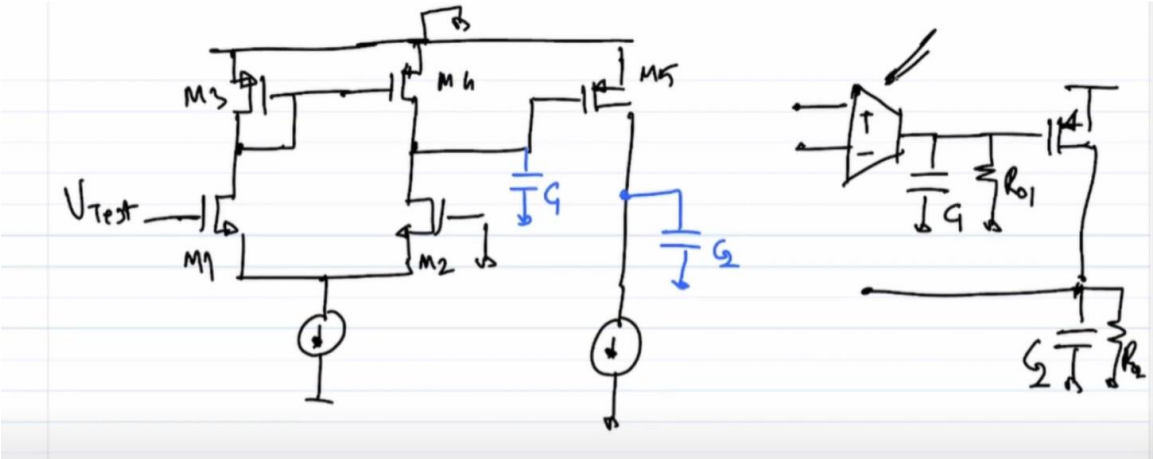
Poles are 1 over time constant if for cost error systems right. If I can break this up into cost error system the poles are 1 over time constant and lower the time constant means or rather higher the time constant means lower the poles which means they are the ones that are going to dominate the transfer function. So we did not bother about at least we did not bother too much about high frequency poles which means a pole associated with 1 over gm right whose conductance is 1 over gm we can safely neglect right.

So it essentially means that the Cgd4 we can assume to be also grounded right because ultimately 1 over gm can be so since 1 over gm is much much less than rds right. So we can assume Cgd5, this is Cgd4 is connected between Vnot1 and ground right. So if that is the case we can add up Cgd4 here also right okay? And we will neglect and also neglect poles associated or rather also neglect time constants associated with 1 over gm right. So essentially though even though we know some pole exist right they in fact can affect our transfer function to make our life easy we will neglect that right.

So essentially we are neglecting the pole associated with we are neglecting the poles associated with the node Vp3 okay. So they are gone okay fine what else? So another important thing is when we had when this guy was connected right when the loop was connected Vnot was seeing Vnot was seeing the Cgs of M1 right. Vnot was seeing the Cgs, I mean Cgs of M1 which means that if I have to find out if I have to ensure that the loop, the loop can actually deflects the behavior of a closed loop property I should ensure that even after breaking the loop Vnot is loaded with Vnot is loaded with the capacitance of M1 right. So which essentially means that I should add Cgs1 here right in principle I should add but I will not add here because ultimately we know that this guy will be I will be driving some capacitive load let me call it C2 right?

So I will be, I will be driving some capacitive load essentially what I am saying some capacitance C2 will be, will be driving some capacitance C2 since we will be driving some capacitance C2 and in general that order of magnitude of C2 should be much higher than the internal capacitance of the op-amp right in general not always but in general. So we can basically neglect whatever other capacitances that are associated with the node right? So we will just simply say that the total capacitance at this node is C2 okay. Fine, what else? So it seems like now seems like after making all those approximations right after also we will have a capacitance here Cdb that Cdb can be absorbed into C2 right. Also, we will have a capacitance here Cgd but Cgd can also be absorbed into the into the capacitance C2 why because ultimately this guy comes from an ultimately I will be having some current mirror right ultimately I will be having some current mirror which means that the looking in impedance becomes 1 over gm which means that I can for practical purposes I can assume that input impedance is low so Cgd can be grounded right.

So whole purpose of this making this approximation is to get rid of as many extra nodes as we can so that we can minimize our effort right without making too much of a too much of a error okay. So essentially what ends up happening is this. Let us assume this is ideal current source because it does not affect our analysis here and we are applying we test here this is rounded again incrementally and we have an effective capacitance some clubbed into this effective capacitance and we have this effective capacitance and we call this C1 and we have some effective capacitance we call this C2 correct. So in other words in a block dynamic form what do I see? What do I see? I see that I have a voltage control current source right whose output is loaded with some capacitance C1 and obviously it has some output Rout1 right and this is the here I have C2 and obviously there is some Rout1 right okay. And what about the signs of the voltage control current source of this guy? So clearly this has to be positive this is negative because we have to connect it like this output goes to the positive terminal to make the loop overall negative feedback.

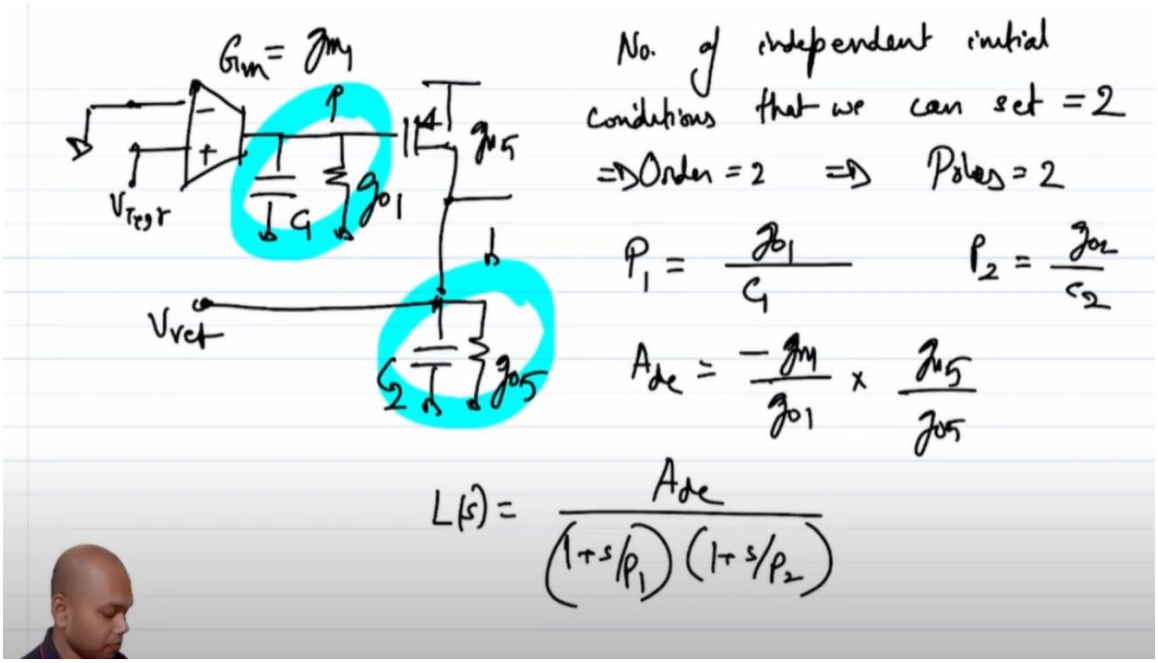


So this guy goes to ground and we will apply Vtest here and this is our Vreturn right and we will have a overall gm for this and this overall gm is gm1 right gm of the transistor m1 right and what is Rout1? Rout1 is rds4 parallel rds2 right. What is Rout2? Rout2 is rds5 parallel rds6 right. So this is supposed to be m6 right okay and C1 and C2 we spent some time understanding right? The reason we are simplifying this is because we are comfortable in dealing with circuits which are which we do not have like 10 transistors at a time right? So we are simplifying the entire analysis okay.

So let us analyze the block diagrammatic transfer function now and then see where we end up right. So what is the order of the system? Clearly the order of the system is 2 right? Clearly the order of the system is 2. We have 2 capacitors right. We have 2 capacitors we can set and how many number of initial conditions that I can set on a capacitor? So number the number of independent initial conditions in the net initial condition also initial voltage initial conditions that we can set in this case is 2 right?

We can set we can set 2 initial voltages on C1 and C2 independently of each other which essentially means that there are 2 differential equations 2 independent differential equations which means the order of the system is 2 right. So that is what that is what it means. So the order of the system is 2 implies order equal to 2 implies we will have 2 poles number of poles it will be poles is equal to 2 right? So what is the pole location? What is the first pole the pole associated with C1 let us say P1 which is the pole associated with C1 will be 1 over time constant is 1 over C1 R01 right? What is the pole associated with or let me write in this form let us say go1 by C1 right?

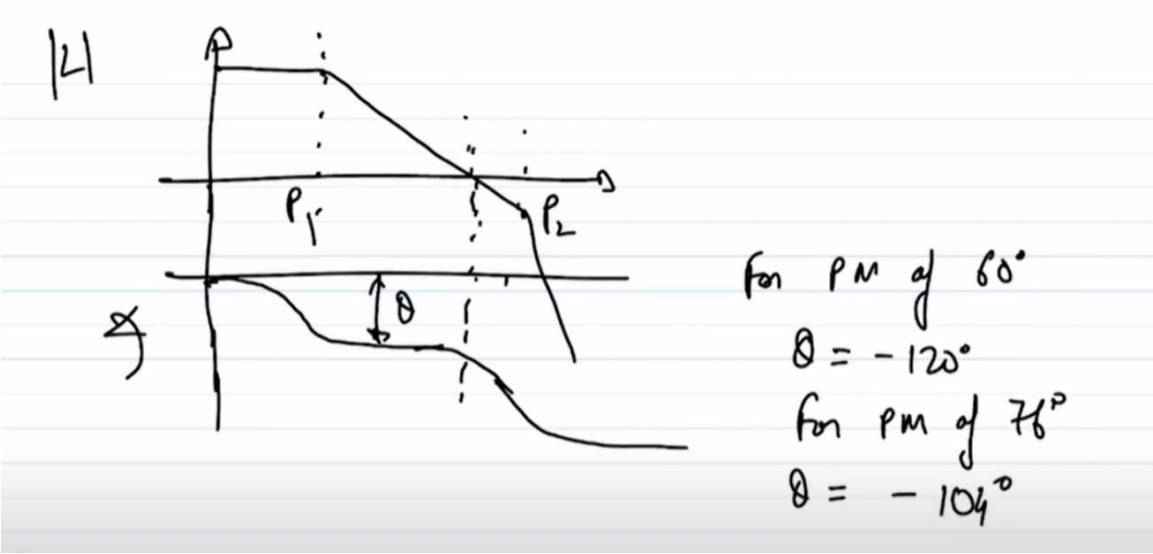
So let us write in conductance domain this is go2 right. What is the other pole? C2 will be go2 over C2 right. What is the DC gain? What is the DC gain of the loop? The DC gain of the loop is gm1 by go1 times gm5 right gm5 by go5 let me call this g05 gm5 by g05 and negative right because ultimately when Vtest goes up this goes up this goes down right so it is negative of this ok. So what is that what is our loop what is the L of S? L of S is DC gain Kdc by 1 plus S by P1 times 1 by plus S by P2 right? This is exactly similar to that of the common source amplifier that we had initially done the analysis for and note that we are still neglecting Cgd right because since we are neglecting Cgd this these two sections these two sections can be can be analyzed independently of each other because there is no coupling between the gate and the drain right.



So if this is the case if this is the case if this is L of S what do I need to ensure what do I need to do to ensure we have proper phase margin? So, if this is L of S now to ensure phase margin of the loop is greater than 45 degree we have to ensure P1 and P2 are far apart and omega u lies in between P1 and P2 right. If that is not that is not going to happen then we

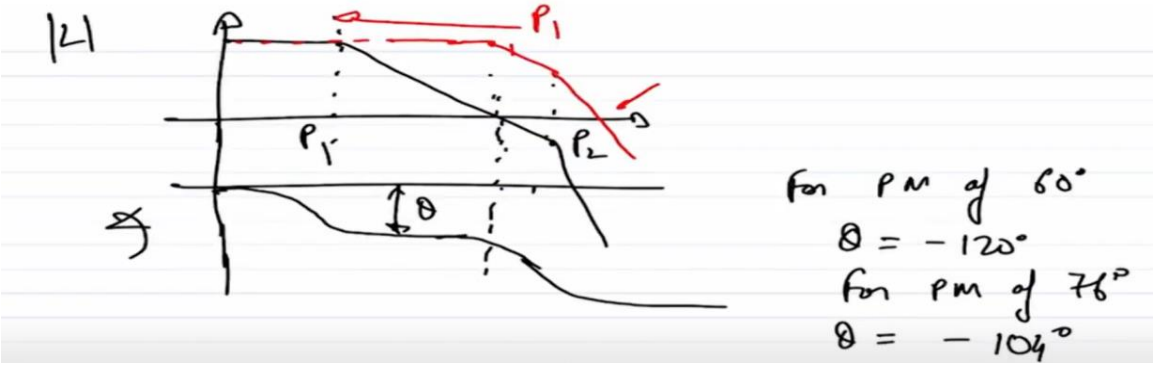
are in trouble right? So now you choose you can choose so choose your choose which one you want to make it which one you may either P1 or P2 you can choose which one you want to make it a low frequency pole and which one you want to make it a high-frequency pole right? So essentially choose which pole we want to be low frequency right? So if P1 is the low-frequency pole then omega u will be what omega u will be so at omega u at omega u ADC by S by P1 is 1 which means omega u will be ADC times P1 right and similarly then you choose the value and you have to ensure that P2 is greater than omega u and depending upon how much phase margin you want to ensure that P2 is further and further away from omega u right.

In other words, what we are saying is the mod of L will be something like this this will be P1 you have to ensure that P2 falls here after the UGB right so that the angle overall angle so the excess phase lag right this is the excess phase lag this theta this theta is this mod of theta is you do not want too much of lag phase lag right so you want this mod of theta to be let us say you want phase margin of 60 degree right so let us say for phase margin of let us say 60 degree this theta has to be minus 120 degree right for phase margin of let us say 76 degree this theta has to be how much minus 11 or minus 104 degree right and so on right so then you choose your P1 and P2.



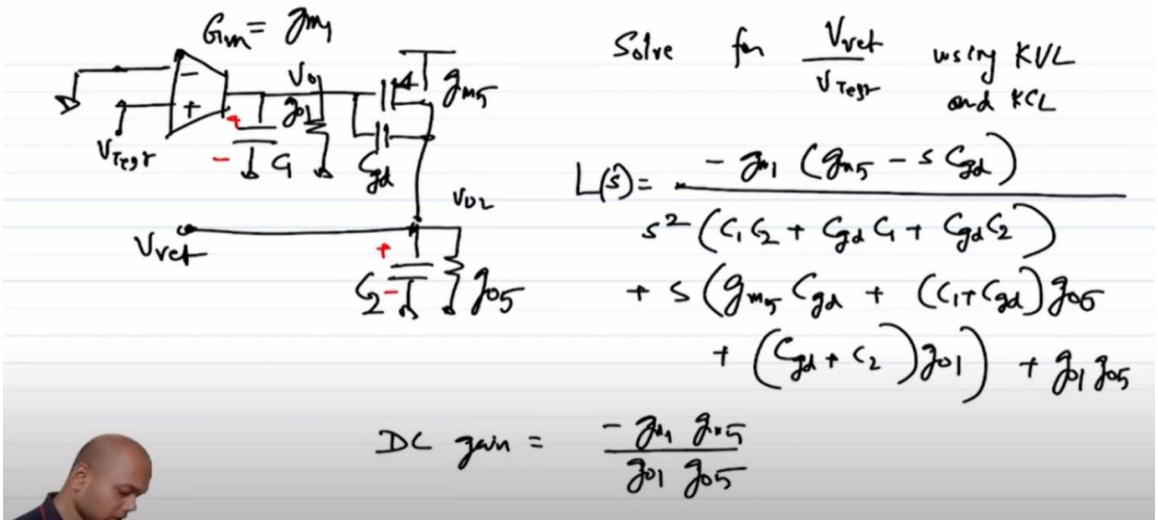
Now the question is let us say you put this circuit together and you found that P1 and P2 are not separated by that much right then what do you do then what you can do is you can if they are by default they are not separated you can choose any one of the you can choose any one of the capacitance and make it dominant right so you can basically in this case you can add more capacitance physically you can add more capacitance to the node to the node V01 right so in order to move P1 to a lower frequency now as you can as you can readily see right in or if you have to choose a capacitance let us say if let us say initially your P1 and P2 were somewhere here let us say initially your P1 was here and P2 was there then

your your loop gain would have look like the red plot right but we know that the phase margin of this red plot is quite bad right because ultimately the UGP of the loop is is at the location where we are getting a minus 40 degree per decade slope which means a phase margin will be quite bad right so in order to in order to get a better phase margin what are we sacrificing we are sacrificing the bandwidth right we are moving the pole P1 to a lower frequency right this this pole moves to a lower frequency P1 correct so we are getting better phase margin but at the cost of at the cost of bandwidth now as you can see you have the curve has a lower unity and frequency which means your amplifier is going to behave like an amplifier right till a lower frequency than than than before okay so that is one of the major bottlenecks of negative feedback right in order to in order to achieve stability we sacrifice speed okay okay



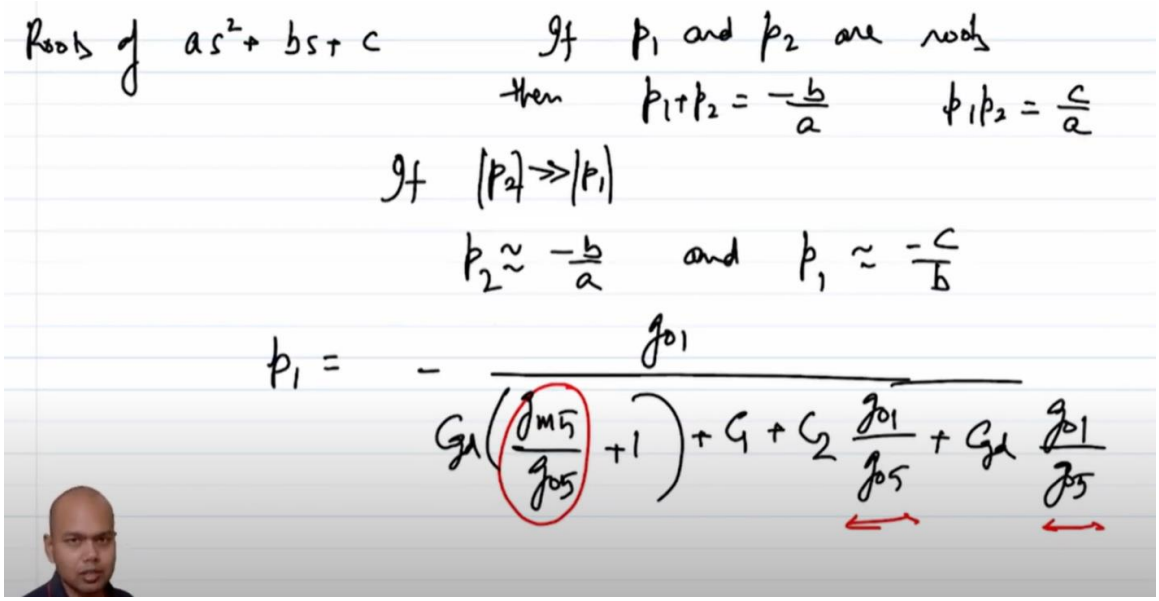
so now let us let us let us go ahead and and incorporate the Cgd capacitance that we have been avoiding till now and if this is a very interesting capacitance and it has a it has profound effects so so that's why let's we have kept the best for the for the last right so let's say so this is Cgd right and this is g02 g05 right we are doing calling it g05 so g01 this is g05 okay so let's see what is the effect right so ultimately in this case now what you can readily see that is V01 and V02 are coupled right in this case we cannot write a transfer function we cannot associate a conductance with the capacitance just by looking at the circuit because V01 and V02 are coupled through to a capacitor right so when we cannot really cannot really associate a time constant associated the time constant with the capacitance because it's a it's a large circuit right because it multiple capacitors are talking to each other so what is the next best solution the next best solution is to we have brute force and find out the entire loop gain right so essentially solve for V return over V test using KVL and KCL right so if you do that you are going to get this right so you will we are going to get L of S to be equal to so I have done this beforehand so so the derivation is not particularly important but the important thing will be the interpretation of the result right so let me write out the result first and we will go ahead and interpret the L of S will be minus gm1 times gm5 minus sCgd right divided by s squared C1 C2 plus Cgd C1 plus Cgd C2 plus s times gm5 times Cgd plus C1 plus Cgd times g not 5 plus Cgd plus C2 times g not 1 plus gds1 gds5 or rather g not 1 g not 5 right seems like a very complicated expression which indeed is it's a big expression second order term and lot of terms here yeah so the next thing will be to to make sense of these of these terms right so so first thing

first thing there's to the easier part what is the DC gain so what is the DC gain, DC gain is you set all the s terms to 0 right if you put s to 0 whatever you get is a DC n which will be minus gm1 gm5 by g01 g05 that is that is good that checks out how many poles will this have this is a second order system right how many poles are you going to have we are going to have two poles right and why does it make sense it makes sense because looking at the circuit I can set two independent initial condition between C1 and C2 right so essentially if I set if I set the voltage and C1 and if I set the voltage and C2 the voltage across Cgd gets set right so I can set two independent initial conditions which means that which means the order of the system is right even though we have three capacitors okay so that that's good.

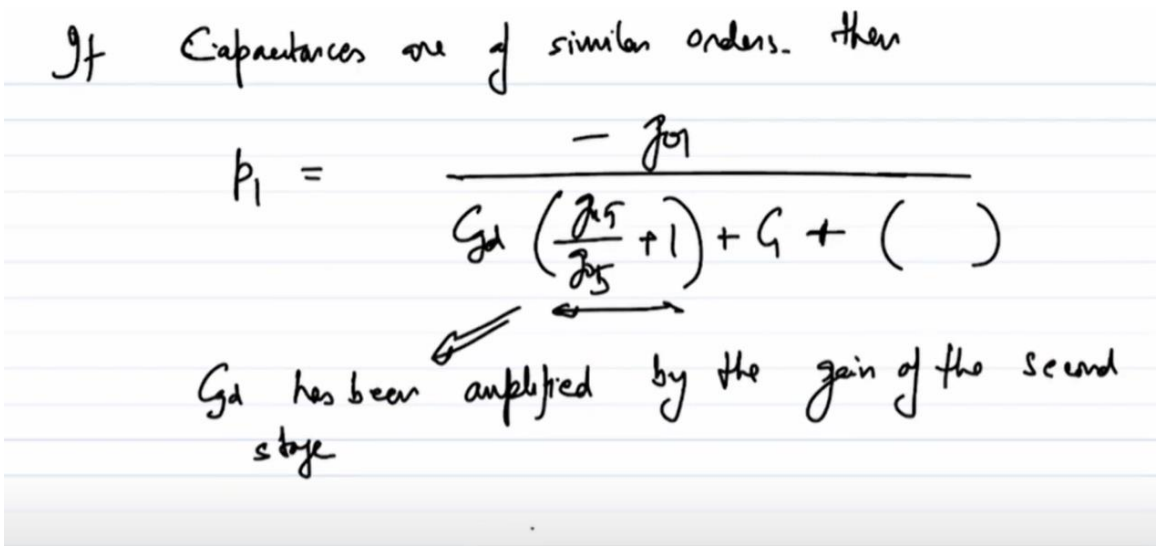


so what so what about the poles how should I go about finding out the poles so so this seems to be an I mean the denominator of the transfer function is of this form s square plus bs plus C right so we holds as the roots of the denominator right so it's the roots of the denominator means I have to find out the roots of roots of a square plus bs plus C right so I can always do that quadratic formula of minus b plus minus b square minus 4ac over 2a but as you can see that algebra will soon become too messy right so we should not we don't intend to go in that route so the route that we want to take is as follows that we ultimately want to design ultimately want to get a circuit that is that is a stable transfer function right a stable loop gain right so which means that we want or rather we want we are in search of the circuit which has a stable closed loop response the good tail margin which means that inherently we want a circuit in which the poles are separated right which means the roots of the equations are separated so that so as it turns out there are ways of simplifying a quadratic solution if the roots of the if the roots of the polynomial is separated right and what and what we are we know that we know that in case of a quadratic equation so if the roots are if P1 and P2 are roots then P1 plus P2 is minus b over a right and P1 times P2 is what its C over a right this is the property of a quadratic that we already know moreover now if P1 or let's say P2 is a high frequency pole and if P2 is much much greater than P1

like mod of P2 mod of P1 then then P1 is approximately minus b by a and P2 is approximately equal to minus e by right so then we see that there is some hope of of simplifying our expression right in this case what is a so this is a what is C this is C and the middle term is e correct so let's let's put those terms back so so what is P1 in our case then the P1 will be minus b over a that is sorry sorry I made a mistake here right if P2 is much more than P1 then P2 is over equal to minus b over a and P1 is minus c over b right so what will be P1 P1 will be minus c over b right so so gnot1 gnot5 divided by that entire term right so if I do that and can we do a further one level simplification we are going to get this we are going to get g not 1 divided by C times gm5 by gnot5 plus 1 plus C1 plus C2 g01 by g05 plus this is Cgd, not C plus Cgd not 1 by right so this is gnot5 right , so essentially we are doing we are simply doing this minus u over b but in C I have gnot1 times gnot5 so I am dividing by gnot5 the numerator and denominator and and this is what we are we are going to get right so now let's see whether this guy makes sense firstly before going into figuring out whether this guy makes sense or not so we what we like to figure out is there a dominant term in the denominator right if there is a dominant term then our life will be easier I can neglect the other terms and try to make sense of it right so what do you think do you have a dominant term so we so moment if we have a GM somewhere then you have to take notice right we have a GM here we have a GM5 by gnot5 what is this what is what does this remind you of so clearly GM5 by gnot5 is the intrinsic gain of the second stage correct is the intrinsic gain of the second stage, second stage is a common source amplifier you can assume that it's a gain of that common source amplifier so clearly this is much greater than 1 right so clearly this is much greater than 1 and this is also greater than gnot1 by 5 and g not 1 by g not 5 right so so essentially it seems like we have a dominant term in the new denominator right since we and but I mean we can always assume that if CGT is much much smaller than everything then this is not dominant that's not the assumption what we are making we are essentially making that assumption that we are making is these are the capacitances are let's say of similar orders right

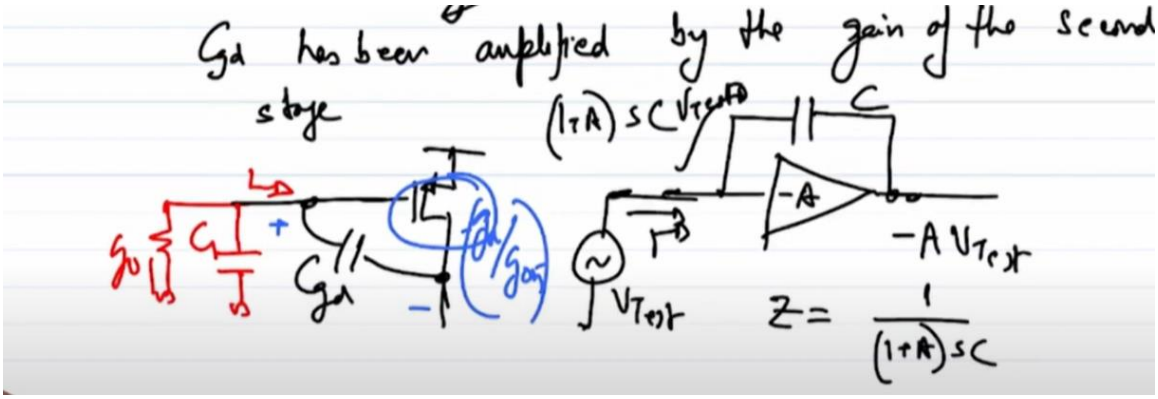


if the capacitances are of similar orders so if C's capacitances are of similar orders then P1 can be approximated as minus g not 1 over Cgd times GM5 by g not 5 plus 1 plus C1 plus bunch of terms which are which I can probably neglect right right so so let's keep those terms for now and I will try to try to motivate you will try to understand why the other terms make sense right so let's see why this these terms make sense so firstly what does this this term remind you of so this term seems to be it seems to be pointing to the fact that we have a Cgd capacitance the Cgd capacitance has been amplified right by the gain of the second stage right this seems like this seems like Cgd has been amplified by the gain of the second stage right okay so now so which means that let's investigate what is happening right so seems like seems like the second stage has a gain right



so let's say if I only concentrate on the second stage we had capacitance here it seems like if I this Cgd right seems like this capacitance here is getting amplified for some reason right okay so we need to investigate that what about g not 1 what about the what about that

numerator what do you why do you think we have a numerator of g not 1 and what does it signify what does it point to so when I am saying our cap our our poles our poles are of the what form poles are generally of the form of some conductance by some capacitance correct so if the conductance is g not 1 which pole that I mean which node am I pointing towards so clearly it looks like I am pointing towards Vnot 1 right looks like because I have a cap I have a conductance g not 1 connected to it so the capacitances around g not 1 would contribute to that pole in the absence of Cgd the capacitance attached to g not 1 was C1 but in the presence of Cgd it looks like in the presence of Cgd it looks like the capacitance associated with g not 1 is C1 and an amplified version of Cgd and bunch of other stuffs right so let's concentrate on why are we having this amplified version of Cgd right because what we are essentially saying saying that we have this C1 here we have g not 1 here right so it seems like the capacitance looking here is the amplified version of Cgd right okay fine so let's let's investigate that for a moment so to investigate that I have to introduce another concept and the concept is that of Miller effect right so so so if we have let's say an voltage control voltage source an ideal amplifier of gain of minus A okay and I put a capacitor across it a value C right and I apply it as voltage we test what is the current that I will see if this is we test this guy will be minus A times we test so what will be the current to the capacitor the current to the capacitor will be 1 plus A times SC times we test right so so



what is the importance that I will see so the importance will be 1 by 1 plus A times SC which means that which means that which means that any contraption any capacity if I put a capacitor across a voltage control voltage source of gain of minus A then looking from the input side it seems like I am driving a capacitor of value 1 plus A times C correct so can you relate this with our with our condition we can relate this because what is the gain of of this guy this gain of this guy is minus gm by g not 5 and and the and the voltage across the Cbd is getting amplified by 1 plus gm 5 by g not 5 which means that it is seeming to our the g not to g not 1 it seems like it not only has a capacitance C1 attached to it but it also has an amplifier capacitance of Cgd times 1 plus the gain of the second stage attached to it and that is what we see here right but note that this is not a voltage control voltage source this is a voltage control current source since this is a voltage control current source we cannot expect this Miller capacitance to come as is and that is why we get some extra

term right but fortunately these extra terms are not dominant right these are the extra terms fortunately these extra terms are not dominant I mean if you now say that C2 is very high then obviously they will become dominant then we'll have to revisit but as long as C1 C2 Cgd they are of similar orders then we can clearly see that C2 is not dominant this extra terms are not dominant which means we can we can develop some rudimentary intuition as to what the pole locations right what the pole locations associated with P1 is okay okay fine so that makes sense what about P2 right what about P2 so let's look into let's look into the intuition behind P2 or the location of the P2.