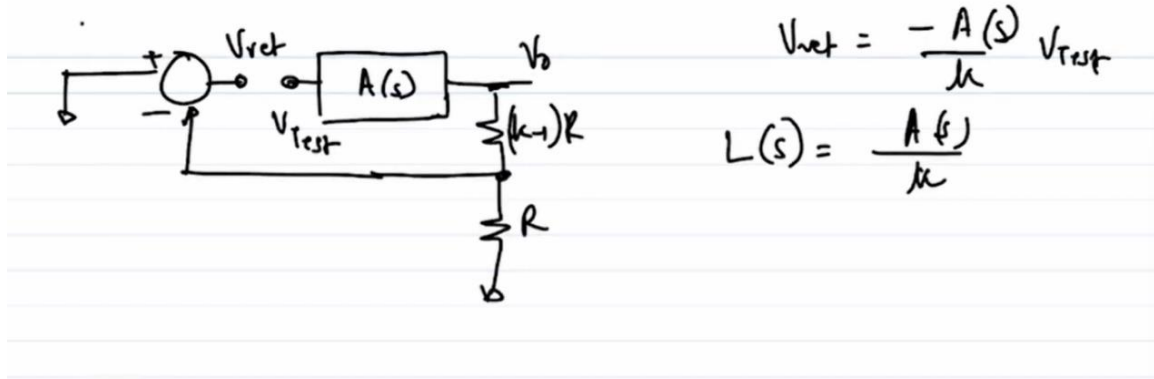


Course name- Analog VLSI Design (108104193)
Professor – Dr. Imon Mondal
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 12
Lecture- 37, module-02

So, let us try and understand what are the impacts of a poor first-phase margin is right. So, this will be a kind of bunch of facts that we can use as a thumb rule for our design. So what does phase margin equal to 0 mean? So let us say I have a system like this. Before we go into phase margin, can you tell me what is the loop gain? How will you evaluate loop gain? For to evaluate loop gain, I can simply desensitize the input, break the loop somewhere. So, let us say I break the loop here, apply a test voltage V_{test} and observe this voltage V return. So, what is V return? V return is equal to minus A of s by k times V_{test} .



So, loop gain L of s is A of s by k . Right. Okay, great. So, now let us go back to whatever we were planning to discuss.

So, let us say this is this. Okay. And we found out loop gain and we found out let us say phase margin. Somehow we have found out phase margin. So let us say we have this is case of phase margin and this is let us say V_0 and the test that we are doing is we assume that the input V_i is a step input with respect to time, like this is 0, this is some unit step right.

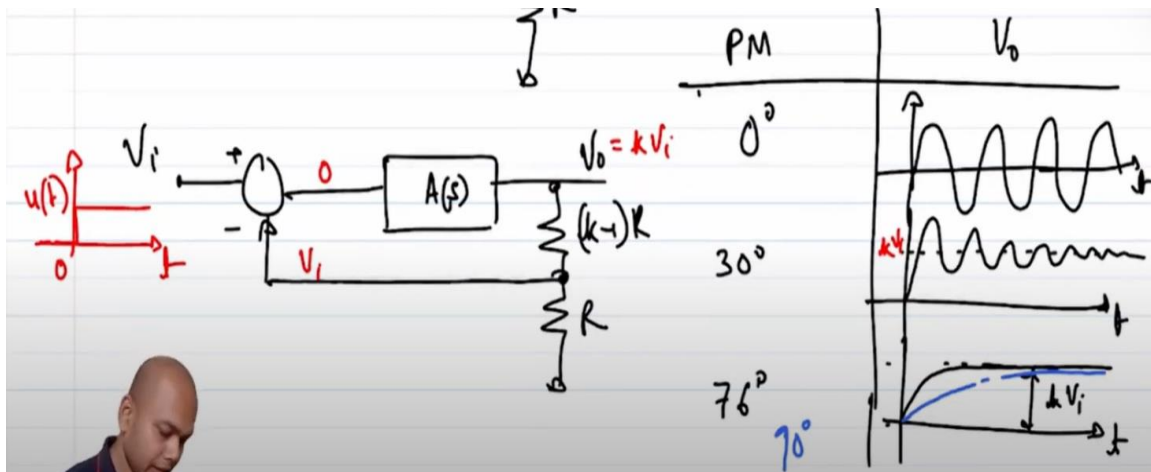
So, that is ut incrementally in the incremental domain this is the unit step. Okay. So, what do you think is going to happen if phase margin is 0 degree, what will V_0 look like? Note that if phase margin is 0 degree means what? Phase margin is 0 degree means at we are cutting that minus 1 0 point in the Nyquist plot or in other words we meet at unity gain frequency the phase is minus 180 degree or in other words the L of $j\omega$ is equal to minus 1 exactly 1 plus L of $j\omega$ is minus 1, 1 plus L of $j\omega$ u is exactly equal to 0 right. That is what phase margin of 0 degree means which means the system is an oscillator

right? So, ultimately your system will oscillate even though you have a step input right.

So, this is phase margin of 0 degree this is what it will seem like right? So, as it turns out if you increase phase margin right if we increase margin, so let us say we go to from 0 degree to 30 degree what is going to happen is. So, let us say this is 1 I have given an unit step. If I have given an unit step what is the expectation? What is the expectation under steady state? If the gain if the under steady state if the loop gain is really high if the loop gain is infinity under steady state what is the expectation? If the loop gain is infinity under steady state this error voltage will be 0. So, this voltage will be equal to V_i which means this voltage will be a step if this is V_i V_0 will be equal to $K V_i$ this is the expectation at steady state right?

So, that expectation at steady state is in the plot of the output voltages. So, I should see K times V_i right this is the expectation I should see this, but as you can see in the plot that I showed in case of a 0-degree phase margin and we have seen this with a couple of lectures back that if you have L of gm equal to minus 1 it does not matter what input you have given even in the absence of any input the output will oscillate right. So, let us say now we have a case in which phase margin is 30 degree right? So, in this case clearly, we are not encircling the minus 1 0 point right which means the system is stable, but however when you give an input as it turns a step input as it turns out the output does not settle output does not settle abruptly it goes something like this and eventually settles it rings and rings and rings and eventually settles. And if you keep on increasing phase margin and as it turns out if you go to a phase margin of 76 degree right if you go to a phase margin of 76 degree as it turns out in a second order system this is an important thing that I missed out in a second order system.

So, your output will not ring and it will settle like this to an eventual value of K times χ ok. And if you keep on increasing phase margin beyond that let us say now we go to 90 degree phase margin then the output will kind of settle definitely, but it will settle even slow slowly ok. So, this is essentially a lookup table kind of here you can you can consider these type of plots as a lookup table plots with respect to what type of output you can expect if you if you give an input of a step if you give a step input under different phase margin constraints right under different phase margin specifications ok. So, so clearly 0 degree is not good and 90 degree is very well I mean quite stable right, but sometimes it is neither possible to go to 90 degree or definitely 0 degree is not also 0 degree we definitely do not want. So, sometimes we settle in between sometimes we say that maybe 76 degree is good enough maybe 60 degree is good enough there will be slight amount of ringing, but the system will eventually settle.

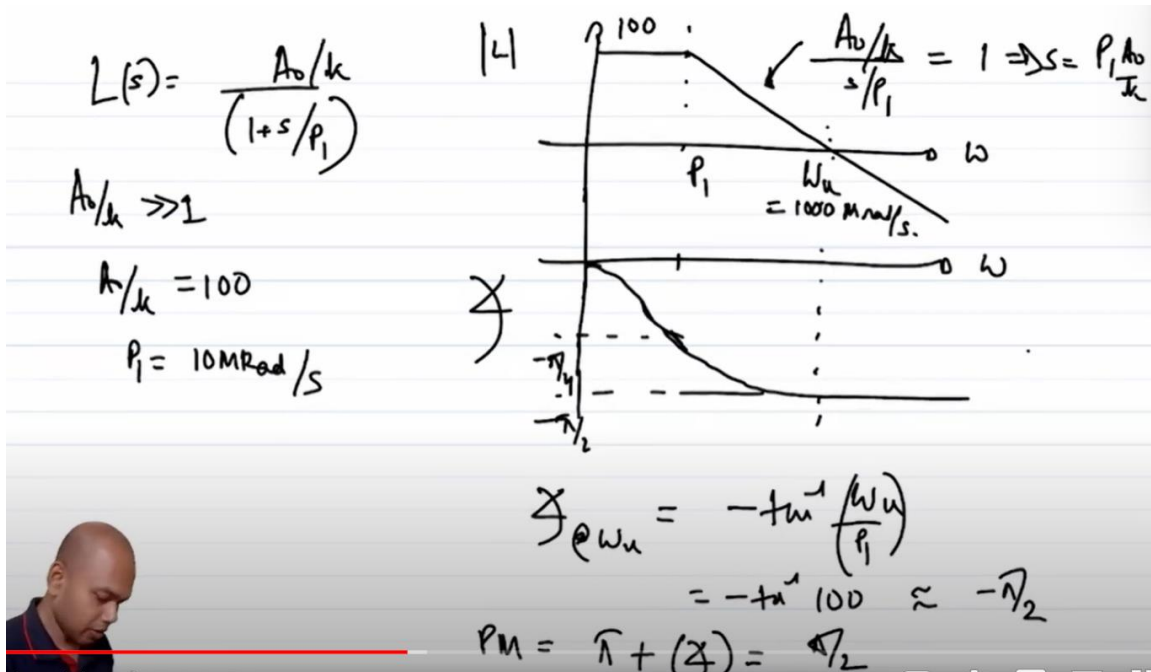


So, that depends on the specifications that we are looking at ok fine. So, now let us see let us take the example of a first order system let us say L of S is a_0 by k plus S by P_1 . So, again we do the bode plot. So, mod of L is single pole. So, it goes like this and obviously loop can be expect to be much high right quite high much greater than 1.

So, we obviously a_0 over k has to be much much greater than 1 this is this is an inherent assumption and what will be the what will be the phase plot the phase plot will it will start from 0 at P_1 it will go to minus 45 and then reach minus 90 eventually right. So, what is so let us take let us take an example let us say a_0 over k is equal to 100 right. So, this will be 100 and let us say P_1 equal to 10 megahertz 10 mega radian per second omega hertz mega radian per second right? So, let us say P_1 is 10 mega radian per second what do you think the omega UGB will be or omega U will be how do I find out same old same old what is the equation of this of this straight line this equation of the straight line is a_0 by k by S by P_1 correct and this if I set to 1. So, what do I get S to be S becomes P_1 times a_0 over k right?

So, in this case what does it mean P_1 is 10 mega radian per second a_0 by k is 100? So, this becomes omega U becomes 1000 mega radian per second ok. So, what is the what is the phase at the UGB? So, the angle at omega U is what minus tan inverse omega U by P_1 which is minus tan inverse 100 right. Now tan inverse 100 is as close to minus pi as close to pi by 2.

So, this is almost equal to minus pi by 2. So, what is our phase margin? Our phase margin is what pi by 2 right because we are pi by 2 away additional phase away from getting to minus pi of total phase right. So, essentially phase margin is pi minus pi plus angle which is minus pi by 2 or which is pi by 2 right. So, our system is stable. If I took at this look at take a look at this lookup table.



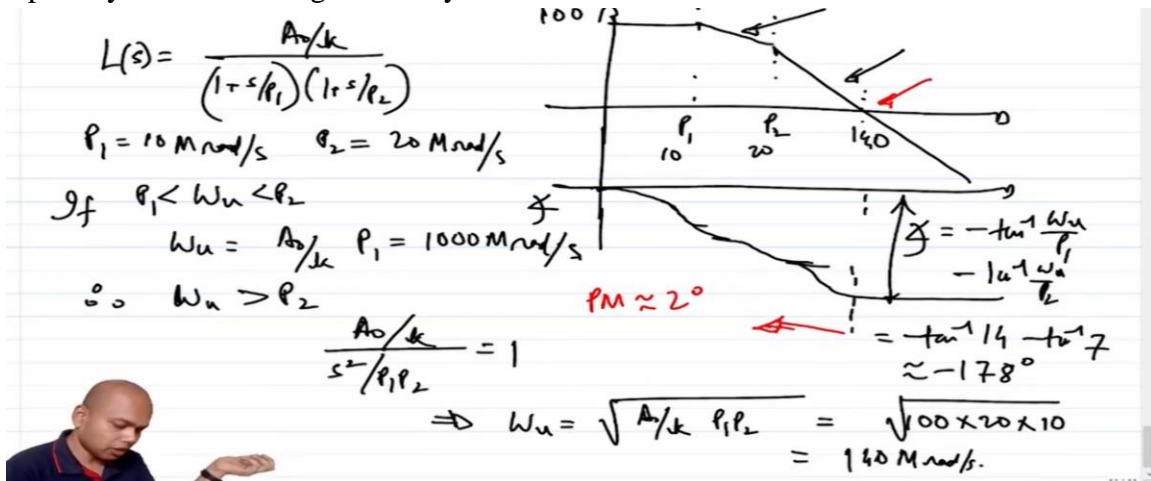
So, this corresponds to this this plot right? So, the system will conditionally stable first order system not a problem. So, now let us go to the second order system. Let us say L of S is a_0 over k $1 + S$ by P_1 $1 + S$ by P_2 right. And let us take another example of same let us say a_0 over k is 100 and let us say same P_1 was at 10 megahertz and let us say P_2 is at 20 megahertz.

P_1 and P_2 are close by right. So, let us say P_1 is at 10 megahertz, P_2 is at 20 megahertz and it goes like this. So, let us figure out where is the UGB to start off right. So, step 1 is finding UGB. So, let us assume the UGB is here between P_1 and P_2 right?

If ω_u is between P_1 and P_2 then what is the position of ω_u ? ω_u will be a_0 by k times P_1 which is 1000 mega radian, this is mega radian position right. So, clearly this is not the solution does not match the assumption. So therefore, so this therefore, ω_u has to be greater than P_2 . So, if ω_u is greater than P_2 , what is the condition that I should apply? The condition will be it exists somewhere in this segment and that will be a_0 by k by S square by $P_1 P_2$ equal to 1, which means that if I put ω_u equal to S mod of S equal to ω_u . So, ω_u essentially becomes under root a_0 by k $P_1 P_2$ which is how much? 100 times 20 times 10 that is 100 to 2 that is 140 mega hertz right, 140 mega radian per second right.

So, this is 10, this is 20, this is 140 correct. So, if that is 140 what will be the phase plot? What will the phase plot look like? So, again it will start off from 0 almost and then it will hit minus P_1 , it will have some phase lag, it will hit minus P_2 , it will have some phase lag

and here it will also have some eventual phase ok. So, what will be this phase? What will be this phase? This angle will be minus tan inverse omega U by P1 minus tan inverse omega U by P2 which is minus tan inverse 14 right minus tan inverse 7 correct, which is how much? Which is almost close to I think this is almost equal to 178 degree right? I mean it might be 178, 177 but it is very close to minus 180, minus 180 which means what? Which means its phase margin is Pm is close to 2 degree ok fine. So, this is a poor system, this is a poor system it will ring like crazy.



So, phase margin of 2 degree is not good. So, if I have to fix this then what should I do? If I have to increase the phase margin let us say I want a phase I want to ensure that the phase margin is at least 45 degree right then what should I do? So, what is the problem? The problem seems to be, problem seems to be that by that time I am hitting the UGB right by around the frequency of omega UGB I have already have lot of phase lag right. So, I have to reduce the phase lag right. So, the solution is to improve phase margin reduce phase lag around UGB or around omega U. So, how do I reduce phase lag? So, what is the source of phase lag? Source of phase lag is a pole correct the I mean at least since we have not taken into Os into account that the source of phase lag is a pole which means that if I am closer to a pole I will have more phase lag correct.

So, I have to ensure that we are away from a pole. So, clearly I cannot be I mean so, I have 3 segments right. So, if I am away from both P1 and P2 I have a problem I cannot be here because I mean that is parallel to the x axis right. So, I have to be between P1 and P2 right. So, which essentially means that which implies we need to ensure 2 poles below UGB are not close to each other because if they are close to each other they will give us more phase lag.

If the poles are at higher frequency if the poles are here if the poles are somewhere if the poles are somewhere here above UGB their contribution will be minus tan inverse omega U by that pole, but that pole is at high frequency which means they are giving relatively

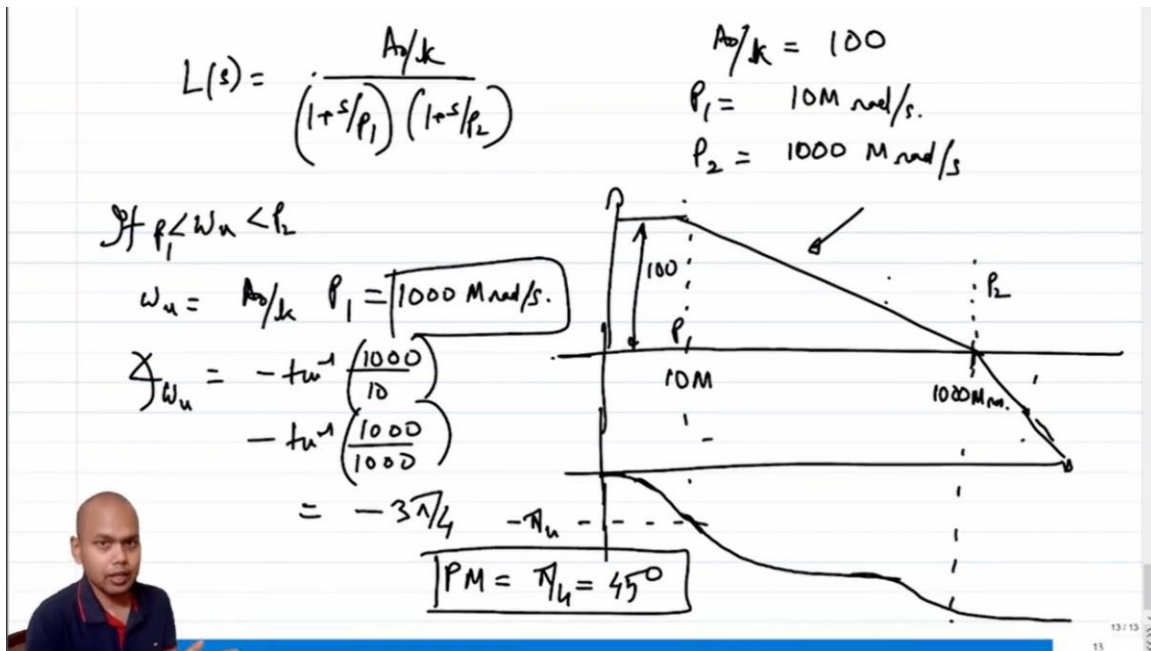
less phase lag right. So, low frequency pole gives high phase lag high frequency poles gives low phase lag right. So, the reason is so, reason is poles below UGB or poles near or below UGB below ω_U causes more phase lags than poles above ω_U which are essentially high frequency poles right fine. So, if that is the case which means let us say we are able to move let us say L of S is a_0 over k by $1 + S$ by P_1 $1 + S$ by P_2 and let us say now I mean a_0 over k again we do not want to compromise. So, gain is 100 P_1 let us say is a 10 megahertz and P_2 let us say is a 200 megahertz right?

So, what is the gain plot what did it look like? So, again P_1 something like this something like this ok. So, what will be what will be by ω_{UGB} how do I figure out? So, if the ω_{UGB} is here if this if ω_U is between P_1 and P_2 if ω_U is between P_1 and P_2 . So, ω_U will be a_0 over k times P_1 which is equal to how much? 100 times 10 that is 1000 right that is 1000 mega radian per second right. So, then also it is not possible right. So, even though I mean we are then also this assumption is not valid.

So, which implies ω_U is ahead after P_2 right. So, essentially the ω_U is still probably somewhere here. So, we will still have poor phase margin right. So, what is it what is the next thing that I should try? I should try and ensure P_2 is at even higher frequency let us say P_2 is at 2000 mega radian per second right. If P_2 is at 2000 mega radian per second or let us say let us assume P_2 is at 1000 mega radian per second right that seems to be the break point right?

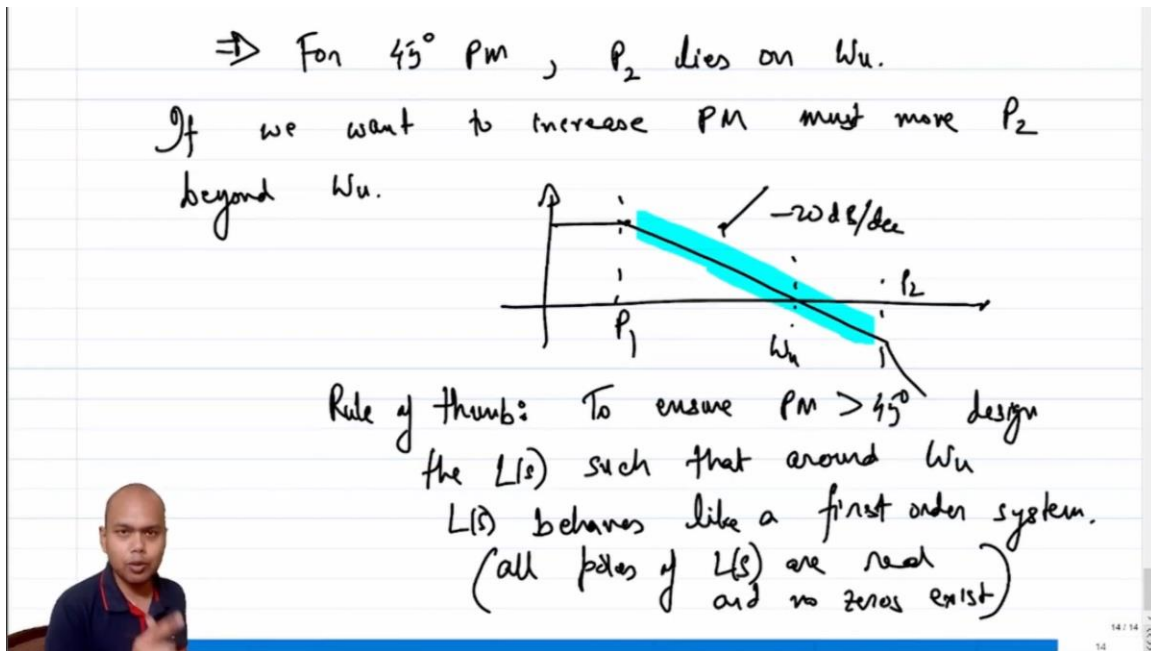
If P_2 is at 1000 mega radian per second what is ω_U ? ω_U by our calculations is so, ω_U by our calculations was this 1000 mega radian per second which means ω_U lies on top of P_2 right which means ω_U lies on top of P_2 . This is actually a quite interesting case right. So, this is 10 mega and this is 1000 mega and this is 100 ok. So, what will be the phase? What will be the phase here? If P_2 lies on top of UGB the phase as far as the bode approximation is concerned this will be 0 then I will reach minus π by 4 then this will go and then will go something like this. So, phase angle at ω_U will be minus $\tan^{-1} 1000$ by 10 minus $\tan^{-1} 1000$ by 1000.

So, this the first guy the first term is minus $\tan^{-1} 100$ which is for all practical purposes minus π by 2 and the second guy is minus $\tan^{-1} 1$ which is minus π by 4 right. So, this is minus 3π by 4. So, what is phase margin? Phase margin is 45 degree π by 4 or 45 degree right. So, if your phase margin is in 45 is 45 degree and if it is a two pole system then what does it tell you? It tells you that the second pole of L of S right the second pole of the loop gain not the closed loop gain, the second pole of the open loop gain, second pole of the loop gain lies on UGB right.



And if I have to increase the phase margin this so, this in plain English means that this implies for 45 degree phase margin P_2 lies on ω_u and if I have to increase phase margin, if we want to increase phase margin where should P_2 go? Should it go before ω_u or after ω_u ? Clearly P_2 should move above ω_u because P_2 is giving us that excess phase lag.

Note that the phase lag due to P_1 since P_1 is sufficiently away from ω_u the phase lag due to P_1 is almost saturated at 90 degree minus 90 degree right. The phase lag due to P_1 is saturated at minus 90 degree P_2 is giving me some hard one right. So, P_2 is in this case a P_2 is giving me 45 degree and that is why I am I also have a 45 degree phase margin right. If P_2 gives me less than 45 degree phase lag then I will have higher phase margin correct. So, which essentially means that if we want to increase phase margin we need to we must move the second pole move P_2 beyond ω_u right.



So, that is why one very often you will see a circuit designer say that if for a stable for a well behaved stable system particularly if it is a second order system we since we expect the second pole to lie above UGB right. So heuristically we try to ensure that when we plot the loop gain we try to ensure that the slope of the loop gain around ω_u is similar to the slope of a first order system right. So, if we only look at this slope if we look only at this straight line it seems like this is a first order roll off right this is a 20 dB per decade roll off this is a minus 20 dB per decade roll off right. So, the rule of thumb is to ensure phase margin of greater than 45 degree ensure design such that design the loop design L of S such that around ω_u , L of S behaves like a first order system.

Now note that this is not sacrosanct right. So, there are many assumptions that have gone in gone into this. So, one of the primary assumptions that we that I purposefully I mean intentionally took without really without really making it explicit is we assume that all the poles of L of S are real right that did not necessarily be the case all the time, but more for more most practical systems they are. So, this is the underlying assumption is all poles of L of S are real and no zeros exist right. So, these are some of the underlying assumptions, but as it turns out these type of assumptions are more or less applicable in most circuits that we deal with right ok. So, let us stop here in the next lecture which will be our which will be our last lecture for this course we will see we will take the structure of two stage amplifier right which is similar to that of an Op-Amp and we will see we will see the implications of stability when we put that two stage amplifier in negatively ok. Thank you.