Course name- Analog VLSI Design (108104193)
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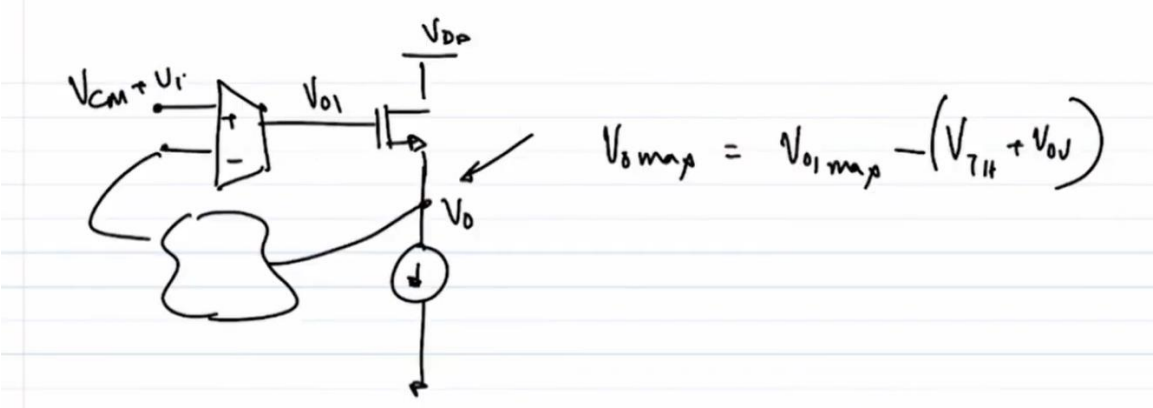
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 11
Lecture- 34, module-02

Ok, so as it turns out there is one more variant of the amplifier that we just did and let me lead with the reason of for exploring a different variant then we can delve into it in more detail. Ok, so let's say I don't connect this and I mean there will be some feedback stuff connected here so that is regardless. So we were doing unity gain feedback but it not necessarily be the case your H can be 1 by 2, closed loop can be 2 or 4 or 5 what there can be a whole bunch of stuffs associated here. The part that I am trying to motivate here is what is the maximum voltage what is the maximum quiescent voltage that V0 can go. What is V0 max? V0 max will be equal to V01 max minus 1 threshold voltage plus V overdrive. Right? What is V01 max? In this case what is V01 max? It is VDD minus 1 overdrive voltage.



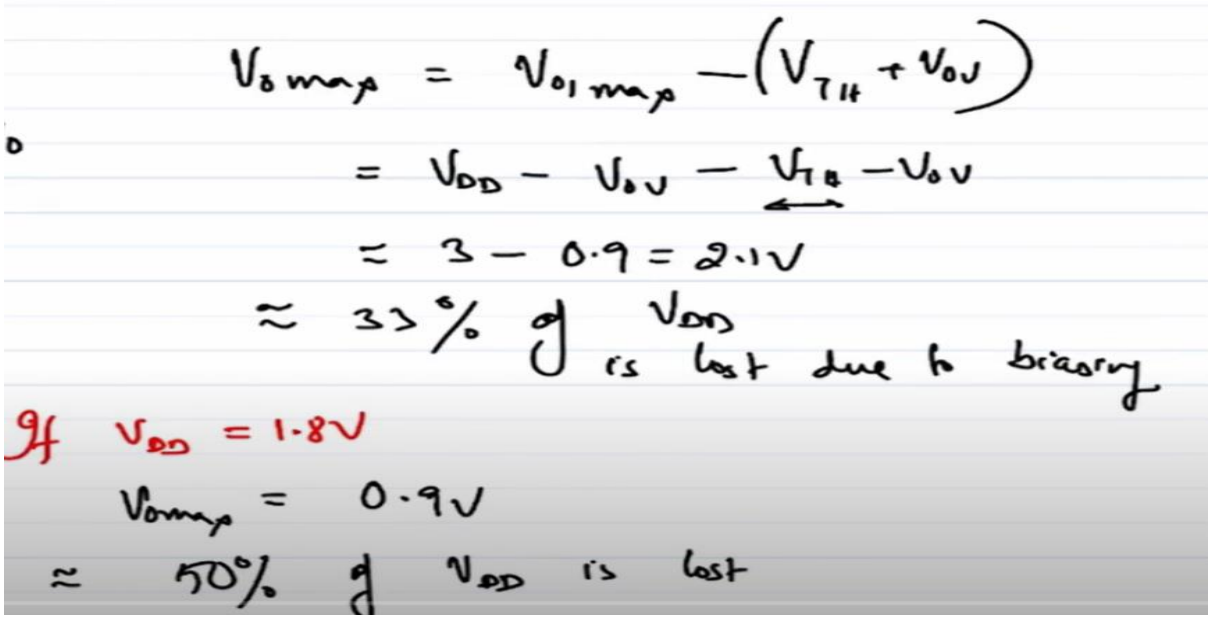
I am assuming all the overdrives and the threshold voltages are identical. They not necessarily be the case but at least they will be in the ballpark range. Right? So V01 max becomes VDD minus 1 overdrive. This becomes minus threshold voltage minus V overdrive.

So this is approximately 3 minus this is let's say 0.5 and 2 overdrive is like 400 so 3 minus 0.9 that is 2.1 volt. Did I make a mistake? Yeah yeah right 2.

1 volt. Ok. Ok. So what is the maximum this voltage can go to then this voltage can go to 2.1 volt.

Ok. But now let's say I am operating with lower supply voltage because many many many technologies have a lower supply voltage. So let's say if VDD is if VDD is let's say 1.8 volt. Right? So then ok and then what is V01 max? V01 max will be 0.

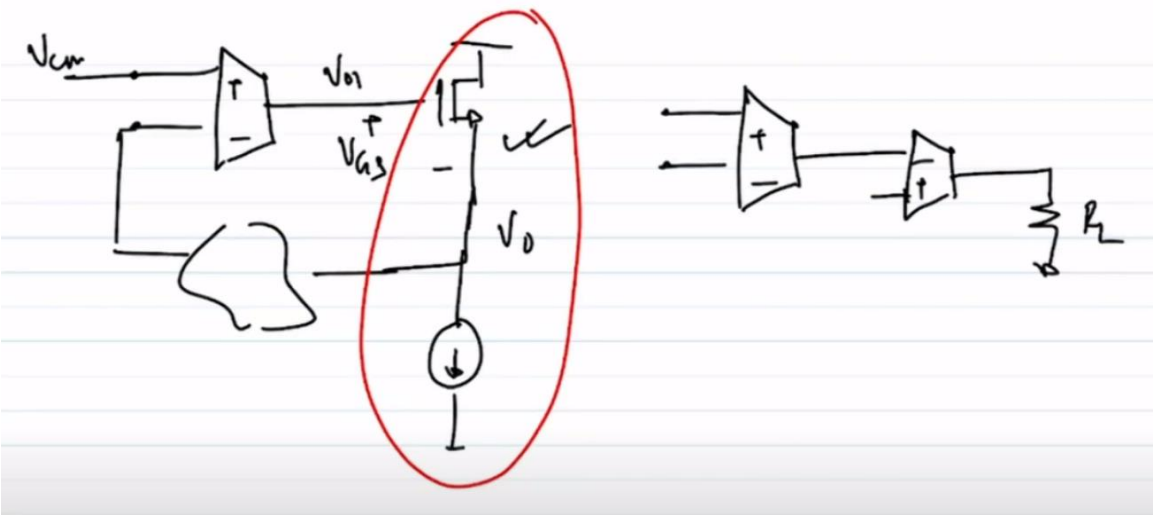
9 volt. Right? Ok. So what percentage of the signals possible signal swing is lost in the first case? So what I am essentially saying is that this voltage 0.9 by 3 volt this ratio right or approximately 1 by 3 or rather I can simply say that approximately 30% of max possible swing is lost or 33% right? 33% of the max possible swing is lost due to biasing. So in this in the second case how much? 50% of the or rather not max possible swing if 33% of VDD is lost due to biasing and 50% of VDD is lost. And since your power is directly proportional to VDD you can see that in the first case, 33% of the power is lost just to keep this guy in saturation properly.Right?



In the second case, 50% is lost and you can see that this problem is becomes increasingly more acute as the threshold voltage drops down. Right? So that led to I mean that coupled with another consideration has led to exploration of different architectures. Right? So one possible scenario is this. One possible scenario is so we have to put something here and let's so there we have a feedback right? So here we have to put a transistor here if we put a NMOS transistor and and bias it as we did right the problem was the problem the major problem was this this voltage was capped and on top of that, I am getting a VGS here. Right? The major problem is on the major problem is we are getting a VGS drop between VO1 and VO.

Correct? So that that is essentially a big problem. But what if what if I don't use a PMOS? What if I use an NMOS? Now you might say that we saw that using a PMOS sorry I mean what I meant what if I don't use a NMOS I use a PMOS but you might say that we saw like in the module one that using a PMOS is a problem because the common common drain buffer is a is a problem right? But what if we say that we will not use a common drain buffer we'll use a second stage common source amplifier. What I am essentially saying is

what if we do this block diagrammatically let's say we have one amplifier and we cascade it with another amplifier or rather let's say we cascade it with another amplifier and then drive an RL then what happens? Then you see that naturally it seems like I can get even more gain because in in this structure in the structure that we have discussed till now the current buffer right sorry the voltage buffer the second stage is not giving you any gain in fact this gain is slightly less than one if at all right the maximum gain that you can get between the gate and the source of a voltage buffer is one theoretically in practice you get less than one but if the second stage is also a gain stage right if the second stage is also a gain stage then I can get some gain out of the second stage also I mean that seems to be even better situation isn't it?

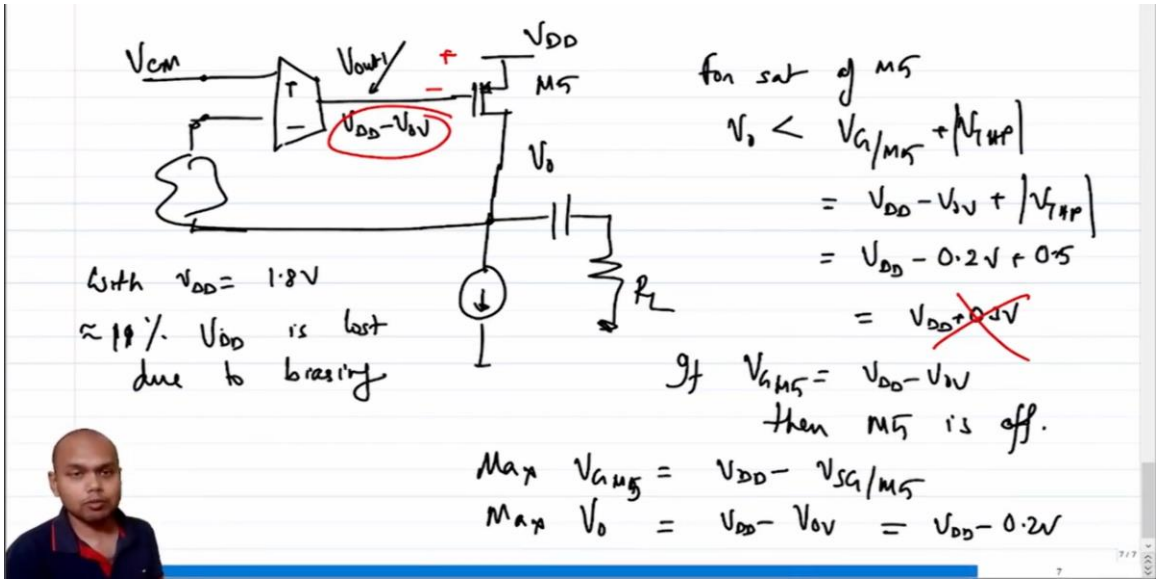


So we get more gain but what about the headroom? So let's consider that so in order to make this a common source amplifier what should we do? We have to ensure that the source is rounded for the second stage the source become rounded right in this case the drain is rounded but in the second stage source has to be rounded now if we we simply have to ground the source we cannot use NMOS we can use a PMOS so let's use a PMOS an incremental rounding is equivalent to saying it connects to VDD right so in principle the second stage is a common source PMOS amplifier right and we put in negative feedback and all those things and now let's consider now let's consider the loop gain and everything okay so before we consider loop gain let's consider what is so if let's say this is connected like this or through some negative feedback stuff what is the maximum voltage V0 can go to? So what is the maximum voltage V01 can go to? V01 can go to again VDD minus 1V overdrive what is the maximum voltage V0 can go to? Note that this is a drain so drain of a PMOS transistor can go higher than 1 over 1 threshold voltage above the NMOS above the gate right in principle right but I mean in principle what in this case how if I if I consider the case or if I only look at the gate and the and the drain if we only so for saturation of M5 all we need to ensure is that V0 is less than Vg of M5 plus threshold voltage right which is VDD minus V overdrive plus threshold voltage right so in the cases

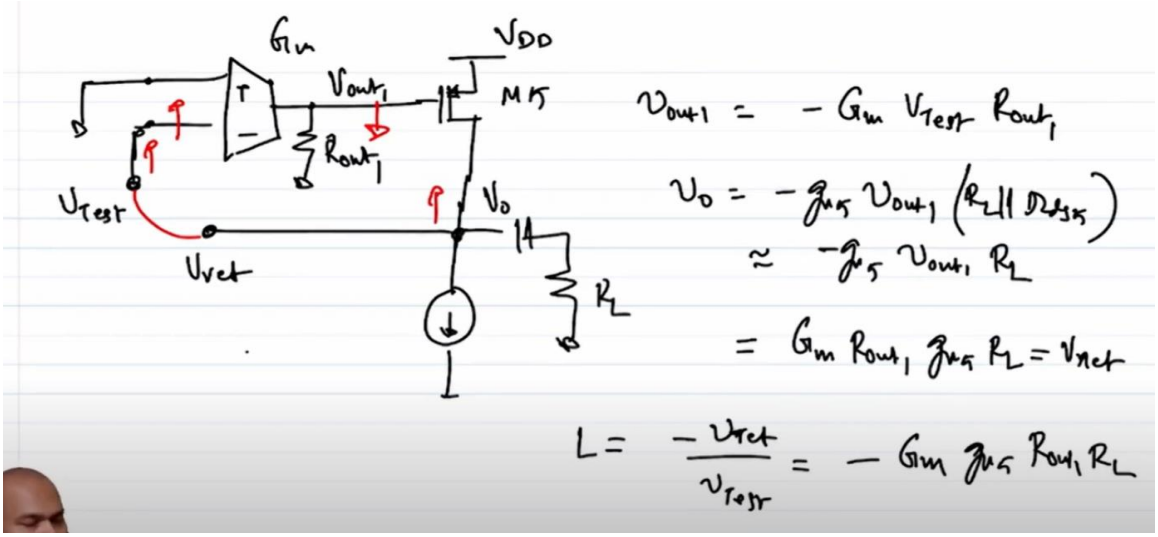
that we took it becomes VDD minus 0.2 volt plus 0.5 volt so this is like VDD plus 0.

3 volt this is the saturation condition for M5 but you can as rarely see that V0 cannot go above VDD right because if V0 goes above VDD the Poisson current direction has to change that is not possible so what is the maximum that V0 can go to? So this is not possible this is this is this is this is this is impractical so what is not possible as a what is the other what is the maximum that V0 can go to? then V0 basically can go to so so so that the issue the issue that you will have is if we did if this guy if this guy goes to VDD minus V overdrive in a comment on the on the condition of M5 is M5 on or off right so what is the VLC of M5 the VLC of M5 is V overdrive only but it has it has to be threshold voltage plus V overdrive right so if this is the condition so if this is the condition if Vg M5 is equal to VDD minus V overdrive then M5 is off so max what is the max Vg of M5? max Vg of M5 is VDD minus 1 Vst of M5 now this is possible this is not a problem because this falls within the range of of the allowable voltage swing at Vout1 so what is so what is the max V VO so max V O is this plus threshold voltage threshold voltage which means VDD minus 1 V overdrive right so this is approximately VDD minus 0.2 volt so in in essence in this case in this case V0 can go very close to VDD right percentage wise right if with VDD is equal to 1.8 volt supply on the higher side only 0.2 volt is lost right so 0.

2 by 1.8 is almost like 11 percent right so 11 percent power approximately 11 percent power or VDD is lost due to biasing so this is far better than the 50 percent loss that we were getting in the previous architecture right and that is why you will see that as the voltage supplies have lowered and lowered people have gone away from using a common drain output stage right and have stuck to using the common source output stages okay now the stuff that I didn't talk about till now is what is the gain of the common source output stage.

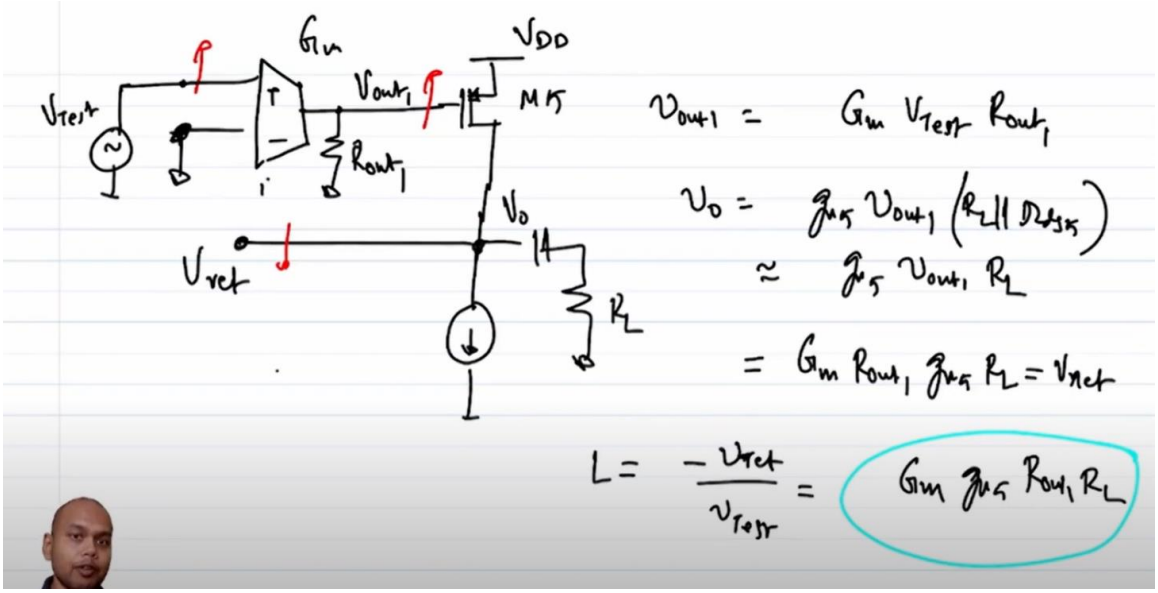


so let's let's investigate that also so loop gain let's do loop gain right you so to do to gain what we do we incrementally ground the input break the loop like this this loop will be closed so I am breaking it here and I apply it as voltage here and you observe the return voltage here and we know that there is an output resistance R out here right okay so what is the loop gain L or rather let's find out what is V return so what is V out 1 V out 1 is minus GM times V test times R out right or does this R out 1 right and here we have this right okay so what is the O what is V O V O will be okay we will soon see you will soon see a problem so let me go ahead with this then we will soon see a problem so V O is what V O is now note that we are this is a common source state so there is another inversion so V O is minus GM 5 times V out 1 right so that should be small right so this is V out 1 this is V O GM times V out 1 times RL parallel RDS by right so this is almost equal to if RL is by definition RL is a very heavy load right so RDS has to be negligible this becomes G minus GM 5 P out 1 RL which is equal to GM times R out 1 times GM 5 times RL so what is L L is minus V return over so this is by the way we return right minus V return over V test which is minus GM times GM 5 times R out 1 and sorry so what does this minus sign tell you what does this imply this minus sign in in the loop can essentially implies that the loop is in positive feedback why is the loop in positive feedback why do you think the loop is in positive feedback so that's easy to see so let's say we we we excite we increase that voltage right if we increase that voltage what is going to happen to V out 1 what is going to happen to Vout 1 V out L1 is going to decrease what is going to happen to V0 V0 is going to increase this voltage increases so we whatever excitation we fed the same I mean a return excitation in the same direction is getting fed back which means this is a positive feedback loop right

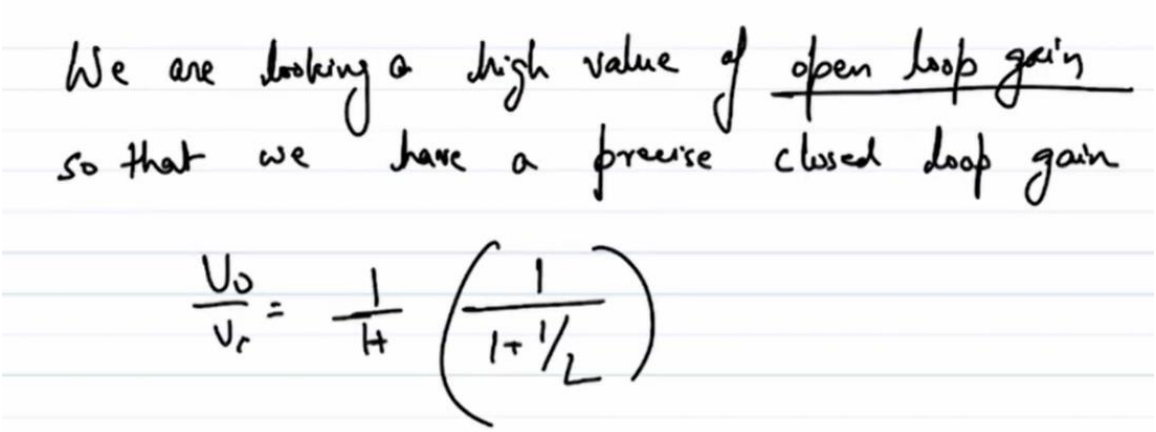


so what is the solution we cannot connect the feedback at the negative terminal we have to connect the feedback at the positive terminal correct so to connect the feedback at the positive terminal and here we'll have this VCM plus VI or whatever okay and then if we have to do a loop analysis we short this right we short this and we apply a this voltage here

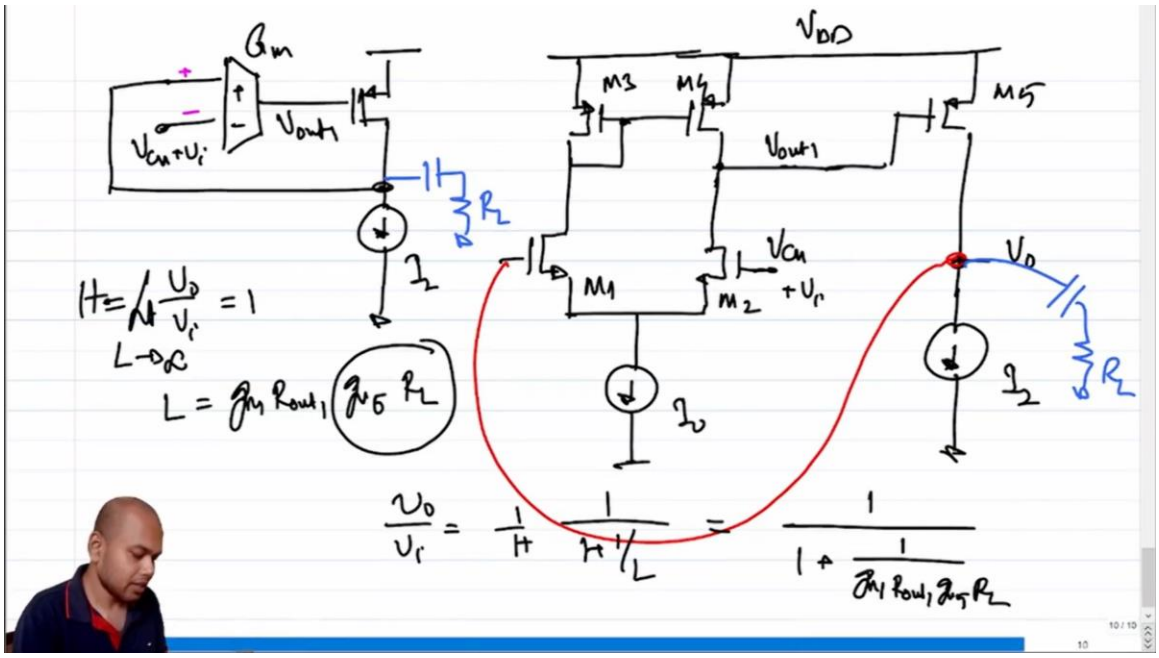
and we observe the return voltage so so again let's go around the loop let's see so if this increases what happens to V out 1 V out 1 increases if you have to on increases what happens to V out V out decreases and now when the loop is closed you can see that we have a negative we have a negative feedback negative voltage that is or rather a voltage in the negative direction that is coming back which means that all these signs will change this will become positive this will become positive this will become okay so the loop gain becomes this the loop gain becomes this now note that this loop gain is proportional to RL but as long as you are keeping gm5 times RL to be at least unity or higher then you have highly again now again very quick reminder we have to I have to emphasize the fact that we are not looking for a precise value of loop gain we are looking for a high enough value of loop gain why are you looking for a high enough value of loop gain we are looking for a high enough value of this loop gain or the open loop gain so that we have a precise value in the closed loop gain right so this is important so let me write this down we are looking for a high value of open loop gain so that we have a a precise closed loop gain or closed loop gain so we are not necessarily looking for a precise value of open loop gain we are looking for a high value of open loop gain so that we have a precise value of closed loop gain why do



we say so because note that V0 over Vi is 1 over h 1 by 1 plus 1 by L so as long as L is high enough I can neglect 1 over L with respect to with respect to 1 and V0 over Vi will become 1 over h we are looking for 1 over h and since we know that h is a ratio of some things that's I mean in the cases that we have seen h is the ratio of resistance we are we are good okay okay fine so now let's what what we will do is let's let's get rid of this all these symbolic GMs and put the transistors back right so let me sketch this once and

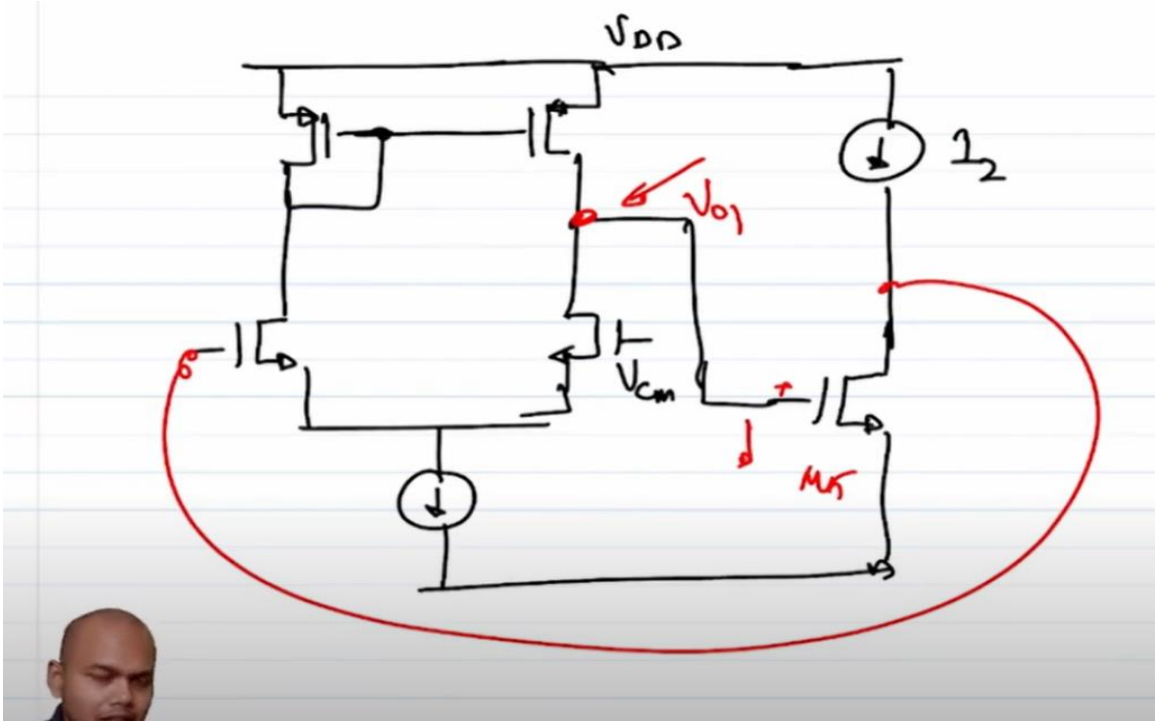


let's see how the transistor equivalent of this circuit looks like so what would be the transistor equivalent of this so this GM we know this is a single stage differential amplifier we have done it multiple times what is the second stage this is V out 1 V out 1 the second stage is a PMOS second stage right so this is I2 not okay so now where do you think should I connect the output should I connect the output here or should I connect the output here so let's let's let's connect the output here and let's see whether our negative feedback is intact or not so in the loop somewhere in the loop let's apply an excursion so let's say this voltage increases if this voltage increases what happens to V out 1 naturally you see that there is an inversion right this is like a common source amplifier if this voltage increases V out 1 decreases if V out 1 decreases what happens to be out the final output this voltage increases so naturally you see that this is a this is a positive feedback loop right so we cannot apply connect the feedback at this terminal which means we have to connect the feedback at the other terminal and we'll have to connect the input here right this will be VCM plus VI and this will be V out this is a unity gain configuration of our of our buffer right okay so if we didn't want unity gain configuration what would we have done we had to we have to again put a R by R or k minus 1 R and R ratio and take the feedback part and and and feed it back right so that's what we had to do I would we would have done but in this case the configuration is that of unity gain right so if the configuration is that of an unity gain what is what is H? H by definition is what? H by definition is V0 over VI limiting value when L tends to infinity right so if L tends to infinity that is a loop gain tends to infinity right what is going to happen with the loop gain tends to infinity clearly these two voltages will track each other and V out will be equal to VI right unity gain buffer so so H is 1 what is loop gain? Loop gain we know is in this case gm1 gm1 R out 1 gm5 times RL right so what is incremental V0 over VI? Incremental V0 over VI is 1 over H 1 by 1 plus 1 by L which is equal to H is 1 so all it becomes is 1 plus 1 over gm1 R out 1 gm5 R out right okay



so note that this is again one order of magnitude better than if we had connected RL directly to the output of gm right because a steady state error in this case is is lowered by a factor of the gain of the second stage right so because the loop gain is higher loop gain is higher by this factor right the loop gain is higher by a factor of gm5 times RL hence hence the steady state error the final error would also go down so the tracking of the output voltage with respect to the input regardless of variation of some value some variation of RL or even some variation of process voltage temperature will be much better much better in this case okay now before we end today's lecture a natural question that comes is the second stage could have been an n-MOS second stage as well right I could have used an n-MOS second stage as well isn't it so what I am essentially saying is I could have as well used an n-MOS common source amplifier in the second stage in that case his output would have had to come here and we probably would have had to connect the current source here right and this probably would have been the VCM and this guy goes and connects here and all those things we would have had to do but what's the issue now the issue is dependent upon what is the what is the expected output voltages what is the quiescent condition but in general as you see that this natural voltage of the output of the first stage is more towards VDD right and it's probably true that the natural voltage expected VGS of the of this m5 is more towards ground right so the range of acceptable voltages the overlap of the range of acceptable acceptable voltages might not be might not be sufficient to use a n-MOS second stage but having said that if the VDD really comes down if let's say VDD is like 1 volt there is quite possible that the range of the first stage range of acceptable quiescent voltages of V0 V01 and the range of acceptable quiescent voltages for m5 VGS might be might be okay so in that case m5 is an n-MOS m5 is also probably fine again as I said it depends upon what is the situation on the ground what you are trying to design for it's not necessary

that just because I said that if you use a n-MOS first stage you have to use a pMOS second stage or the pMOS common source amplifier need not necessarily be the case all the time right okay



so as you can see that if you remember at the beginning of the course I had promised you the final architecture as you can you if you look back at this architecture you this seems like it is almost similar to whatever we promised right we are getting closer and closer there in the next few lectures you will see more in-depth analysis of what this is whether this will work as is let me give you a brief primer there are issues with this architecture with regards to stability right so if we just connect this like that the way we have there can be some interesting phenomena that can happen we will discuss those things in the next few lectures right okay see you. Thank you.