Course name- Analog VLSI Design (108104193)
Professor – Dr. Imon Mondal
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 11
Lecture- 33, module-01

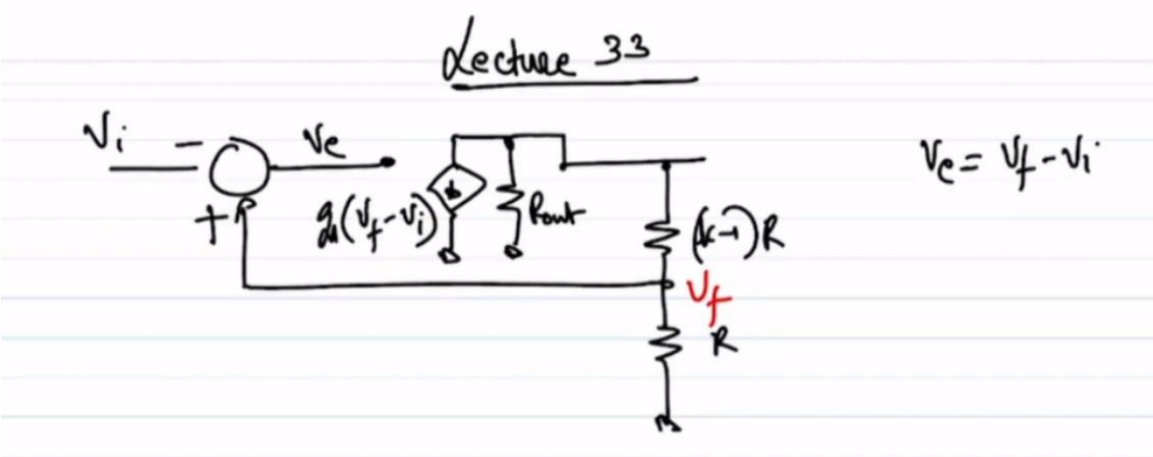
Now, welcome back this is lecture 33. So, we were discussing a differential amplifier and its various avatars right in the last few lectures. So, a very 1000 feet overview of what we were discussing till now was the following. So, we wanted to make a voltage-controlled voltage source of gain of more than 1 right and for that we said that we will use negative feedback, we will resort to negative feedback and we will compare the desired output with an actual output right and we came up with this architecture where this guy had to be again A which tended to infinity. If this was the case right, if this were the case then V0 will be equal to A times Vi and we also saw that this contraption is likely to have a very low output impedance right which means that this would have this would act like a voltage-controlled voltage source and then we said that ok. So, how do I realize this gain of A? So, only gain block that we knew was a common source amplifier and so, we replace this with a common source amplifier right, common source amplifier with some Rd right instead of Rd in we can call this an Rout right and this voltage control current source was supposed to be gm times Ve correct, where Ve is the error voltage and this is how we were supposed to connect it, but then we saw there was a problem with this connection.

What is the problem? The problem was that this becomes a positive feedback loop because there is an inversion in the common source amplifier right. So, here we can break the loop anywhere let us break the loop here and insert an insert increment if that voltage increases then this voltage decreases, if this voltage decreases, this voltage decreases. So, once it goes to the summer there is one more sign inversion which means this voltage increases which means this becomes a positive feedback loop. So, what we there then we say we said that given that we have to use a common source amplifier because that was the only gain block that we knew what was the other fix? The other fix was to invert the signs of the loop itself right.

So, we can say that this becomes the sign of the loop right. So, in this case we go around the loop the same way. So, this voltage let us say it increases because of some injection this voltage increases. So, this decreases, this decreases, so this decreases. As you can see if I inject any disturbance in the loop right externally then the loop has an action of reducing the disturbance right.

So, this is negative feedback. So, the signs of the the signs are all right ok. So, if the signs

are all right this is fine. So, now how do we and then we said that fine if this is ok how do we actually club this how do we arrange this summer and how do we make the entire arrangement then we said that this seems like gm times Ve is equal to what gm if this is Vf. So, gm times Ve is essentially gm times Ve is Vf minus Vi right, Vf minus Vi because Ve is equal to Vf minus Vi ok.



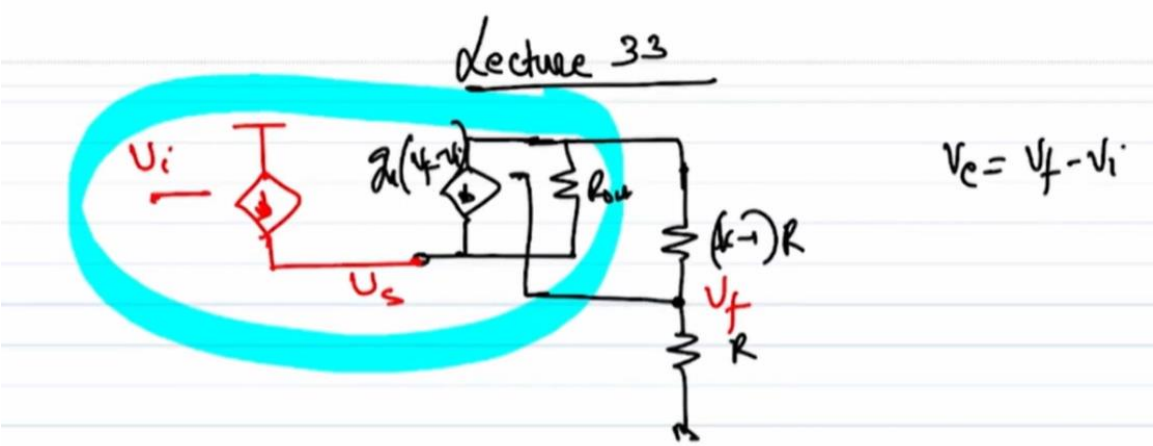
So, that was all good. Then we said that ok then how do I use this summer then we knew that a common source amplifier this voltage source like this control current source responds to the difference between the gate and the source voltages. So, we were trying to see if we can get rid of all these things and directly apply the feedback voltage here and if we can make this voltage equal to Vi then we are good right. But then we saw that if Vi has a resistance and which then this is a low impedance node the source the source terminal is a low impedance node if the source terminal is a low impedance node then the feedback voltage from here it has an infinite impedance, but they this impedance is 1 over gm right. So, which means this is not particularly a this can load the whatever is driving that that node.

So, then we said that this probably is not a very great idea. So, what we can do is maybe use a voltage buffer a voltage buffer and apply a apply a voltage Vi right. So, so then we rearrange this circuit in a in a slightly better way right. So, that it it made sense. So, what did we do to rearrange we we we said that so let us do this instead of so let us let us do this.

So, ultimately this is a voltage control voltage. So, voltage control current source. So, this is Vf right. So, this is Rout. So, this is gm times Vf minus Vi and this becomes Vi right.

So, how do I realize this buffer? This buffer we could realize using a common drain amplifier right. This buffer could have been realized using a common drain amplifier and a common drain amplifier was nothing, but this where we apply an input Vi right and this becomes a source node a common source node correct. This has to be connected ok. So,

then we this eventually became the small signal equivalent of of our of our differential amplifier and over the course of last few lectures we have been trying to figure out the properties of this thing right. We have been trying to figure out the properties of of the stuff inside the inside the skyblue box right.

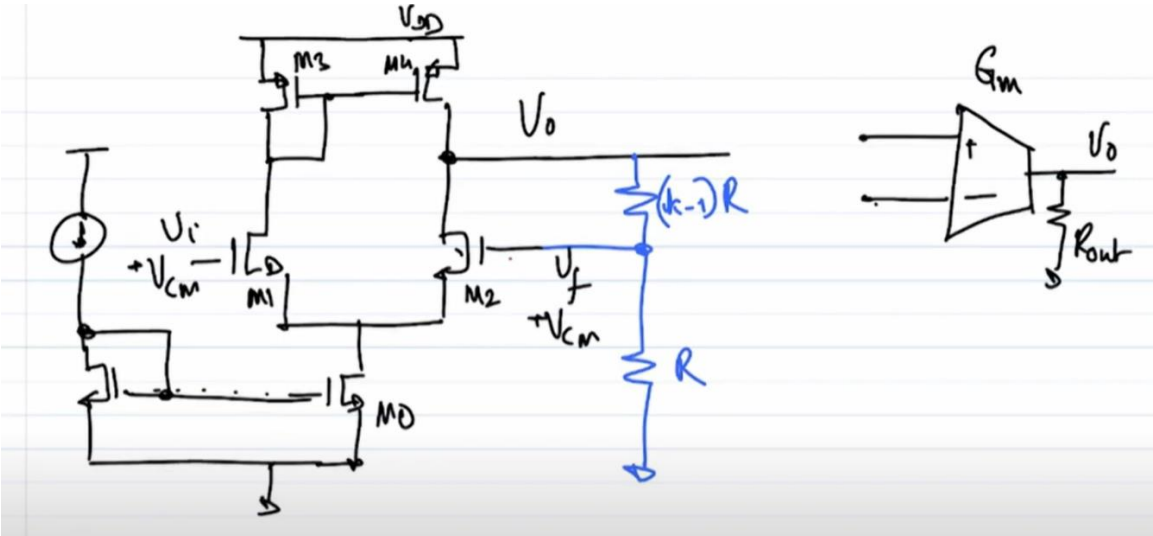


Since we are trying to figure out the properties of the sky blue blocks we did not consider the feedback network at all right. So, now if we if we go back and try to consider the feedback network what will it look like. So, essentially the stuff inside the skyblue box was a differential amplifier and we saw multiple versions of the differential amplifier. The last version that we saw was a differential amplifier with a current mirror Load and let us sketch that first. So, ok this was Vi and this is supposed to be Vf.

We have been calling this D1 and D2 right over the course of last few lectures, but if we have to equate this picture with this picture then it seems like this node will be Vf and this node will be Vi incrementally, but if you if we have to use if we have to add bias then this should be plus some Vcm this should be plus some Vcm right. And so what will be the output voltage this will be the output and if I have to equate this picture with our total picture what will I end up with we will end up with this structure where so let me use some different color code. So, this guy like this. So, so this is k minus 1 R this is R right. So, Vf is V0 over k and the feedback loop is is closed ok fine.

So, do you see the relation do you see the similarity between this structure and this structure. So, the structure that we have in this page is essentially a very rudimentary small signal equivalent of this structure, but now we know the differential amplifier a differential amplifier has an equivalent gm an equivalent output impedance and we can then replace this differential amplifier with its with its overall overall small signal model and that was that would have been what the differential amplifier in our case a very rudimentary or a very block level way of representing a differential amplifier was this right. So, this is plus this is minus and this is some equivalent gm and it has some equivalent Rout ok. So, if the

structure on the left and the structure on the right have to be same which one do you think is Vi which which of these two input terminals is Vi and which terminal is V Vf how will you how will you go about analyzing that. So, we can do about we can go about analyzing the same using the same way that we have been doing earlier.



So, let us say we break break the loop here and we insert a we increase a voltage there right. If we increase a voltage there what is going to happen what is going to happen to V0. So, what is going to happen to the incremental current if we increase a voltage there this incremental current right this I will increase which means I am effectively drawing a current out of V0 right. So, which means V0 will decrease if V0 decreases right if V0 decreases then this guy decrease. So, the this is a negative feedback that is well and good, but what is the relationship between the terminal Vf and V0 if Vf increases V0 decreases which means there is a inverted relationship between Vf and V0 right.

So, in the in the structure in the symbol in the right which one should be Vf. So, clearly this terminal should be Vf and the other terminal should be Vi correct. So, now, if I have to if we have to equate the structure on the right and the left what should I do I should basically complete the loop by connecting the feedback around it and this becomes R this is k minus 1 ok fine. So, in case of a differential amplifier right in case of our differential amplifier this is by the way small signal equivalent right this is small signal equivalent does not show any does not show any bias ok. So, in case of a differential amplifier what is gm? gm is gm of M1 or M2 they are they are essentially the same if they are not same then we can say that this is equal to gm1 gm2 by gm1 plus gm2 and what is Rout? Rout was rds2 parallel rds4 right.

So, this is obviously on the second is obviously under the condition that M1 is equal to M2 and M3 equal to M4 otherwise rds2 I mean there were a lot of there were a lot of current

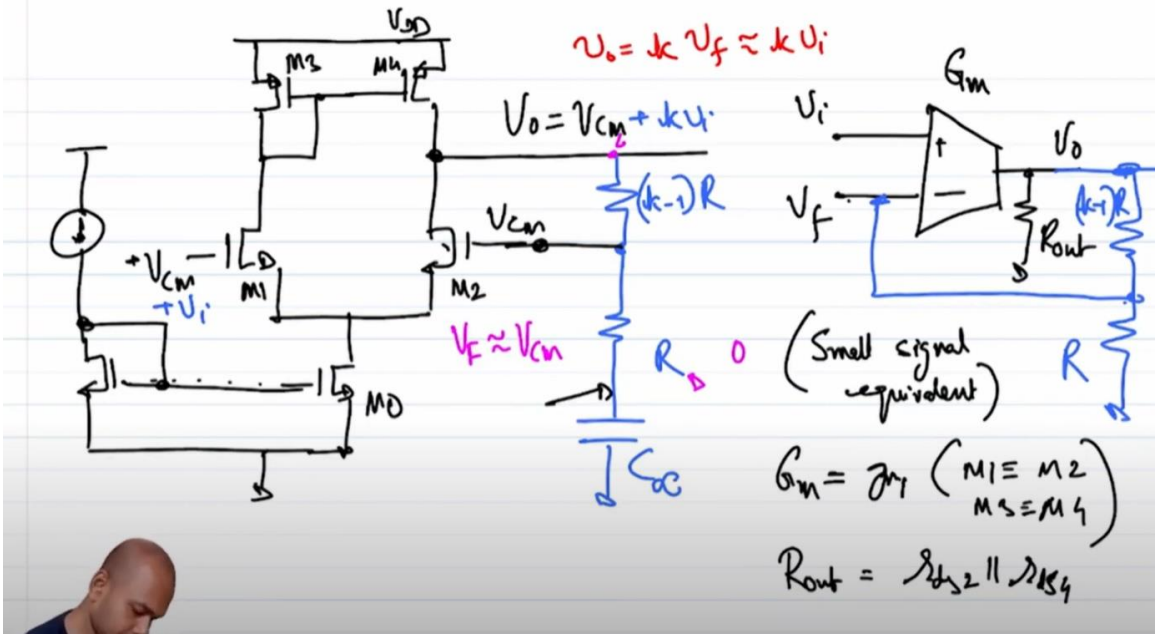
mirroring and all those things used to happen if that if those conditions wouldn't have been fulfilled then we probably will get a different expression right. So, for now let us assume that everything is identical that is M1 is equal to M2. So, this is under the condition is M1 is equal to M2 M3 equal to M4 ok fine, but there is one more rudimentary thing that we didn't talk about the stuff that we didn't talk about is if your feedback is just like when you said that feedback the gain of the amplifier has to be infinite, so the gain of the amplifier it cannot ever be infinite it has to be very large if it has to if it is large enough then what do you think what do you think V0 will be and what do you think Vf will be incrementally V0 will be K times Vf V0 will be K times Vf and Vf will be equal to Vi because of what because ultimately we saw that if the loop gain is infinity the inputs of the error amplifier have to track each other right because that was the only solution. So, which means this is equal to K times K times Vi ok. So, V0 has to be equal to K times Vi now the way I have sketched the circuit on the left right there is no distinction between the incremental and the incremental and the and the small signal equivalent and what is the implication of that the implication is the following under DC condition right under DC condition let us say we haven't applied any input right we have we haven't applied any input it is a VCM as we haven't applied any input if we apply VCM to M1 right if we apply VCM to M1 right.

So, if we apply VCM to M1 what is going to happen what is going to happen to Vf Vf will also be equal to approximately equal to Vf will approximately equal to VCM because of negative feedback large loop gain and so on and so forth. If this is equal to VCM what is this current this current is VCM over R note that we are doing quiescent right if this is VCM over R what is this voltage this voltage this voltage becomes K times VCM right. So, if K if let us say VCM is I don't know 1 volt and K is 5 then V0 becomes twice and twice 5 volt right. So, now if you are operating with a VDD of let us say 5 volt oRLess then obviously this is not possible because you cannot have any quiescent voltage larger than VDD. So, what is the solution let us say we want a gain of K but we don't want a gain of K on quiescent right.

So, what should you do? So, the obvious thing to do is to recognize the fact that this node need to be small signal ground right that need not be a absolute ground right. So, which means that what we can do is given that we know that this voltage at VF will become VCM because of negative feedback. So, what we can simply do is add a battery of value VCM here. If we add a battery of value VCM here under quiescent condition what will be this current this current will be almost equal to 0 because VF is equal to VCM which means what will be V0 under quiescent V0 will also be VCM right. So, that way your the problem of setting up the bias is solved and however incrementally this node is still rounded.

So, we are still getting an incremental gain of K correct. But now you might say that we cannot use multiple power multiple sources you are correct but what is the solution? The

solution is same old same old what we have been doing forever we can we can add a capacitor a large capacitor and call it C infinity right. If we call if this is the case right. So, what will happen to this node this node will become sorry this node will become open right this node will become open at under DC condition which means no current will flow through this stack if no current flows to this stack this will be VCM this will the loop will set this voltage to VCM V0 will be equal to VCM but V0 will be equal to VCM in the absence of input in the presence of input let us say I have an input plus VI V0 will be VCM plus K times Q. So, this way we can solve we can essentially solve the problem of that biasing voltage going out of out of range ok fine.

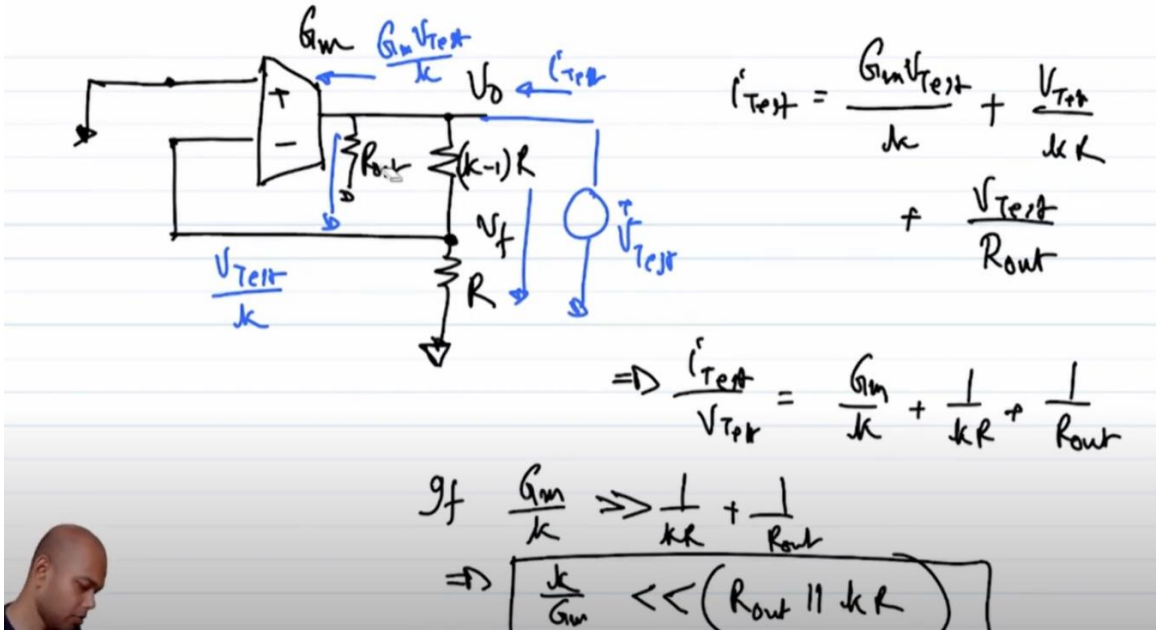


So, let us stick to this architecture for a bit more time so incrementally if this is VI this is VF incrementally this is round this is V0 this is gm right and we have to drive some output impedance let us say we have to drive some external load because ultimately we make a amplifier to drive some load. So, we need to figure out whether the amplifier has a capability to drive this load by capability I mean what do I mean essentially mean that whether whether if I put if in the absence of the load I will have some voltage right when I connect the load back will I have the same voltage or the voltage will drop appreciably. So, what is the test the test is to find out the output resistance right or the Thevenin output resistance. So, let us find out the Thevenin output resistance of this structure what will be Rout. So, in order to figure out Rout what should we do we apply a test voltage here right and find out what is I test.

So, if I apply a test voltage here what is the voltage at VF this is K minus 1 R this is R what is the voltage at VF it is Vtest over K right. So, by the way we have to short we have to short input because we are trying to find out impedance right. Desensitize all

independent voltage sources this is Vtest over K. So, what is the current that is coming out of the gm is that voltage control current source in this case the Vtest over K is appearing at the negative terminal which means the negative current will come out or in other words the positive current will get sucked in right. So, the current that will get sucked in the current that will get sucked in is gm times Vtest over K right.

Okay. So, what is the total current what is I test. I test equals gm times Vtest over K plus the current that is flowing through this node this stack which is Vtest over K over KR plus the current that is flowing through the output resistance which is Vtest over Rout. Okay. So, what is I test over Vtest that is one sorry gm over K plus one over KR plus one over Rout right. So, as long as you can ensure so if gm over K is much much greater than one over KR plus one over Rout right or in other words I can say that K over gm is much much less than the parallel combination of Rout and KR right.

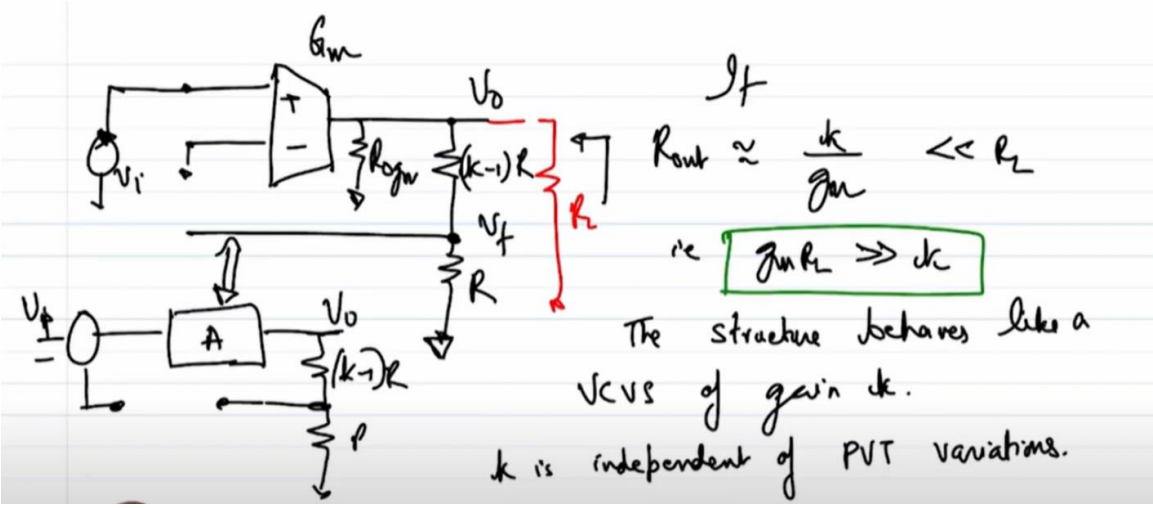


So, as long as we can ensure that right. So, this our output impedance effective output impedance so let us sketch this circuit again. I probably have to use a different terminology instead of Rout because we can use Rout of the gm right. So, this is R o gm because Rout of the entire block should be of should be called Rout R o gm. So, what is the output impedance after this Rout becomes almost equal to K over gm and as long as this is much less than RL if this is true right or that is as long as gm times RL.

So, what is RL? RL is resistance that I am planning to planning to drive as long as gm RL is much much greater than the intended gain K right. The structure behaves like a CVS of gain right ok. So, this is something that is a very good thing because what is K? K is a ratio of resistances and K is note that K is independent of process voltage temperature variations

ok. So, if you recall the characteristics of a good voltage control voltage source that we desire was we should have gain of at least more than 1 that is for sure. We should have the gain which is independent of RL and we should have a gain which is independent of PVT right.

So, a simple common source amplifier was able to give us a gain of more than 1 ok, but it was not able to give us a gain which is independent of PVT and it was also not able to give us a gain which was independent of RL. Now, if we consider and we say that ok if the intrinsic if the GDS or if the RDS of our common source amplifier the output impedance of the common source amplifier was much lower than RL then sure we get a gain which is independent of RL. Yes indeed we get however still the third point is not valid that is again is still dependent on process voltage temperature right. However, when you make a feed when you make an amplifier using the principles of negative feedback it is possible to meet all three criterions that is you make a amplifier of gain K, but K has to be I mean obviously K has to be greater than equal to 1 else it does not make a difference. So, as long as K is more than equal to 1 you can use the principles of negative feedback to get a amplifier of gain more than 1 right.



Now, however you see that there are certain issues right the what are the issues and the issue that this structure has is we saw that the what was the output range output common mode range what was the range at with what was the range that the output is output can swing till all the transistors are in saturation. For example, if I take this guy Vo what is the maximum it can swing to the maximum it can swing to is VDD minus 1 over drive voltage of M4. So, that is good it can swing quite high towards the supply voltage right, but what is what is the lower side problem how low can we not go Vo only can go Vcm minus 1 threshold voltage right. Since Vo can go only Vcm minus 1 threshold voltage then which means that we can potentially have a problem because you are not allowing the output to swing too much right. So, that is one problem what is another problem another potential

problem is if RL is very low right.

So, which means that let us say we are not able to meet this criteria we are not able to meet these criteria gm RL is much much greater than k then RL will end up loading our differential amplifier right. If RL becomes if RL if this is if a differential amplifier gets loaded then we will not be able to impose the same condition that the gain is very high right. What is the gain what in that condition of A what is the gain the gain is that gain right. So, if I have to equate this structure with if we have to equate this structure with this structure what is the what is the gain if I have to equate these two structures. So, even without getting into too much detail what we need to do to figure out the gain we can simply disconnect the feedback we can simply disconnect the feedback and find out the gain between Vi and Vo right.

So, if I disconnect the feedback if I disconnect the feedback here and let us say incrementally grounded what will be the gain between Vi and Vo and if I apply Vi here the gain will be gm times the all the resistances in parallel correct. So, if that gain if A the gain becomes gm times all the resistance in parallel if that gain goes to much closer to 1 right if A has to be ideally infinite that gain has to be much closer to infinity or rather it has to be high right. So, if that gain becomes lower what is loweRLower is the gain has to be with respect to 1 right you remember it was like loop gain by 1 plus loop gain. So, if the gain becomes comparable to 1 then the all the good things of negative feedback go for a toss your gain your negative feedback will no longer be valid which means youRoutput will not be k times Vi which means you are going to have more and more steady state steady state error so on and so forth right. So, hence you have to ensure that the open loop gain right after you break the loop you will find an open loop gain that open loop gain has to be much more than 1 right.

So, if the open loop gain is less than 1 then we are in trouble right. Thank you.