**Course name- Analog VLSI Design (108104193)**
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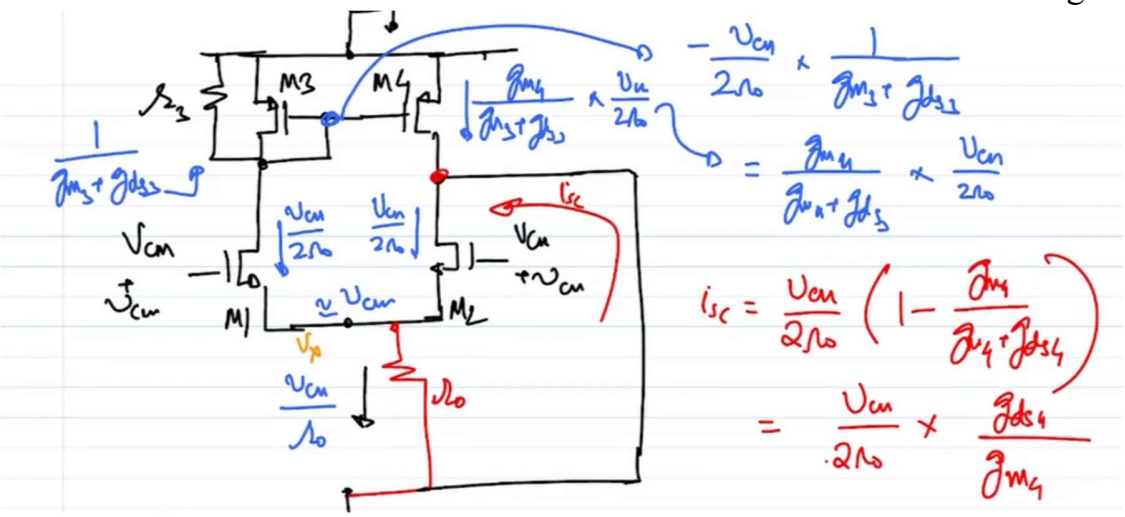
So, till now we have been dealing with this differential amplifier and you must have noticed that I have used this constant current source at the source and we had done that earlier also when we were dealing with differential amplifier with resistive loads and then we replace the current source with a more realistic thing and that was a current mirror based current mirror based configuration and what did that do? What effect did this transistor have? The effect this transistor had was on the common mode response of the circuit because why am I saying common mode? Why not differential? Because if you consider differential modes right, so then if this is plus delta V, this is minus delta V then the total voltage swing at this node Vx is 0 right. If the total voltage swing is 0 then essentially this the existence of this external resistance existence of this rds right, this parasitic resistance of M naught is irrelevant because no current is flowing through R naught right. However, if we have common mode excitation, if we have common mode excitation let us say we have plus delta V here and plus delta V here right. Then what? Then we cannot neglect right because if this happens then what is the voltage swing here? This is approximately equal to delta V right. So, as far as the voltage swing at this node Vx is concerned that is same I mean that was almost equal to delta V in the previous architecture. So, do you think it is the same in this architecture? It is kind of the same right, why am I saying it is kind of the same? It is because nothing has changed if I look this side, something has changed on the top side but nothing has changed on the bottom side of the as far as the working of M1 and M2 is concerned right.

So, it is quite natural for us to expect that the voltage swing at this node Vx is almost equal to delta V correct. So, okay fine if that is the case now note that it cannot be exactly delta V, if it is exactly delta V which means that

there cannot be knowing there cannot be any incremental current through M1 and M2. So, this is approximately delta V right. So, if that is approximately delta V what is the current through R0? So, since we are doing common mode excitation now, so I can as well get rid of I mean let us do incremental right.




So, if I do incremental then we can get rid of this M0 and all these things right. So, what is the current through R0? Current through R0 becomes delta V or let me call it Vcm right instead of delta V let me call it Vcm small Vcm. So, that helps us and make the point that we are talking about incremental common mode excitation right. So, if this is also approximately Vcm, so what is the current through R0? Current through R0 is Vcm by R0. So, where will this R0 flow once it reaches that node Vx it will get split into two branches equally right.

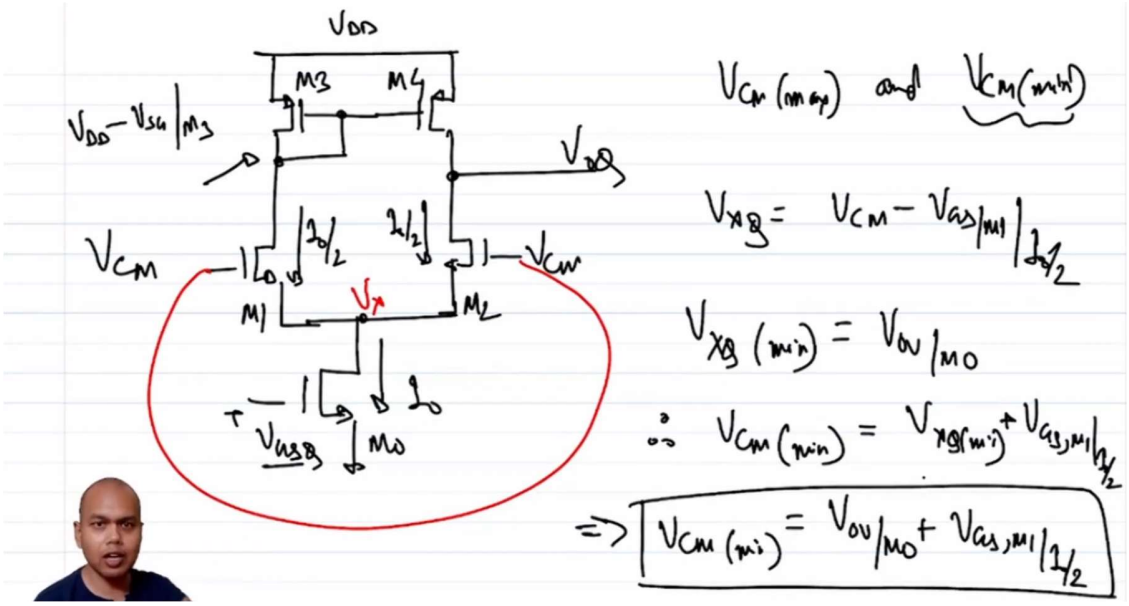
So, it will get split into two branches equally. So, this will be Vcm over 2 R0 and this will be also Vcm over 2 R0. Now, note that why are we doing this we are trying to find out the common mode gain of this architecture right. We already found out the differential equivalent of this architecture differentially that equivalent trans conductance was the gm of M1. We now are trying to figure out what is the common mode response of this architecture right.

So, in order to do that let us incrementally short this also because otherwise

it is I mean we would like to normalize everything in the end right ok. So, if this is Vcm by R0 this Vcm by R0 on the left branch that is flowing through M1 flows through M3 this is also Vcm by 2 R0 correct. So, this current gets copied through M4. So, this also this becomes Vcm by 2 R0. So, what is the current that is flowing into the incremental short? This is 0 right Vcm by 2 R0 is coming from top Vcm by 2 R0 is being dragged out.

So, essentially the incremental current in the short is 0 right which what does this tell you this is essentially telling us that the common mode response of this network is this network does not respond to any common mode excitation right. That is what it is telling us, but whenever you get something to be 0 or infinity then you have to step back and start thinking did I neglect something because of which we are getting 0. Because note that we cannot neglect anything with respect to 0 right ok. So, what are the things you think we might have neglected? So, we neglected channel and modulation we neglect channel and modulation for M3 and M4 right. So, if we do not neglect that right if we do not neglect that what is going to happen.

So, let us put in channel and modulation which means that we have R3 and we have R4, but R4 is irrelevant because both sides of R4 are shorted right. So, I can essentially make essentially say that channel and modulation of M4 is irrelevant. So, that goes out of the window ok. So, what about this Vcm by 2 R0 where does this Vcm by 2 R0 go? Vcm by 2 R0 goes and develops a voltage at this node. What is the impedance looking up? What is the impedance looking up? The impedance looking up is 1 over gm3 plus gds3 right.




If that is the impedance looking up what is this voltage? This voltage becomes minus Vcm by 2 R0 times 1 by gm3 plus gds3 correct. So, at this time you might be telling us telling me a why do not you neglect gm3 now, why do not you neglect gds3 now? So, the reason I am not neglecting gm3 is the following. So, if we neglect gds3 with respect to gm3 what will be the current through M4? The current through M4 will be gm3 times this correct gm3 times this in the direction pointing down right gm3 times this including the negative sign in the pointing in the direction pointing up, but if I flip the current direction this will become gm3 times Vcm by 2 R0 times 1 over gm3 which means again we are we will be getting Vcm by 2 R0 pointing down. So, neglecting gds3 will lead to the same answer that is 0 right. So, we are trying to figure out if neglecting channel length modulation has caused a problem or not right.

So, we cannot neglect it now. So, if this is the case what is the current through M4 in the point in the direction pointing downwards this will be gm4 by gm3 plus gds3 times Vcm by 2 R0 using the incremental model you can as well say it is pointing upwards with a minus direction right because Vg is negative right, but I can as well say I flip the current direction and point it towards the ground towards bottom right fine. If this is the case so this is almost equal to what this is not almost exactly equal to if gm3 and gds3 are same gm3 and gm4 are same. So, this becomes let us say gm4 by

gm4 plus gds3 times Vcm by 2 R0 right. Do you think there is less than Vcm by 2 R0 or greater than Vcm by 2 R0 this clearly less than Vcm by 2 R0 right.

So, essentially there will be a difference current that will flow there will be a difference current that will flow in this through this short right in order to if basically if I solve right KCL at this node I should see an extra current flowing through the short what will be that extra current. So, Isc what will be Isc? Isc will be Vcm by 2 R0 minus this new guy right. So, essentially Vcm by 2 R0 1 minus gm4 by gm4 plus gds3 gds3 and gds4 are same. So, let me put gds4. So, this becomes Vcm by 2 R0 times gm right times gds4 by gm4 plus gds4.

Now, I can neglect gds4 with respect to gm4 right because I mean we have solved that problem of things getting cancelled and becoming 0 right ok. So, this becomes a short circuit current right. Note that if we neglect gds4 right if gds4 becomes 0 then clearly our short circuit current also becomes 0 right. So, ok. So, this becomes a short circuit current and what is the then what is the common mode equivalent what is the incremental equivalent for a common mode differential for the common mode input in a differential amplifier.

So, for common mode inputs the incremental equivalent becomes note that in this case the current direction is this right because the current is flowing from the short into the device. So, the current direction reverses and this becomes Vcm by 2 R0 right times gds4 over gm4 times gds4 over gm4 and what is output resistance output resistance are then change that is whatever we figured out in the previous module that is rds2 parallel rds4 right. So, this becomes a V o c m. So, this becomes V o c m and right and for differential mode what was it what was the equivalent what was the equivalent Norton what was the Norton equivalent Norton equivalent was gm times V diff right gm times V diff and output resistance remains rds2 parallel rds4 right. So, this would have been the differential mode equivalent right V o diff of our differential pair correct.

So, this part we have dealt it in detail this is the new part and what is the observation the observation here is there are two fold observation you ideally would want the common mode response to be 0 right. So, under what condition do you see the common mode response becoming 0 there are two cases if we neglect the channel and modulation of if we neglect the channel and modulation of the tail transistor which means R naught tends to infinity then the incremental current the incremental common mode current goes to 0 that makes sense because that is equivalent to saying we are using a ideal current source at the tail node. Alternatively if we neglect the gds if we neglect the channel modulation of m3 then also we see that we can we can we are likely to get 0 common mode response right. So, what does it what does it translate to in terms of designers choice in terms of designers choice if you are looking to get low common mode rejection right or rather high common mode rejection or low common mode out response then you have to do one of these two things either you make you cannot ever have an ideal current source, but you have to make R naught to be larger. How do you make R naught larger R naught for the tail transistor larger you have to increase the length of the transistor right you have to increase the length of the transistor and if you do not want to impact the current then you have to increase the W also essentially you have to increase the size of the difference.

So, that will help in increase increasing the R naught right similar things you will have to do in case of m3 and m4 as well right. So, that will give you decent common mode rejection ok. So, before we stop on this on this differential pair let me talk about one more specification that is also quite vital while trying to figure out while trying to design a differential pair and that is the range of inputs the range of acceptable inputs that your our transistor can take right. So, let us say I have this is biased let us say m naught is biased with a constant current source and you have some Vgsq right. So, we know how to do this we are not particularly bothered and let us say I naught is here and here I have Vcm and I have Vcm ok fine.

So, what I am what essentially I am asking is what is the what is the limit of whenever app when we apply an input right when we apply input we are

applying the input to the inputs of m1 and m2 right. So, if we have if we have transistors biased using Vcm essentially what you are asking is how far can you push the Vcm up or down before the transistor goes out of its operating region right or rather which transistor will start going out of its operating region that is of interest to us ok. So, for that we need to first understand what are the bias points right. If we know the bias points we know the quiescent voltages and currents of all nodes then it is easy to figure that one out right.

So, let us do that. So, let us assume that I mean so even before we assume let us see which bias points we know accurately if things are biased properly right if things are biased properly this current through m1 is I naught by 2 current through m naught is I naught by 2 right. What is this voltage? This voltage will be Vdd minus Vsg of m3 for a bias current of I naught by 2 this we also know. What is the voltage at V naught? This we do not know right because that is a high impedance node right that is the node that is giving us gain. So, we do not know exactly what is that voltage because the current through m2 and m4 can as well be I naught by 2 for a range of voltages of V naught right because that is the drain voltage of m2 and m4 and ideally a change in drain voltage should not should not lead to any change in current right. So, which means that multiple solutions for V naught is possible ideally ok.

So, which means that we have to assume certain value of V naught. So, let us assume V naught is at some V naught Cm or some V naught Q and that V naught Q has to be set by some external factors we have we have not yet seen how the external factors set V naught Q, but let us assume it is set right it is given to you by somebody. So, then a question that we are asking is what is V Cm V Cm max and what is V Cm min. This is equivalent to the swing limits condition that we have done for single transistor circuits right ok. So, what do you think how should we go about doing analyzing this.

So, let us do the V Cm min first because you will see that this is slightly simpler to there is a continuity to what we are doing. So, what do you think is likely to happen if I connect these two nodes and yank them up and down

right they are connected on V Cm I connect V Cm up I pull V Cm down below its quiescent point what is going to happen. So, this is equivalent to saying that I have a common mode excitation right I am pulling V Cm down and this is equivalent to saying that I have a common mode excitation. So, if V Cm goes down on both arms which node is I mean do you think the current will change if I assume in if I assume that I mean if I neglect channel and modulation and all right if I neglect channel and modulation of M naught do you think reducing V Cm will change current no it would not right. So, but what is going to change because the current is not going to change the Vgs of M1 and M2 will remain constant right if Vgs remains constant the node voltage of Vx is supposed to drop right because I am dropping the gate voltage the Vx is supposed to drop.

So, what is Vxq? Vxq was V Cm minus Vgs of M1 for a current of I naught by 2 which is same as V Cm minus Vgs of M2 for a current of I naught by 2 right. So, what is the minimum that Vx can go the minimum can the minimum Vxq, Vxq min is essentially the overdrive voltage of M naught right is Vgsq minus the threshold voltage right. So, this is V overdrive of M naught right which means that which means what which means therefore V Cm min is Vxq min plus Vgs of M1 for a current of I naught by 2 which means the minimum V Cm becomes V overdrive of M naught plus Vgs of M1 for a current of I naught by 2 right. So, this is V Cm min right. Do you think anything else is going to affect do you think the voltages at the gate of M3 is going to change? No right because the current has not changed the voltage at the gate of M3 is not likely to change correct ok.

So, often this V Cm min is also called input common mode range the lower limit right. So, this is I CMR minus right. So, this is often called I CMR minus this is abbreviation of input common mode range lower limit the minus corresponds to the lower limit. So, let us see what is going to happen to the upper limit then ok.

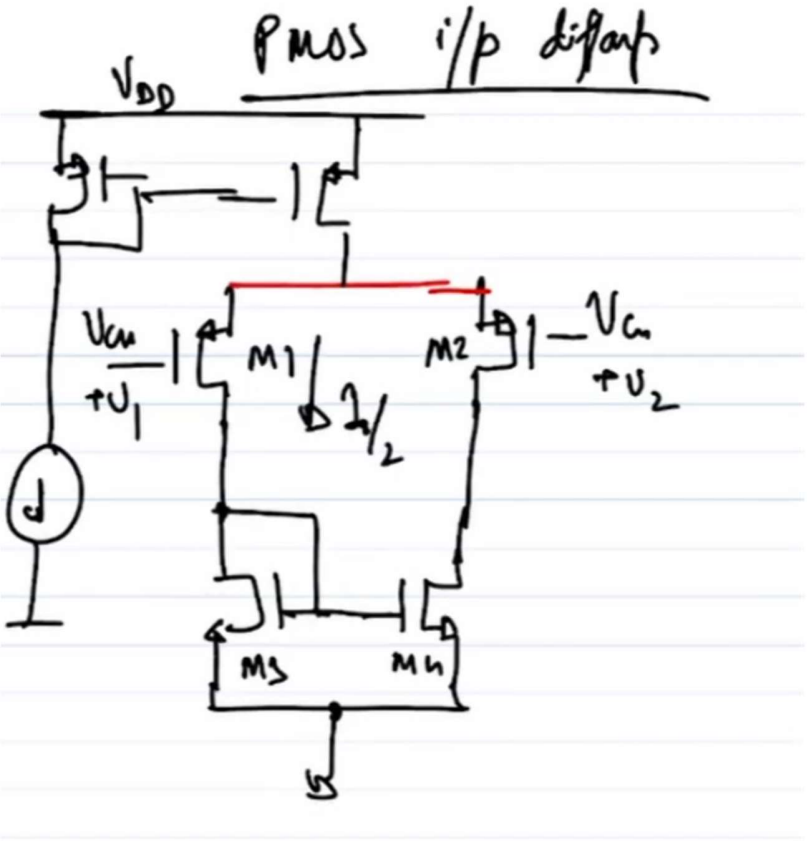
So, let us see that. So, now let us see let us assume that we are yanking this voltage up we are yanking this voltage up ok. We are yanking V Cm up

both sides. So, what do you think is going to happen to Vx? This Vx is going to increase right because Vgs has to be same. So, do you see a problem with M naught going out of saturation? No obviously not right, but what is going what is likely to be the problem? So, if V Cm increases if current is current does not change if I neglect channel modulation do you think the gate voltage of M3 or do you think the drain voltage of M3 is going to change? No, because current has not increased. So, which current has not changed which means what? How far can I raise V Cm? I can raise V Cm till till we reach right.

So, V Cm or rather the condition with is the drain voltage of M1 has to be the drain voltage of M1 has to be greater than equal to the gate voltage this is V Cm minus 1 threshold voltage right which means that Vdd minus V sg of M3 has to be greater than V Cm minus 1 threshold voltage right. So, which means that V Cm has to be less than Vdd minus Vdd plus 1 threshold voltage minus V sg of M3 right. So, this is as far as a constraint on or this is constraint on on M1 right M1 inset. What about M2? So, M2 inset what will be the constraint? So, note that instead of the drain voltage of M2 is what? Is Voq and I as we initially assume Voq is being said by something else we do not know what is it what it is. So, essentially whatever is setting Voq will determine the will end up having an impact on how far that the gate voltage of M2 can go and in that case what will be the constraint it will be V Cm should be less than equal to Voq plus threshold voltage M right.

So, what will be the maximum V Cm? The maximum V Cm will be the minimum of this and that right. So, ICMR plus will be minimum of Voq plus Vthn or Vdd plus Vthn minus V sg of M3 right whichever is smaller will be your input common output range upper limit range beyond this you will not be able to use increase V Cm. So, these are an important parameter because ultimately when you are using a differential amplifier you need to know till what range you can give your inputs you cannot apply any input or of any range right. So, that becomes important parameter right. So, before we stop before we stop on the single stage differential amplifier what I would like to point out is everything that we have developed till now has been by using an nMOS transistor right.

So, in other words so this is what our circuit has been right from the beginning right. So, this is what the circuit has been right from the beginning at least right from the beginning of today's lecture, but whatever we have been doing till now has been under the condition that the input is being applied to an nMOS transistor just like in case of a common source amplifier we started off with an nMOS transistor in case of a differential amplifier also we started off with nMOS transistor we assume the input is being applied to the nMOS transistor, but equivalently you can have a complementary scenario where the input is applied to a pMOS transistor. So, essentially we flip the entire thing just like in case of a common source amplifier with the nMOS input we could have flipped it and made it a pMOS input. So, we can do the same thing here and if we do that what is going to happen I mean we use the same principle current flows from right current flows from high potential to lower potential in case of a pMOS transistor the current will flow from a source to drain right. So, let us replace one transistor at a time whatever is nMOS will make it pMOS whatever is pMOS will make it nMOS and let us see what happens right.




So, let us see so in case of M1 so let us say the equivalent for this is the pMOS equivalent pMOS input differential pair with M right. So, M1 is nMOS in our case so M1 let us replace M1 with the pMOS transistor. So, let us replace M2 with the pMOS transistor. So, let us call this M1 here M2 there ok. So, where will what will be the current direction in M1 and M2 naturally the quiescent current flows from source to drain.

So, the quiescent current here has to flow from it has to be I0 by 2 from top correct. So, in case of a in case of the nMOS equivalent what is connected to the source we have a we have a current source connected to the source essentially this is a I mean essentially this is this thing right this is an I0 connected to the source right. I am sinking current out of the source in case of a pMOS I should be sourcing current of I0 correct ok. Fine. So, what is now let us replace M3 and M4 in the differential in the circuit in the left M3 and M4 are pMOS we will make them nMOS right.

So, let us make them nMOS and their gates are connected the sources are connected and what is connected to the source in case of in case of the circuit of the left that source of pMOS is connected to the highest potential VDD in our case the M3 and M4 source will be connected to the lowest potential that is that is ground. What should we do with the drain and the gate of M3 in the circuit in the left the drain and the gate of M3 are shorted here also we do the same thing and we apply VCM here VCM here and if we have to apply an input we can apply an input just like this right. So, now, if we have to replace this I0 what can I do in we go back to the transistor level equivalent M0. So, if you have to replace that I0 we replace this with a current mirror a pMOS current mirror which we have done multiple times before right.

So, this is a known circuit right. So, this becomes a pMOS equivalent differential amplifier right. So, whatever is valid for the circuit in the left is also valid for the circuit on the right incremental equivalent is identical right. So, incremental Norton equivalent is identical for both the circuits because incrementally there is absolutely no difference between an nMOS and a pMOS transistor, but what will be different what will be different the difference will be in terms of quiescent points right. So, what I would request you to do is solve for whatever we have done right ICMR plus ICMR minus output resistance right, GM flow of current directions right all these things for the pMOS equivalent plus S right. Thank you. .